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DSRC Applications in Intelligent Transportation System using SOLS Technique for fully reused VLSI Architecture

B. Priyanka
PG Scholar
Department of ECE
Vaagdevi College of Engineering
Bollikunta, Warangal

Madupu Sanjay
Asst. Professor
Department of ECE
Vaagdevi College of Engineering
Bollikunta, Warangal

***Abstract*—The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the postlayout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.**

***Index Terms* - Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.**

1.1 Introduction

Dedicated Short Range Communication (DSRC) is a protocol used for communication for a short range of distance, say a few hundred meters through a dedicated channel. It is used to introduce intelligent transport system into our day to day life. The DSRC communication aids in both vehicle to vehicle communication as well as vehicle to roadside communication. The vehicle to vehicle communication mainly deals with the collision alarms, hard break warnings etc. At the same time the vehicle to infrastructure communication includes the Electronic Toll Collection (ETC), highway-rail intersection warning, in vehicle signing etc. However the primary motivation of the DSRC communication channel is collision detection and vehicular safety. In addition to it, it also aids in smooth traffic control. The DSRC equipment mainly consists of three modules namely; base band processors, RF front end and the microprocessors. The microprocessors are responsible for scheduling the tasks of base band processing and RF front end and intercept the instructions. The RF front end takes care of the transmission and reception of data. Finally main function of the base band processing includes modulation, error correction, clock synchronization, and encoding. For the purpose of encoding data, normally an FM0 or

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Manchester encoding are used so as to reduce the chances of occurrence of noise in the channel when it is left idle. When a system that can be reused between both the FM0 and the Manchester encoding is implemented, the hardware utilization rate is reduced thereby reducing the efficiency. This in turn affects the performance of the system. Hence a new method of designing a reusable VLSI architecture is proposed. This novel method of designing called the Similarity Oriented Logic Simplification (SOLS) improves the hardware utilization rate of the reusable architecture thereby improving the performance and area footage.

2. Related Technologies

2.1 DSRC Protocol

Dedicated short range communication (DSRC) is a fast, short to mid range, wireless technology. It enables one way or two way communication between vehicles or between vehicles and roadside. It is to used make streets safer, travel easier and minimizes the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per second. [1] In DSRC communication, the most important concern is collision detection. Each DSRC equipped vehicle broadcasts its basic information including speed, trajectory, location etc to a short range of distance, say a few hundred meters. All other DSRC equipped vehicles in the vicinity receives this message. Later on this message is decoded by the receiver vehicles and a caution or warning may be issued to the driver. This can be issued audibly, visually or haptically [3]. The DSRC communication is based on direct communication between vehicles and hence does not need networking. Therefore it is also referred to as single hop. This type of communication can also be referred to as uncoordinated broadcast messaging. Each DSRC equipped vehicles can extend this network to its neighbors and hence this network can grow unbounded. In case of safety, privacy is also an important concern. Therefore all safety communications are carried out in the control channel only. The safety communication involves two types of messages:

- Routine safety messages: These are status messages including change of speed, location, etc that are regularly sent by the vehicle.
- Event safety messages: These are messages that signify an event like a hard brake.

3. Methodology

3.1 FM0 Encoding

FM0 encoding is also a type of Non-Return to Zero code. It is also used to represent the binary signals in a digital system. In FM0 encoding, even though the data stream does not encounter transition, the encoded signal experiences a transition for every clock cycle. The FM0 encoding can be specified by using the three basic rules[1]. They are as follows:

1. There should be transition for every logic zero input within a clock cycle.
2. There should be no transition for logic one input.
3. There should be a transition after every clock cycle irrespective of the input data.

These rules can be better be explained by using the diagram (Fig 2).

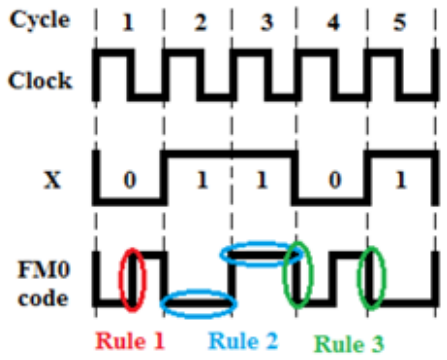

Figure 2: FM0 encoding

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FM0 encoding can be realized by using two flip-flops and also multiplexers. The FM0 encoding can be implemented by using the block diagram as shown below in fig 3. In the following block diagram, A(t) and B(t) signifies the two states.

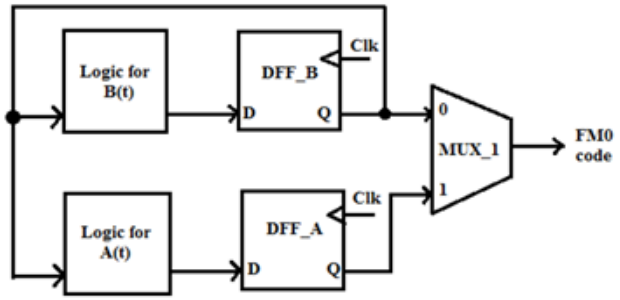

Figure 3: FM0 encoder

3.2 Manchester Encoding

One of the most common data coding methods used today is Manchester encoding. Manchester coding gives a way of adding the data rate clock to the message to be used at the receiving end. To represent the binary values 1 and 0 in digital system, the Manchester codes are used. Manchester code represents binary values by a transition rather than a level. Manchester coding states that there will always be a transition of the message signal at the mid-point of the data bit frame. What occurs at the bit edges depends on the state of the previous bit frame and does not always produce atransition. A logical 1 is defined as a mid-point transition from low to high and a 0 is a mid-point transition from high to low.[1] An example of a Manchester encoding is shown below in Fig 4.

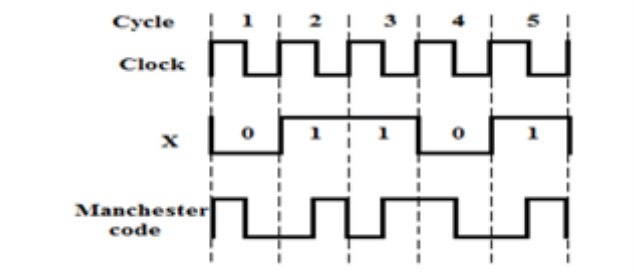

Figure 4: Manchester Encoding.

The Manchester encoding can be implemented using an XOR gate where the clock signal and the data signal are XORed together to obtain the encoded data as shown in the diagram below (Fig 5.)

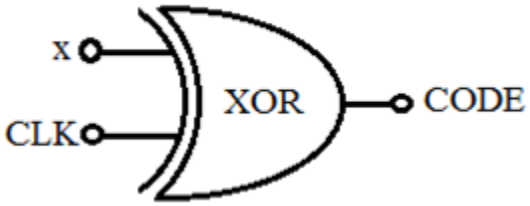

Figure 5: Manchester encoder

3.3SOLS Technique

Normally DSRC encoders make use of both the FM0 and the Manchester encoding. Hence both the encoders can be combined together to form a reusable encoder. Such a reusable encoder can be illustrated as shown in the figure 6.

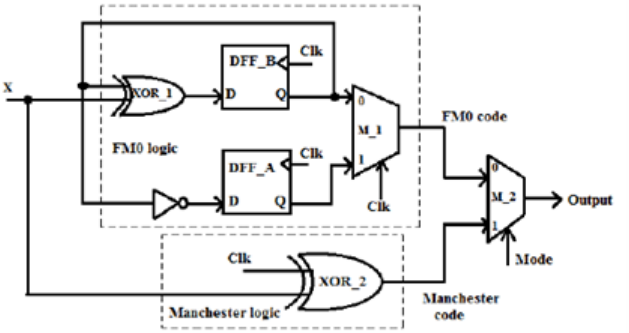

Figure 6: Reusable encoder

This block diagram can be further simplified using the SOLS technique. The SOLS encoder consists of mainly two methods, area compact retiming and the balance logic simplification.

4. VLSI Architecture Design of FM0 Encoder And Manchester Encoder Using Sols Technique: The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. The SOLS technique is classified into two parts: area-compact retiming

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and balance logic operation sharing. Each part is individually described as follows. Finally, the performance evaluation of the SOLS technique is given.

A. Area-Compact Retiming: The FM0 logic in Fig. 6 is simply shown in Fig. 7(a).The logic for *A(t)* and the logic for *B(t)* are the Boolean functions to derive *A(t)* and *B(t)*, where the *X* is omitted for a concise representation. For FM0, the state code of each state is stored into DFF*A* and DFF*B*. According to (2) and (3), the transition of state code only depends on $B(t-1)$ instead of both $A(t-1)$ and $B(t-1)$.In Fig. 7(b), when the CLK is logic-0, the *B(t)* is passed through MUX−1 to the *D* of DFF*B*. Then, the upcoming positive-edge of CLK updates it to the *Q* of DFF*B*. As shown in Fig. 8, the timing diagram for the *Q* of DFF*B* is consistent whether the DFF*B* is relocated or not. Suppose the logic components of FM0 encoder are realized with the logic-family of static CMOS, The transistor count of the FM0encoding architecture without area-compact retiming is 72,and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

B. Balance Logic-Operation Sharing: As mentioned previously, the Manchester encoding can be derived from $X \oplus \text{CLK}$, and it is also equivalent to $X \oplus \text{CLK} = X\,\overline{\text{CLK}} + \overline{X}\,\text{CLK}$. (6)
This can be realized by the multiplexer, as shown in Fig. 9(a).It is quite similar to the Boolean function of FM0 encoding in (4). By comparing with (4) and (6), the FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of CLK. As shown in Fig. 9(b),the concept of balance logic-operation sharing is to integrate the *X* into *A(t)* and *X* into *B(t)*, respectively. The logic for *A(t)/X* is shown in Fig. 10. The *A(t)* can be derived from an inverter of $B(t-1)$, and *X* is obtained by an inverter of *X*. The logic for *A(t)/X* can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of $B(t-1)$ and *X*. The Mode indicates eitherFM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for *B(t)/X*, as shown in Fig. 11(a). Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The *X* can be also interpreted as the $X \oplus 0$, and thereby the XOR operation can be shared with Manchester and FM0 encodings.

The CLR is the clear signal to reset the content of DFF*B* to logic-0. The DFF*B* can be set to zero by activating CLR for Manchester encoding. When the FM0 code is adopted, the CLR is disabled, and the $B(t-1)$ can be derived from DFF*B*. Hence, the multiplexer in Fig. 11(b) can be totally saved, and its function can be completely integrated into the relocated DFF*B*. The proposed VLSI architecture of FM0/Manchesteren coding using SOLS technique is shown in Fig. 12(a). The logic for *A(t)/X* includes the MUX−2 and an inverter. Instead, the logic for *B(t)/X* just incorporates a XOR gate.

In the logic for *A(t)/X*, the computation time of MUX−2 is almost identical to that of XOR in the logic for *B(t)/X*. However, the logic for *A(t)/X* further incorporates an inverter in the series of MUX−2. This unbalance computation time between *A(t)/X* and *B(t)/X* results in the glitch to MUX−1,possibly causing the logic-fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between *A(t)/X* and *B(t)/X* is shown in Fig. 12(b). The XOR in the logic for *B(t)/X* is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for *A(t)/X*. This shared inverter is relocated

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backward to the output of MUX−1. Thus, the logic computation time between *A(t)/X* and *B(t)/X* is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller.

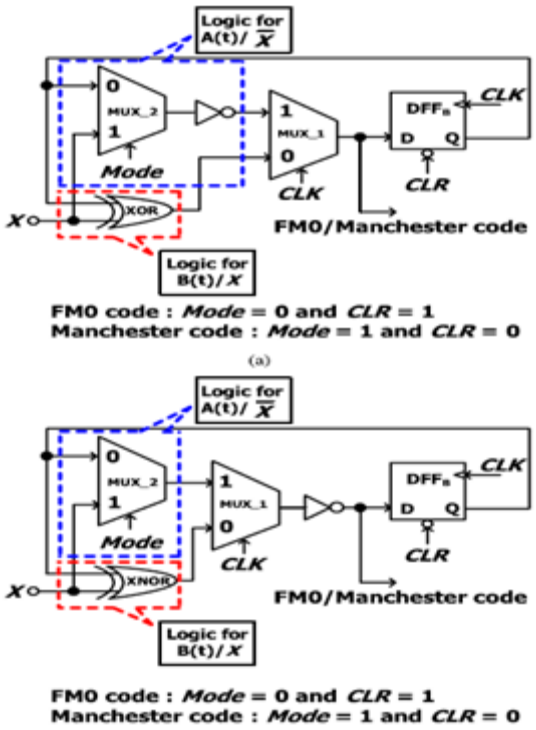

Fig.12 VLSI architecture of FM0 and Manchester encodings using SOLStechnique.
(a) Unbalance computation time between *A(t)/X* and *B(t)/X*.
(b) Balance computation time between *A(t)/X* and *B(t)/X*.

C. Timing Analysis

The logic functions of SOLS technique can be realized by various logic families. Each logic family optimizes one or more electrical performance, such as area, power, or speed, from circuit topology perspective instead of architecture perspective. The proposed SOLS technique is developed from architecture perspective to achieve 100% HUR. Among the logic families, both static CMOS circuit and transmission gate logic are widely applied in digital circuit owing to their superior integration in process manufacturing. Hence, the timing analysis is given under these two kinds of logic families for a more general purpose. Although the SOLS technique enables the VLSI architecture to be fully shared for Manchester and FM0 encoders, their critical paths are not identical. For Manchester encoding, the delay time is given as

*T*Man= max{*T*MUX, *T*XNOR} + *T*MUX + *T*INV (7)

$$T_{\text{Man}} = \max\{T_{MUX}, T_{\text{XNOR}}\} + T_{\text{MUX}} + T_{\text{INV}} \quad (7)$$

where T_{Man} denotes the delay time of Manchester encoding.The T_{MUX}, T_{XNOR}, and T_{INV} represent the delay time of the multiplexer, the XNOR gate, and the inverter, respectively.

The DFF*B* is always kept at logic-0 in Manchester encoding; therefore, it is excluded from *T*Man. This delay path is also incorporated into that of FM0 encoding. Moreover, the FM0encoding applies the DFF*B* to store the sate code, and thereby the delay time of DFF*B* is further considered as

$$T_{\text{FM0}} = T_{\text{Man}} + T_{\text{DFF}} \quad (8)$$

For simplicity, both rise and fall times of static CMOScircuit are assumed to be identical. The fall time is adoptedto denote the propagation delay with Elmore delay estimation.The static CMOS topologies of two-input multiplexer and twoinputXNOR are shown in Fig. 13(a) and (b), respectively.The pull-down network of two-input multiplexer includesM_1, M_2, M_3, and M_4. The M_1 and M_2 are in parallel, and so are M_3 and M_4. Indeed, this connection can improve the discharging capability. However, the transistor sizing still considers the worst case where the discharging path is constructed by only two

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transistors in series. The propagation delay of the static CMOS two-input multiplexer is given as

$$T_{\mathrm{MUX-SC}} = T_{\mathrm{INV}} + C_A R + C_B 2R \qquad (9)$$

The *CA* aggregates the junction capacitances of M_1, M_2, M_3, and M_4. The *CB* gathers the junction capacitances of M_3, M_4, M_5, and M_6. Similarly, the propagation delay of static CMOS two-input XNOR is given as

$$T_{\mathrm{XNOR-SC}} = T_{\mathrm{INV}} + C_C R + C_D 2R. \qquad (10)$$

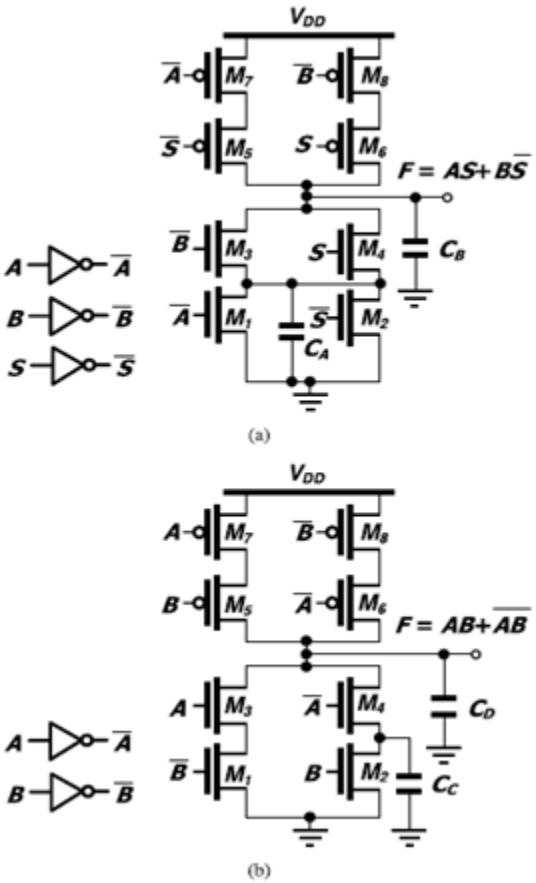

Fig. 13.Static CMOS topologies of multiplexer and XNOR. (a) Two-input multiplexer. (b) Two-input XNOR

In Fig. 12(b), for static CMOS, the series of MUX−1 andMUX−2 dominates Manchester encoding path and leads to a total propagation delay as

$$2T_{\mathrm{MUX-SC}} = 2(T_{\mathrm{INV}} + C_A R + C_B 2R). \qquad (11)$$

5 Conclusion

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors.

The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding deviceefficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively.

The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

References

[1] F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., “Vehicle safety communications—Applications (VSC-A) final report,” U.S. Dept. Trans., Nat. Highway Traffic Safety Admin., Washington, DC, USA, Rep. DOT HS 810 591, Sep. 2011.

[2] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.

[3] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Design of 5.9 GHz DSRC-based vehicular safety communication," IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36–43, Oct. 2006.

[4] P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156–1159.

[5] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, "A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz," in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1–4.

[6] Y.-C. Hung, M.-M.Kuo, C.-K.Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester and Miller encoder," in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541.

[7] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based Manchester encoder for UHF RFID tag emulator," in Proc. Int. Conf. Comput., Commun. Netw., Dec. 2008, pp. 1–6.
[8] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FM0 and Miller encoder for UHF RFID tag emulator," in Proc. IEEE Adv.

Comput. Conf., Mar. 2009, pp. 1317–1322.

[9] J.-H. Deng, F.-C.Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in Proc. Adv. Commun. Technol. Jan. 2013, pp. 98– 03.

[10] I.-M. Liu, T.-H.Liu, H. Zhou, and A. Aziz, "Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay," in Proc. Int. Workshop Logic Synth., May 1998, pp. 162–168.

Author's Profile:

Author-1:

Ms. PRIYANKA BOSKA receiving her PG degree specialized in VLSI in Vaagdevi College of Engineering, Bollikunta, Warangal in the year 2015 and completed her B.Tech from Vaagdevi College of Engineering and she is interested in the area of VLSI.

Author-2:

Mr. MADUPU SANJAY working as Asst. Professor in Vaagdevi College of Engineering, Bollikunta, Warangal with 5years of experience. He is interested in the area of VLSI.