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Design of a High Range Proposed Buffer for Level Shifter Operation

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Abstract: ***In this Paper, we propose a novel level shifter circuit Which was capable of converting sub threshold to above-threshold signal Voltage levels. In contrast to other existing implementations, it does not require a static current flow and can therefore offer considerable static power savings. The output current was mainted high using Current Mirror stage later we extend to Wilson Current Mirror Circuit. In order save static power savings we proposed a new level shifter buffer in this paper. The circuit has been optimized and simulated in a 180-nm process technology. These results are carried using Tanner EDA tool.***

Keywords: ***CMOS, Output Buffer, TSMC018.***

Introduction:

To increase the display resolution, the load capacitance of the buffer amplifier is also increased, while the settling time is reduced. As we know the inbuilt buffer amplifier produce the power dissipation at high level. To achieve the high resolution, low power dissipation and high driving capability column drivers are mostly used.The analysis of analog circuit is very difficult, when we design the column drivers especially for LCDs. In this case buffer amplifier plays an important role, because they deter-mine the speed, resolution, voltage swing, transient response and the power dissipation. The MOS transistor is the basic building block of integrated circuits. Scaling of the MOS transistor improves its size, cost and performance. Today's fabricated integrated circuits are many times faster and occupy much less area, like today's microprocessors that contain nearly one billion transistors on a single chip. The role of supply voltage is vital for controlling the power consumption and hence reducing the power dissipation. It is reducing for each new technology generation. Threshold voltage of the device must be reduced proportionally as supply voltage reduces to sustain the transistor's output performance. The reduction in threshold voltage increases the leakage current drastically with each new technology generation• . As the leakage current increases with a new technology generation, it will affect the overall logic circuit's power dissipation. Leakage current is the major problem in the deep submicron region, so we need a powerful leakage reduction technique to minimize the effect of threshold Voltage scaling. Scaling methods pay a significant role in reducing the power dissipation from one technology node to another node. There are various scaling methods used for VLSI circuits. Most common are voltage scaling.• , load scaling• , technology scaling. and transistor sizing (width scaling). The purpose of studying various scaling methods is to decide a suitable method for scaling while keeping power dissipation and propagation delay in mind. In this paper the work investigations are carried out on the above said four scaling methods for a CMOS buffer circuit.

Output Voltage swing / supply voltage:

Another way of obtaining more output power is to increase the voltage swing that can be safely handled at the drain of a device. With circuits that can handle peak voltages above the nominal CMOS supply voltage, higher voltage swings in combination with a higher supply voltage can be used, thereby significantly increasing the maximum output power There are three approaches that can be followed to handle voltages higher than the nominal supply voltage, while maintaining sufficient lifetime.

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Technological solutions use extra process steps and masks that deliver a high-voltage tolerant transistor at the cost of a more expensive process. Extended drain devices can be created in standard CMOS without the need for extra process steps but require special models and layout rules to be created. Circuit solutions on the other hand limit the voltages across all transistor terminals to such values that sufficient lifetime is ensured and can be used within a standard CMOS process.

Current Mirror Based Buffer Design

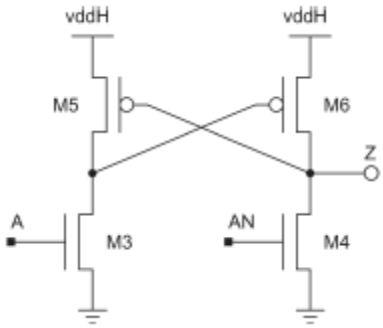

Fig1: Current Mirror Based Buffer Design

A conventional half-latch-based level shifter circuit is shown in Fig. 1. The low-voltage signals A and AN are connected to the gates of NMOS transistors M3 and M4, respectively. PMOS transistors M5 and M6 form a half-latch. On each input transition, either M3 or M4 must overcome the drive strength of the corresponding PMOS to make the half-latch switch. This is achieved by transistor sizing, i.e., making the NMOS transistors sufficiently wide. It is concluded in [1] that the required NMOS-to-PMOS ratio grows exponentially when the lower supply voltage scales down in the subthreshold region because the pull-down transistors only allow a subthreshold oncurrent while the pull-up half-latch has above-threshold drive strength.

Drawbacks:

For the 90-nm process technology used in this brief, an NMOS-to-PMOS ratio of ~2400 would be required to make the conventional level shifter circuit operate correctly at a supply voltage of 200 mV. Due to the resulting large width of the NMOS transistors, this circuit is not suitable for subthreshold to above-threshold level shifting.

Wilson Current Mirror Design

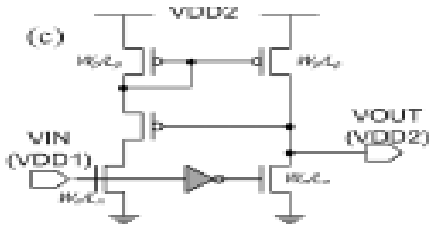

Fig2: Wilson Current Mirror Design

Wilson Current Mirror Design is CM-type LS that uses a Wilson current mirror. Which clamps the quiescent power consumption under a suprathreshold input.

Drawbacks:

WCM LS is problematic when its input and output levels are close. Because of a weak PUN, theWCM LS has a long rising delay, which is up to one hundred times longer than the falling delay (Fig. 2). This severe signal skew is not easily tolerated.

Proposed Buffer:

The Interface circuit proposed is shown in the figure. The Circuit Provides bidirectional voltage level conversion. Therefore, without any change in circuit configuration, the interface circuit can be used at both the driver and receiver ends of a low voltage swing circuit architecture to invert voltage levels from high to low and low to high.

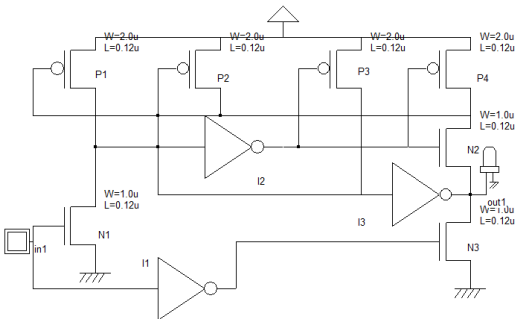

Fig3: Proposed Buffer Design

In that proposed interface circuit, P1is isolated from the input to minimize both the static power consumption and propagation delay. As the pull-up and pull-down networks are never simultaneously on, the proposed voltage interface circuit consumes no

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static power while driving high capacitive loads full swing (Vdd2) at high speed.

In this circuit, only I1 is supplied by Vdd1.The rest of the circuit (to the right of the demarcation line)is supplied by Vdd2. This circuit operates in the following manner with a 0 to 1transition at the input, node2is discharged through N1.P2 ensures that P1 is cut-off, and I2 ensures that P3 is cut-off during the output transition, so that the short circuit power consumption and output transition time are minimized. When node2 becomes sufficiently low, the output transitions high. With a 1to 0 transitions at the input, node 1 goes high. Node 4 is pulled down to the ground through N2 and N3 (N2 is on before the input signal changes). As node 4 is discharged to ground, P1 turns on, Charging node 2.when node 2 is sufficiently high, the output signal transition low. There is a negative feedback path from node 3 to node 4 to node 2 through I2,P4, and P1.P3 preserves the output stage after P1 is cut-off through the feedback path.

Results:

The circuits are simulated in Tanner Tools using TSMC018 Technology

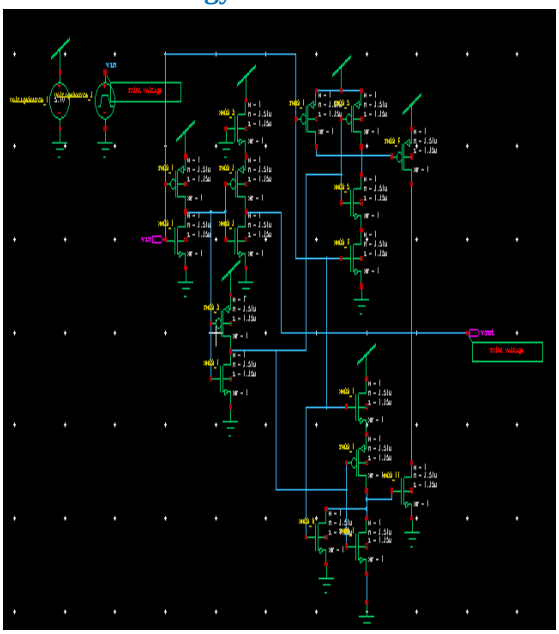

Fig4: Design of New CMOS Buffer

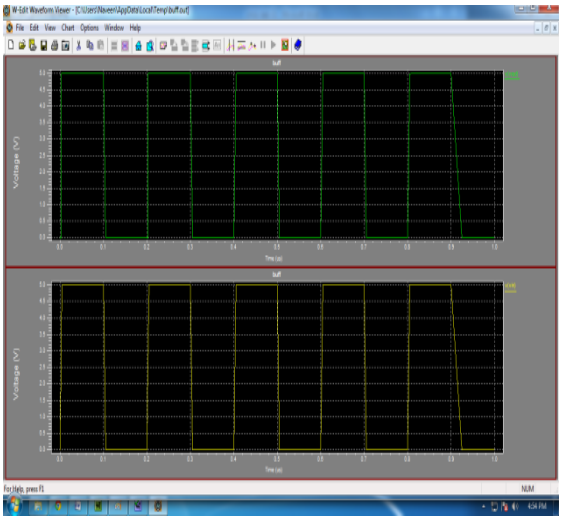

Fig5: Simulation of New CMOS Buffer

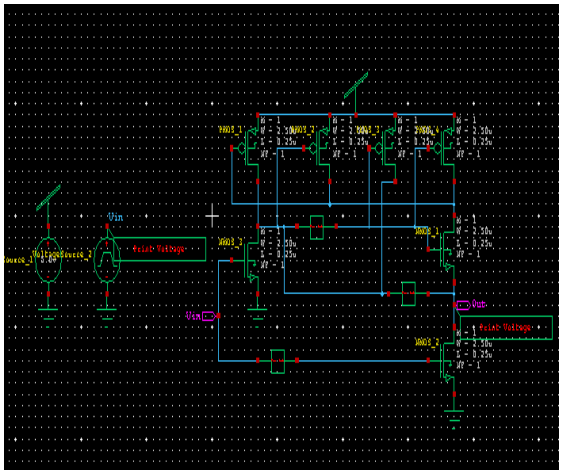

Fig6: Proposed CMOS Buffer Design

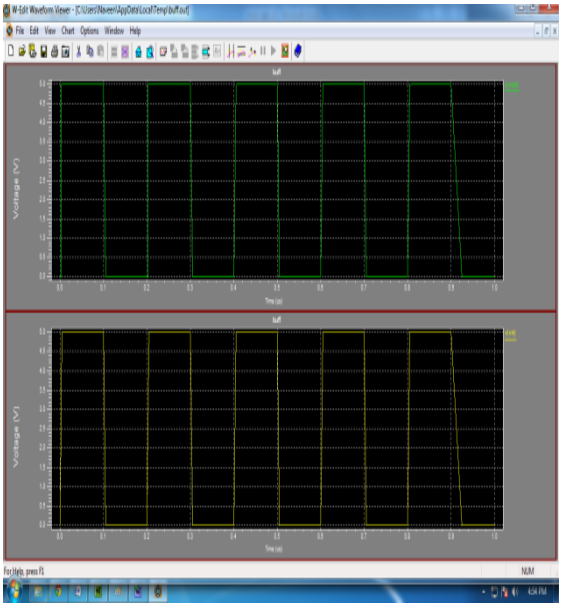

Fig7: Simulation of Proposed CMOS Buffer

Conclusion:

The new proposed buffer can operate at different voltage level is presented in paper. This circuit has much driving capability and less area consider the existing one and also power dissipation was also lower.

References:

[1] Y.Lin, Xuecheng Zou, Zhaoxiao Zheng, W. Huo, Xiaofei Chen and W.Kang, "High-speed, Low Switching Noise and Load Adaptive Output Bufler", in proceedings of the International Symposium on Integrated Circuits 2009, (ISCI 2009), Singapore, 14-16 Dec. 2009, pp. 280-282.

[2]R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS Circuit Design, Layout, and Simulation", New York: IEEE Press, 1997.

[3] T. Gabara, W. Fischer, J. Harrington, and W. Troutman, "Forming damped LRC parasitic circuits in simultaneously switched CMOS output buffers", IEEE con! Custom Integrated Circuits. pp. 277 -280. May 1996.

[4] L. Yang and 1. S. Yuan "Design of a new CMOS output buffer with low switching noise", in proceedings of the ICM 2003, Cairo, Egypt, 9-11 Dec. 2003, pp.131-134.

[5] F.Garcia, P. Coli, and D. Auvergne "Design of a slew rate controlled output bufler", in proceedings of the con] 1998, pp.147-150.

[6] K. Leung, "Controlled slew rate output buffer", in Proc. IEEE Custom Integrated Circuits Con!, 1988, pp. 5.5.1-5.5.4.

[7] C. W. Lu and L. C. Huang, "A 10-bit LCD column driver with piecewise linear digital-to-analog converters," IEEE J. Solid-State Circuits, vol. 43, pp. 371-378, February. 2008.

[8] C. W. Lu and K. Hsu, "A high-speed low-power rail-to-rail column driver for AMLCD application," IEEE J. of SolidState Circuits, vol. 39, pp. 1313-1320, Aug. 2004.

[9] Y. S. Son, 1. H. Kim, H. H. Cho, 1. P. Hong, 1. H. Na, D. S. Kim, D. K. Han, 1. C. Hong, Y. 1. Jeon, G. H. Cho, "A column driver with low-power area efficient push-pull bufler amplifiers for active-matrix LCDs," in proceedings of the ISSCC Dig. Tech. Papers, Feb. 2007, pp. 142-143.

[10] G. D. Cataldo, A. D. Grasso and S. Pennisi, "Two CMOS current feedback operational amplifiers," IEEE Trans. Circuits Syst. II, vol. 54 , pp. 944-948, Nov. 2007.

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