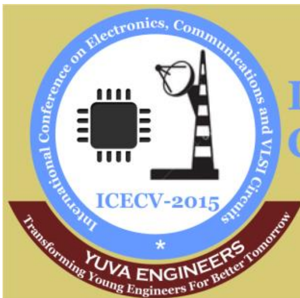
ISSN No: 2348-4845



International Conference on Electronics, Communications and VLSI Circuits (ICECV-2015)
July 10, 2015 - Hyderabad, India
Papers Published in IJMETMR, A Peer Reviewed Open Access International Journal.

A Novel 6T SRAM based design with integration of NBTI technique

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Abstract: ***Rapid advances in the field of very large scale system designs brought memory circuits are continuously regulated and in turn, more number of cells could made possible to integrate on small chip. However in Nano scale SRAM there is large variation of threshold voltage occurs. To slove Vt variation problem in SRAM in this paper we proposed the adiabatic SRAM cell and later we introduce a NBTI SRAM which effectively reduces the problem. This project was carried out using Tanner EDA Tools.***

Keywords: ***Adiabatic SRAM, NBTI, Tanner EDA.***

Introduction:

Today‟s mobile/multimedia applications, e.g., a combination of text, audio, still images, graphics (discrete media) and audio, animation, video, video on demand, video recording, interactivity content forms (continuous media), etc. need to be incorporated in one digital system. So, there is a strong need to reduce the standby current leakage while keeping the memory cell data unchanged [1]. In other words, it demands the processor with high processing power, high performance, and low-power on-chip memory. According to the ITRS-2003 (International Technology Roadmap), 90% of the chip-area will be occupied by the memory core by 2014.

Aggressive scaling of semiconductor dimensions with every technology generation has resulted in raised integration density and improved device performance. Leakage current will increase with the scaling of the device dimensions. Raised integration density at the side of raised outflow requirements ultralow-power operation was major one for operating a device. The ability demand for the battery-operated devices like cell phones and laptops is even additional tight. Reducing supply voltage reduces the dynamic power quadratic ally and leakage power linearly to the primary order. Hence, offer voltage scaling has remained the main focus of low power style.

On chip caches plays a important in speed of Processors in order to increase the speed majorly now we increases the frequency of operation which makes caches to operate more faster . To achieve higher reliability longer battery life we require low power caches.

The Problem Found in the existing SRAM designs are listed below:

- SRAMs are consuming most of the power of the core Processor Element.
- The leakage in the SRAM circuit is high when compared to the all other processor components.
- As its consuming much power heat dissipation also occurs
- So less efficient than all other elements.

The total effect of the supply voltage scaling along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write failure, and access-time failure

This shows the more demand for chips with high functionality and low-power consumption. It is important to focus on minimizing the leakage power of the SRAM structures [3]. The main source for dynamic power consumption is through the switching. But there are several sources for the leakage current, i.e., the sub-threshold current due to low threshold voltage, the gate leakage current due to very thin gate oxides, etc., [4]. The MOS transistor miniaturization also introduces many new challenges in Very Large Scale Integrated (VLSI) circuit designs, such as sensitivity to

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process variations and increasing transistor leakage. In Fig.1, the leakage power from a high-performance microprocessor has been shown. It increases steadily, as the technology is scaled down [5].

A high-performance VLSI chip also demands ever increasing on-die SRAM to meet the performance needs. This pushes the SRAM scaling towards a more concern domain in today‟s VLSI design applications. The SRAM cell stability is further degraded by supply voltage scaling. The SRAM leakage power has also become a more significant component of total chip power as a large portion of the total chip transistors directly comes from on-die SRAM. Since the activity factor of a large on-die SRAM is relatively low. So, it is recommended by the researchers in the field to be more effective to put it in a power reduction mechanism dynamically, which modulates the power supply along the memory addressable unit or bank and the need for active/standby mode of operation. In this work, a novel technique of full-supply body-biasing scheme is devised to meet it.

In this work we shows the conventional 6T SRAM design and show the implementation of a 5T SRAM Cell. In order to improve the read/write performance of the circuit we shows the Adiabtic SRAM Design with the Virtual Grounding Technique. So later we propsed aNBTI(Negative Bias Temperature Instability) SRAM to over come the threshold voltage problems generated by the PMOS.

II PREVIOUS WORKS

Conventional 6T SRAM design:

There are many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell design. The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only, we will see how these are carried out.

Read Operation: Before starting of the read operation, we should charge the bit lines to VDD. When the word line (WL) is enabled, the bit line which connected to the node of the cell containing ‘0’ is discharged through the NMOS transistor. By this we can know which node is containing’0’ and which is having ‘1’ in it. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing ‘1’ means it's connected to the node containing ‘1’ and vice versa.

Write Operation: For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar ($\overline{BL}$). When the word line (WL) is enabled the data is written into respective node.

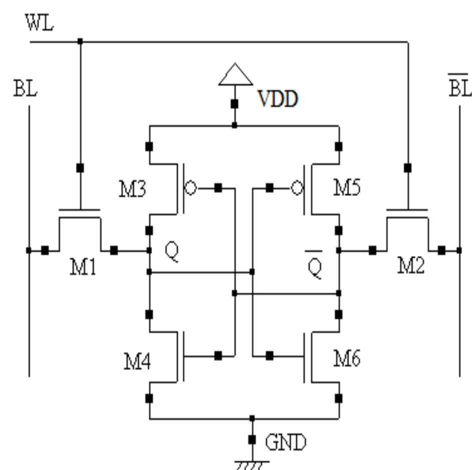

Fig.1 Conventional **6T SRAM**

But the conventional 6T SRAM have stability limitations at low supply voltages.

CONCEPT OF PROPOSED SRAM

A conventional 6T SRAM Cell uses a two bit line Precharge for the Read operation but in the proposed SRAM cell we introduce a single bit line SRAM redaing.The problem is that the low-voltage node of an FF increases from 0 V. In contrast, a single-BL SRAM uses only one BL for reading. When $V1$ = 1 and $V2$ = 0, $V2$ is not connected to the precharged BL; so it remains at a low level. Therefore, a single-BL SRAM has a larger SNM than one with two BLs.

To examine the effect of adiabatically charging, we assume that the capacitance of a BL is small and that the voltage of a BL decreases from the Precharge voltage to 0 because the initial conditions are $V1$ = 0 and $V2$ = 1.

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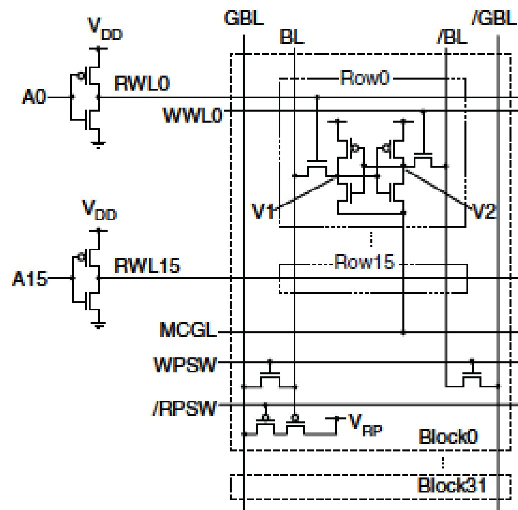

Fig2: Adiabatic SRAM Cell

Operation:

The proposed SRAM Cell consists of two bit line writing and Single bit line reading.

Write operation: During the write operation RWL0 and WWL0 are enable and WPSW are enabled so the both GBL and /GBL are Connected to the BL and /BL so the data was feed to the cell and voltages are represented at V1 and V2.

Read Operation: Read operation was done through the single bit line /RSPW depends upon the V1 voltage GBL was charged to Vrp voltage when 0 was read and 1 was read GBL was at 0 Voltage n threr is no need of charging of both bit lines like in 6T SRAM. The MCGL line will acts to disconnect the ground line when SRAm was not n operation. This also not over comes the NBTI problem of PMOS in SRAM

Negative bias temperature instability

When silicon is oxidized, most of the Si atoms at the surface of the wafer bond with oxygen while a few atoms bond with hydrogen. When a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor , the relatively weak Si-H bonds get disassociated, leading to the generation of interface traps at the Si/SiO interface. These interface traps cause the threshold voltage of the pMOS transistor to increase, which in turn degrades the speed of the device and the noise margin of the circuit, eventually causing the circuit to fail [10]. A detailed discussion on the physics of interface trap generation due to NBTI. (NBTI) is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.

This NBTI makes PMOS threshold voltage to increase. In order to reduce this NBTI problem of SRAM network here we introduces a recovery boosting technique. In recovery boosting technique SRAM operates in two modes of operation by switching CR line. One was normal mode which acts like normal SRAM network and another was recovery mode which makes PMOS to off and acts like a recovery transistor.

Here we apply recovery boosting technique to SRAM

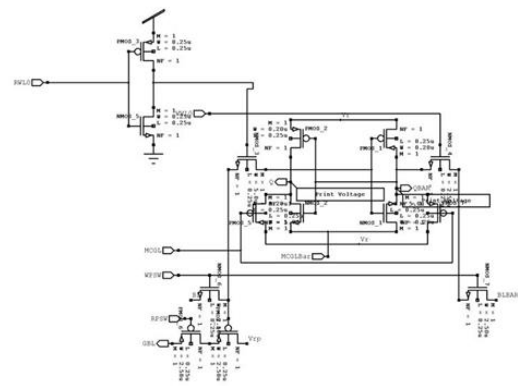

Fig: NBTI SRAM Cell

Conclusion:

In this technique we apply NBTI recovery technique which helps in th e Vt voltage change SRAM and their mo need of large Precharge of bit lines by providing single bitline reading operation .NBTI is one of the most important silicon reliability problems facing processor designers. SRAM memory cells are especially vulnerable to NBTI since the input to one of the pMOS devices in the cell is always at a logic "0." In this paper, we propose recovery boosting, a technique that allows both pMOS devices in the cell to

be put into the recovery mode by raising the ground voltage and the bitline to . We show how fine-grained recovery boosting can be used to design the physical register file and issue queue and evaluate their designs via SPICE-level simulations.

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