ISSN No: 2348-4845
International Conference on Electronics, Communications and VLSI Circuits (ICECV-2015)
July 10, 2015 - Hyderabad, India
Papers Published in IJMETMR, A Peer Reviewed Open Access International Journal.

Design of a Prescalar for Low Power Single Phase Clock Distribution

P.Ramya
PG Scholar
Department of ECE
Vaagdevi College of Engineering
Bollikunta, Warangal-506001

B.Vijay Kumar
Asst. Professor
Department of ECE
Vaagdevi College of Engineering
Bollikunta, Warangal-506001

P Prasad rao
Professor & HoD
Department of ECE
Vaagdevi College of Engineering
Bollikunta, Warangal-506001

1.Abstract

Frequency synthesizer is one of the important elements for wireless communication application. The speed of VCO and prescaler determines how fast the frequency synthesizer is. A dual modulus prescaler contains logic gates and flip-flops. This project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. The multiband divider consists of a proposed wideband multi modulus 64/65 prescaler and an improved bit-cell for swallow (S) counter and programmable(P) counter and can divide the frequencies. The low power wideband 2/3 prescaler and wideband multimodulus 32/33/47/48 prescaler which can consume power up to 162 mw at Maximum Frequency 522.371MHz. To overcome this we used a low power wideband 4/5 prescaler and wideband multimodulus 64/65 prescaler which can consume power up to 161 mw at Maximum Frequency 522.371MHz.

Frequency dividers are also called prescaler which are used in many communication applications like frequency synthesizer, timing-recovery circuits and clock generation circuits. A prescaler is loaded at the feedback path of the synthesizer, takes signal and generates a periodic output signal and frequency.

It is one of the most critical blocks in frequency synthesizer because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption. So low power wideband 4/5 prescaler and a wideband multimodulus 64/65 prescaler is used in this project.

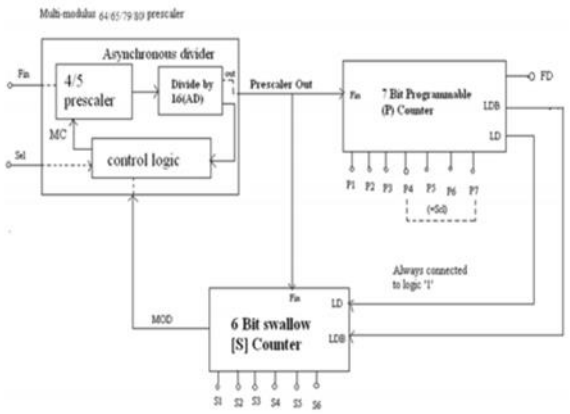

Fig .1. proposed dynamic logic multiband flexible Divider.

2. Design Considerations

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

f max = 1/tpLH+tpH L (1)

Where tpLH = low to high transition

tpHL = high to low transition

tpLH,tpHL are the propagation delays of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching. and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching}=\sum f_{CLK} C_{Li} V^2 dd \quad (2)$$

where n = number of switching nodes

fclk= clock frequency

CLi = load capacitance at the output node of the ith stage

Vdd = supply voltage

ISSN No: 2348-4845
International Conference on Electronics, Communications and VLSI Circuits (ICECV-2015)
July 10, 2015 - Hyderabad, India
Papers Published in IJMETMR, A Peer Reviewed Open Access International Journal.

Normally the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$Psc=T_{SC}*Vdd$ (3)

Where Tsc is the short-circuit current.

The analysis in E-TSPC shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that ofE-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.1/1 CMOS process.

3.Wideband 4/5 Prescaler

The wideband single-phase clock 4/5 prescaler is used in this design and it consists of 3 D-flip-flops and 2 NOR gates as shown below

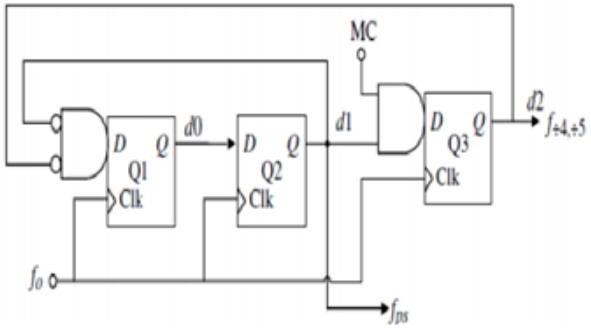

Fig.2 wideband single phase clock 4/5 prescaler

It depends on the logic value at MC. When MC = 0 the division ratio is 4 MC = 1 the division ratio is 5 A modulus control signal M is used to control the division ratio either N or N+1. When M = '0', D1 and D2 will form a divide-by-4 with q3 remaining at 'high' and NAND1 behaving like a NOT gate. When M = '1', NAND2 will behave like a NOT gate and NAND1 will output '0' when both q2 and q3 are at 'High'. Hence q1 will change from high-t0- low after 3 cycles of fclk, forming a divide-by-5.

4.Multimodulus 32/33/47/48 Or 64/65 Prescaler

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47 and 48 or 64, 65,78 and 79 is shown in Fig. 3. It is similar to the 32/33 or 64/65 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48 or divide-by-78 and divide-by-79) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

The multimodulus prescaler consists of the wideband 2/3 (N1/(N1+1)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios

Beside the usual MOD signal for controlling N/(N+l) divisions, the additional control signal sel is used to switch the prescaler between 32/33and 47/48 modes.

1) Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation.

The division ratio N performed by the multi modulus prescaler is

$$N = (AD*N1) + (0*(N1+ 1)) = 32$$

Where N1=2 and AD=16 is fixed for the entire design. If MOD = 0 , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is

$$N+l = ((AD - l)*N1) + (1 * (N1 +1)) = 33$$

ISSN No: 2348-4845
International Conference on Electronics, Communications and VLSI Circuits (ICECV-2015)
July 10, 2015 - Hyderabad, India
Papers Published in IJMETMR, A Peer Reviewed Open Access International Journal.

2) Case 2: sel =' l'

When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates in divide-by- 3 mode and when MC=0, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when sel='0' If MOD=1, the division ratio N+ 1 performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

N + l = (AD * (N1+1)) + (0 * Nl) = 48

If MOD=1, the division ratio N performed by the multimodulus prescaler is

N = ((AD - l) * (N1 + 1)) + (1 * Nl) = 47.

In order to get 64/65/78/79 clock cycles we need to operate 4/5 prescaler by making the control signal sel of second MUX to „1".To get 32/33/47/48 prescaler, the second MUX should be equal to "0" means the control signal sel of the second MUX should be equal to 0and to get 64/65 prescaler, the second MUX should be equal to "1" means the control signal sel of the second MUX should be equal to "l". sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 4/5 prescaler and the multimodulus prescaler operates as the normal 64/65 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 4/5 prescaler operates in the divide-by-2 mode and when MC = 0, the 4/5 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multi modulus prescaler is

N = (AD*N1) + (0*(N1+ 1)) = 64

Where N1=2 and AD=16 is fixed for the entire design. If MOD = 0 , for 62 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is

N+l = ((AD - l)*N1) + (1 * (N1 +1)) = 65

5.Multiband Flexible Divider

The single-phase clock multiband flexible divider which is shown in Fig.1 consists of the multi modulus 64/65 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal MODE decides whether the divider is operating in lower frequency band or higher band.

A. Swallow (S) Counter:

The 6 bit s counter shown in fig.5 consist of six asynchronous loadable bit cells, a NOR embedded DFF and additional logic gates. If MOD is logically high nodes s1 and s2 switches to logic 0 and the bit cell does not perform any function. The MOD signal goes logically high only when the s-counter finishes counting down to zero.

In the initial state, MOD=0, multimodulus prescaler selects the divide by (N) mode and p, S counter start down counting the input clock cycles. When the s counter finishes counting, MOD switches to logic 1 and the prescaler changes to divide by N+1 mode for the remaining clock cycles.

B. Programmable (P) Counter:

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and

ISSN No: 2348-4845
International Conference on Electronics, Communications and VLSI Circuits (ICECV-2015)
July 10, 2015 - Hyderabad, India
Papers Published in IJMETMR, A Peer Reviewed Open Access International Journal.

thus a fixed division ratio is achieved. If a fixed 64 (N) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus 64/65 prescaler eases the design complexity of the P-counter.

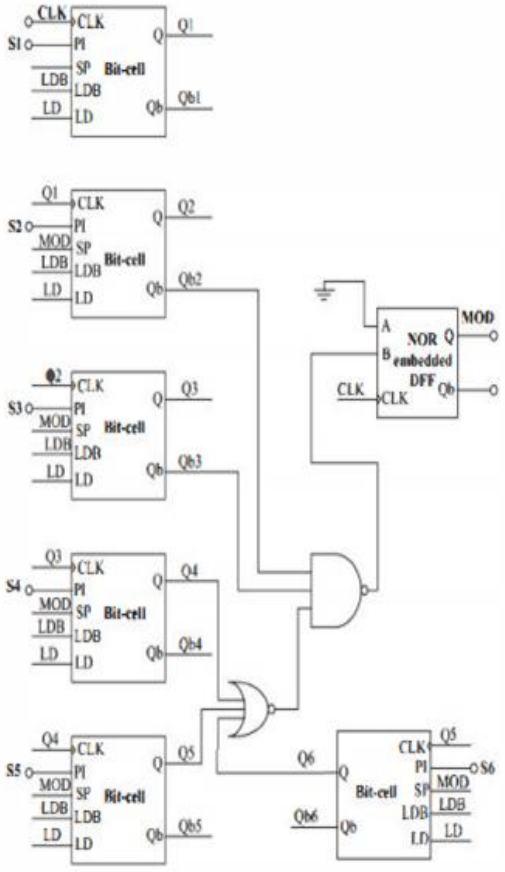

Fig 3Asynchronous 6 bit S-counter

6.Results And Conclusion Simulated Environment

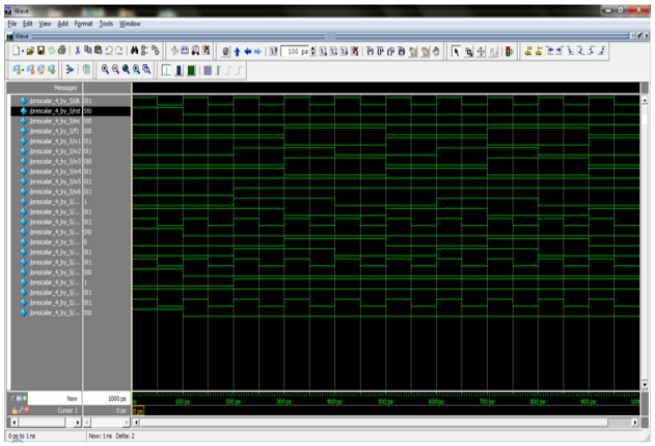

Fig 4 Output of Divided by 4

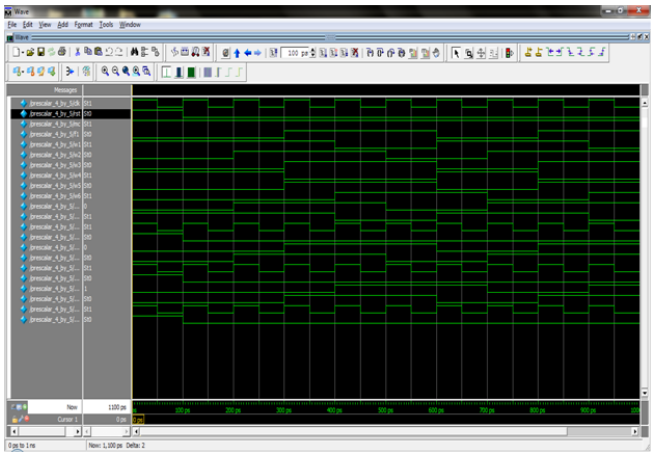

Fig 5 Output of Divided by 5

	Total	Dynamic	Quiescent
Power Supply(W)	0.162	0.003	0.159

Fig.6. Power consumption of 4/5 Prescaler

	Total	Dynamic	Quiescent
Power Supply(W)	0.161	0.002	0.158

Fig.7. Power consumption of 4/5 Prescaler

7. Conclusion

In this paper, a multiband flexible divider is implemented which consist of a consist of program counter; swallow s counter and multimodulus prescaler. It is simulated by using modalism .This type of divider is widely used in Bluetooth, Zigbee technologies which are the common wireless standards . Also in the modified flexible divider existing 2/3 prescaler is replaced with modified 4/5 prescaler. By the implementation of modified divider we can achieve reduced power consumption.

AUTHOR 1:-

P.Ramya completed her B tech in Kakatiya Institute of Technolgy & Sciences, warangal and pursuing M-Tech Vaagdevi College of Engineering

AUTHOR 2:-

Mr. B.Vijay Kumar is working as Asst. prof in Dept of ECE Vaagdevi College of Engineering.

AUTHOR 3:

Mr. P.Prasad Rao, Head of the Department of Electronic & Communication Engineering Vaagdevi College of Engineering.