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A High Performance Double tail Comparator design using Inverter Stage

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Abstract: ***Comparator was the basic building block of Analog to Digital Comparator. In this paper we propose a new CMOS dynamic comparator using dual input single output differential amplifier as lat ch stage suitable for high speed analog-to-digital converters with High Speed, low power dissipation and immune to noise than the previous reported work is proposed. Back to-back in verter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The simulation results will be shown in the W-Edit, average power consumption is in T-spice.***

Keywords **–** ***CMOS comparator, low power, High Speed, Analog-to-Digital Converter and Tanner EDA.***

Introduction

Comparator is one of the fundamental building blocks in most analog – to –digital converter. Designing high-speed comparators is more challenging when the supply voltage is smaller. In other words to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Developing a new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low voltage operation, especially if they do not increase the circuit complexity. Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low voltage operation.0.18µm CMOS technology used in tanner software for simulation.C18 process ensuring very low defect densities and high yields.0.18µm CMOS technology offers RF integration, analog mixed signal, digital design flows and high density system on chip capability. The proposed comparator of works down to a supply voltage of 0.8V with a maximum clock frequency consumes 12 µW .Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double tail comparator is based on designing a separate input and cross coupled stage. Based on the double tail structure proposed a new dynamic comparator is presented which does not require stacking of too many transistors. By adding a few minimum size transistors to the proposed comparator. Latch delay time and mismatch also reduced. This modification also results in considerable power saving compared to conventional dynamic comparator and double tail comparator. In many applications comparator speed, power dissipation and number of transistors are more important.

Greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less hysteresis , less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem,

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dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The main problem with all these dynamic comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals. In this paper we have designed all type of comparators.

Dynamic Vs. Static Logic

Static Logic always has a path from power or ground to the output
– Stable over long periods
– Simple clocking schemes
• Dynamic Logic relies on capacitance of gates or other structures to hold state
– Can be faster than static logic
– Has minimum operating frequency
– More restrictions about how/when inputs can change
• Consequence of how we implement dynamic logic

Dynamic Logic Concepts

• All dynamic logic we'll look at is clocked
• In one phase of the clock, we'll precharge the gate to either 0 or 1.
• In another phase, we'll evaluate whether the gate's output should stay at the precharged value or change.

In this Dynamic comparator designs there will be two phases one was Reset phase when Clk=0 and then Latch Phase when Clk=1.

Need of this work:

Traditional operational amplifier designs most commonly use transistors in the saturation region, which generally requires at least one DC bias current. As technology size has decreased, low power, high gain amplifier design has become more challenging for designers. Since transistor threshold voltage generally doesn't decrease as fast as feature size and power supply voltage, many cascaded or folded designs are not possible with reduced voltage supply. Given that the reduction in headroom reduces the ability to cascode devices, low voltage high-gain amplifiers are commonly built by expanding outward, using two or even three cascaded amplification stages. These multi-stage cascaded designs require the designer to take extra measures to ensure amplifier stability, and, depending on the topology, can be very challenging or complex to stabilize. Most stabilization schemes require additional compensation capacitors and/or nulling resistors, which use additional silicon area, and can decrease circuit bandwidth; however, these compensation.

Reduced power supply voltage and the increasing demand for low power consumption make sub-threshold operation and design a more viable alternative when a reduction in bandwidth is acceptable. Operation in the sub-threshold region causes the drain current to increase exponentially with VGS as opposed to quadratically in the saturation region [14]. The disadvantage with sub-threshold operation is the reduction in amplifier driving current, and the loss of ability to quickly drive large capacitive loads.

In this paper, an inverter-based operational amplifier topology and operation and design principles are discussed and evaluated. We use two previously used figures of merit to objectively compare various aspects of the different circuit topologies. We conclude that the inverter-based differential amplifier topology with current starving provides one of best circuit topologies for energy efficiency

Design Process of this Work

A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed During the RESET PHASE, when Clk is LOW (Clk =0), transistor NMOS_5 is in off state and pmos transistors PMOS_3, PMOS_6, PMOS_7, are in on state. Transistors NMOS_1 and NMOS_2 are in cutoff mode. Switch transistors PMOS_3, PMOS_9, PMOS_4, and PMOS_10 will charge the drains of transistors NMOS_ 1 and NMOS_2 and the output nodes Outp and Outn towards Vdd. During the

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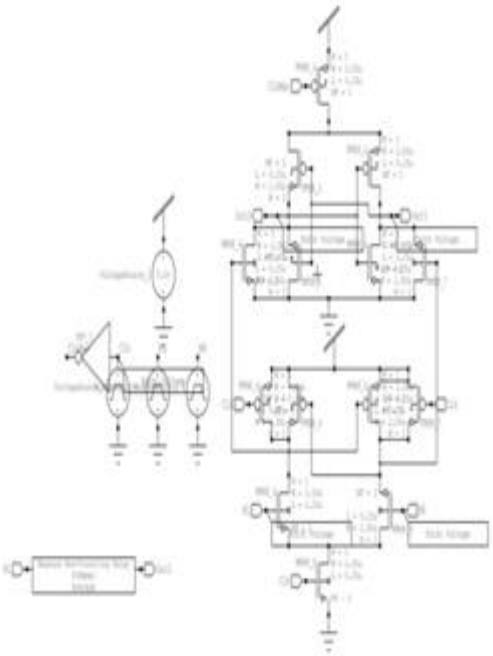
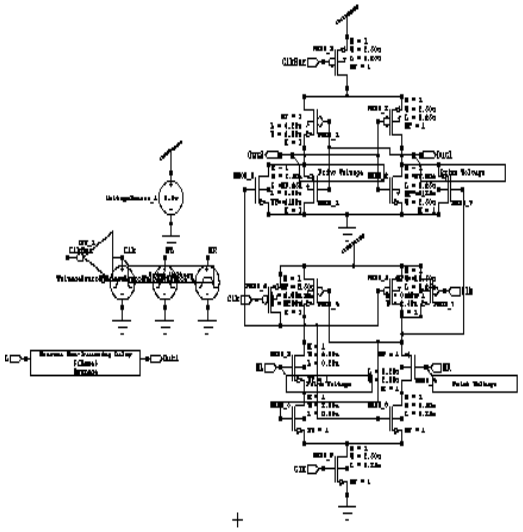
REGENERATION PHASE, when Clk is HIGH (Clk =1).

The process starts by turning the transistor NMOS_3 on and immediately an current 'I' starts to flow and the drain of transistor NMOS_3 starts to discharge towards ground (Gnd).In this succession the differential input transistors NMOS_3 and NMOS_4 are turned on. The currents of transistors NMOS_1 and NMOS_2, (at the drain terminal) will start to pull the output nodes Outp and Outn towards Gnd. Due to the difference of voltages between the input signals, the current at the drain terminals of transistors NMOS_ 3 and NMOS_4 will be different. Now in the regeneration mode the output node are discharging towards Gnd and pmos transistors PMOS_1 and PMOS_2 will come in saturation mode as the voltage at output nodes falls below The design is simulated using 0.25µm CMOS Technology using Tanner EDA Tools. Proposed design exhibits reduced delay and high speed with a 5.0 V supply. This design can be used where high speed and low propagation delay are the main parameters schemes have been improving with the usage of active compensation networks.

Proposed Dynamic Comparator



Main Idea



Final structure

The proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between Clk and Clkb over a wide common mode and supply voltage range. The overall area is small even though number of transistors is more. It is because of widths of transistors are optimized without compromising the speed and performance of the comparator.

For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistor PMOS_6 and PMOS_7 are turned on and they charge Di nodes' capacitance to VDD, which turn both NMOS transistor NMOS_1 and NMOS_2 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor PMOS_1, PMOS_2, PMOS_6 and PMOS_7 are turned on and they make Out nodes and SW nodes to be charged to VDD while both NMOS transistors NMOS_4 and NMOS_3 are being off. During the evaluation (decision-making) phase (Clk=VDD), each Di node capacitance is discharged from VDD to ground in a different time rate proportionally to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between Di+ and Di- node. Once either Di+ or Di- node voltage drops down below around VDD−|Vtp|, the additional inverter pairs PMOS_1/ NMOS_1and PMOS_2/

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NMOS_2 invert each Di node signal into the regenerated Di' node signal. Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch. The additional Feed back transistors NMOS_% and NMOS_6 which used for reduceding the static loss effect which was suffered by the before comparator design.

Subthreshold

Subthreshold conduction or subthreshold leakage or subthreshold drain current is the current between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The terminology for various degrees of inversion is described in Tsividis.

In digital circuits, subthreshold conduction is generally viewed as a parasitic *leakage* in a state that would ideally have no current. In micro power analog circuits, on the other hand, weak inversion is an efficient operating region, and subthreshold is a useful transistor mode around which circuit functions are designed.

In the past, the subthreshold conduction of transistors has usually been very small in the *off* state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, subthreshold conduction has become a bigger factor. Indeed, leakage from all sources has increased: for a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption.

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. The amount of subthreshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device *off*, and as subthreshold conduction varies exponentially with gate voltage (see MOSFET: Cut-off Mode), it becomes more and more significant as MOSFETs shrink in size.

Subthreshold conduction is only one component of leakage: other leakage components that can be roughly equal in size depending on the device design are gate-oxide leakage and junction leakage.[5] Understanding sources of leakage and solutions to tackle the impact of leakage will be a requirement for most circuit and system designers.

To reduce the sub threshold effect here we uses the stacking scheme an design of inverter based amplifier was proposed

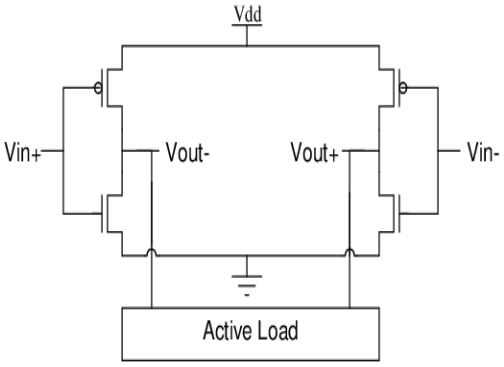

Fig: Inverter Based amplifier Design.

The inverter-based amplifier topology shown in Figure 1 uses CMOS inverters as the amplifier input. This input stage design has the advantage of combining the transconductance of the n and p transistors.

This combination of the two transconductances should provide 6dB increase in gain over a traditional common source amplification stage, with approximately the same DC bias current. When this architecture is implemented with a standard supply voltage (>2vt), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter. High current through the inverter allows significantly high bandwidths to be achieved. Another advantage of this topology is an increase in output

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swing and linearity when compared to a traditional common source or cascode amplifier if the respective transconductances of the p and n type transistors are approximately equal in magnitude. For noise, the inverter-based topology offers lower equivalent noise resistance compared to the equivalent common source topology.

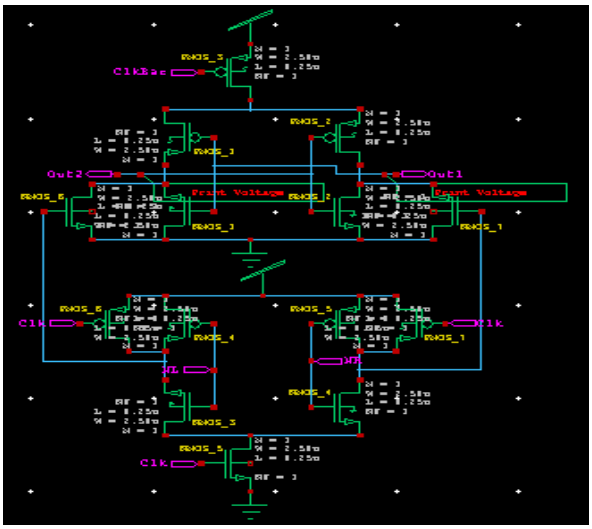

Fig: Inverter based amplifier design with reduced Sub threshold.

Conclusion:

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventionaldouble-tail dynamic comparators were analyzed. Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator and pre amplifier based clocked comparator. For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation than the other two comparators. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in TSNC025 CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator

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