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Reducing Number of Switches Using a Nine Level Cascaded H-Bridge Multilevel Inverter

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Abstract:
The multilevel inverter utilization have been increased since the last decade. These new type of inverters are suitable in various high voltage & high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. Multilevel inverters are the best solution for medium and high voltage power electronic drives. Because of its unique characteristic of synthesizing sinusoidal voltage with less harmonic contents using several DC sources. In a three phase multilevel inverter, each phase of a cascaded H-bridge inverter requires 'n' DC sources to obtain 2n + 1 output voltage levels. One particular disadvantage is that, it increases number of power semiconductor switches.

To overcome this disadvantage a multilevel DC link inverter (MLDCLI) with reduced number of switches and batteries is analyzed and implemented in this paper. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality. Compared with the existing type of cascaded H-bridge multilevel inverter, the MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases.

Keywords:
Cascaded H-bridge multilevel inverter (CHB), DC link, MLDCL, Multilevel inverter.

Introduction:
Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns, low switching losses, and high-voltage capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies.

These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. In this paper we implement a nine level cascaded H-bridge multilevel inverter based on an MLDCL and a bridge inverter. Compared with the existing cascaded multilevel inverters, the cascaded MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases.

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Cascaded H-Bridge Mldcl Inverter Topology:

Figure.1 shows a block diagram of the presented cascaded H-bridge MLDCL inverter topology, which consists of a multilevel DC source to produce DC-link bus voltage Vbus and a single-phase full-bridge (SPFB) inverter consists of four switches S1-S4 to alternate polarity of DC-link bus voltage to produce an AC voltage. The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches Sak and Sbk. The two switches and operate in a toggle fashion. The cell source is bypassed with Sak on and Sbk off, or adds to the dc-link voltage by reversing the switches. Figure.2 shows a circuit diagram of the presented cascaded H-bridge MLDCL inverter topology.

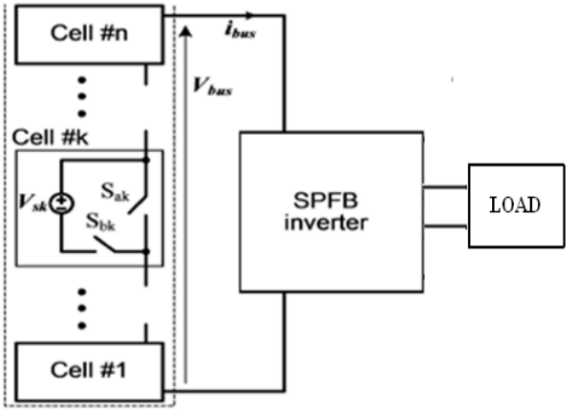

Figure 1 Block diagram of Cascaded H-bridge MLDCL inverter

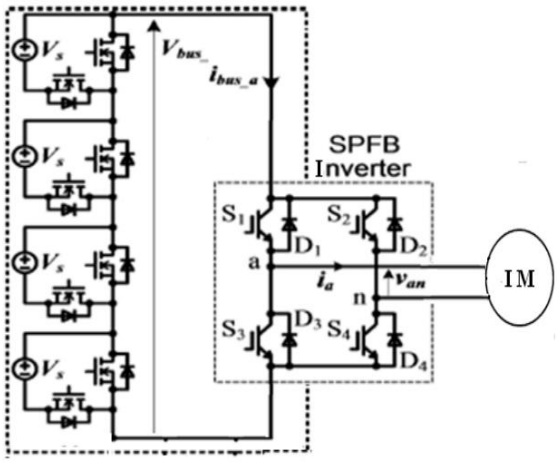

Figure 2 Circuit diagram of Cascaded H-bridge MLDCL inverter

The circuit diagram of the cascaded H-bridge multilevel DC-link inverter topology shown in Figure 2 consists of multilevel DC-link voltage source and single phase full bridge inverter.

A. Multilevel DC-link voltage source:

Multilevel DC-link voltage source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two MOSFET switches as shown in the Figure 3. The two MOSFET switches will operate in a toggle fashion. Low on resistance and fast switching capability, low voltage MOSFETS are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. The MOSFET switches are triggered by proper switching signals to produce multi level DC-link bus voltage which is indicated by Vbus in the circuit diagram.

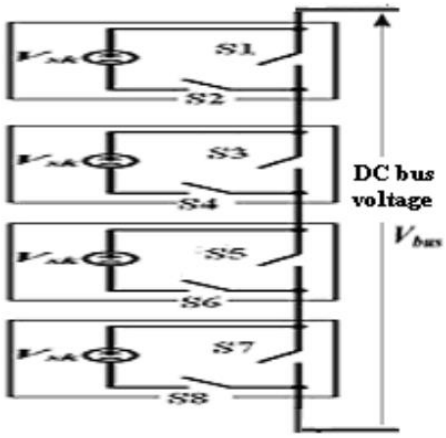

Figure 3 Multilevel DC-link voltage source

Various modes of switching sequence is given in the table 1 to produce DC bus voltage V_{bus} with the shape of stair case with (n=4) steps, where n is the number of cell sources that is given to the SPFB inverter.Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 4.

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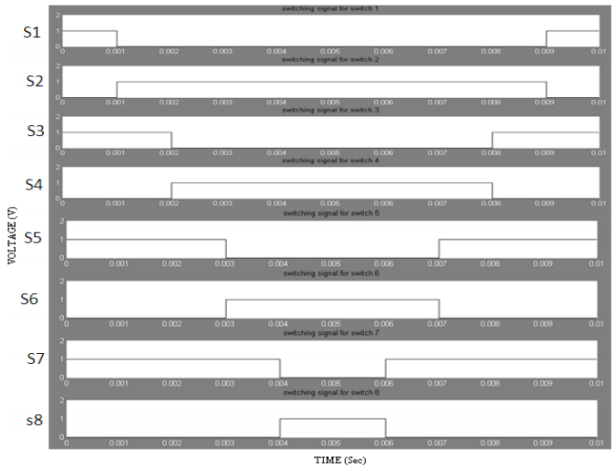

Figure 4 Switching pulses for switches in four H-bridge cells

By giving the switching pulses shown in figure 4 to the switches in four H-bridge cells the MLDCL voltage source produces DC bus voltage V_{bus} with the shape of stair case with (n=4) steps that approximates the rectified waveform of the commanded sinusoidal voltage, where n is the number of cell sources that is given to the SPFB inverter. The desired DC bus voltage V_{bus} is shown in the Figure 5.The switches in four cells will operate at twice of the fundamental frequency of the output voltage.

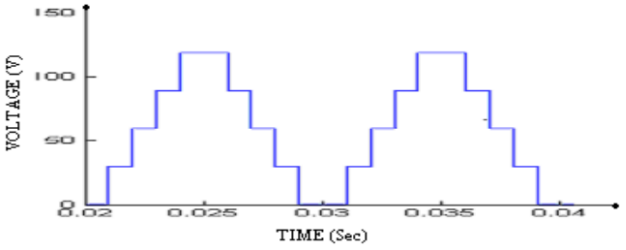

Figure 5 Desired DC bus voltage V_{bus} of cascaded H-bridge MLDCLI

B. Single phase full bridge inverter:

The single phase full bridge (SPFB) inverter shown in Figure 6(a) consists of four IGBT switches S1-S4 which can switch at faster rates and have less demanding gate drive requirements compared to the GTOs in two level inverters.

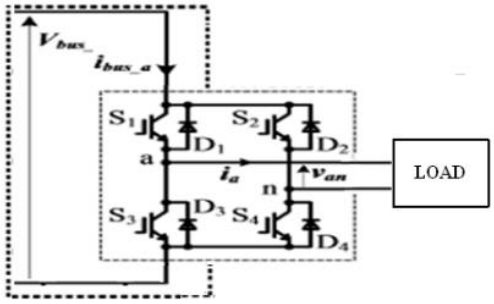

Figure 6(a) Block diagram of SPFB inverter

The switches S1-S4 always work in pairs such that S1&S4 triggered for positive half cycle and S2&S3 will trigger with some delay to produce negative half cycle by operating the switches at the fundamental frequency of the output voltage. The switching sequence for producing multilevel AC output voltage is shown in Figure 6(a).

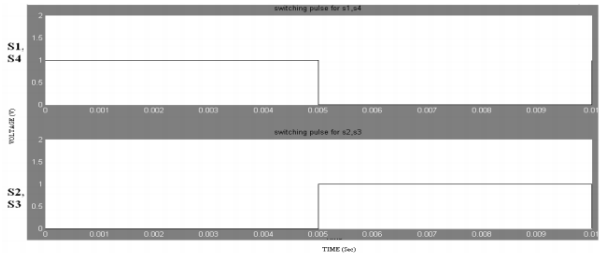

Figure 6(b) Switching signals of SPFB inverter

The principle of operation of nine level cascaded multilevel DC-link inverter is explained by explaining the operating principles of multilevel DC link voltage source and single phase full bridge inverter . To produce nine level AC output voltage V_{an} the multilevel DC-link source is formed by connecting four H-bridge cells in series with each cell having a separate voltage source controlled by two switches S_{ak} and S_{bk} which will operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the DC link bus voltage by reversing the switches. The DC bus voltage V_{bus} is fed to the SPFB inverter. The switching signals shown in Figure 6(b) are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage V_{bus} for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels, whose

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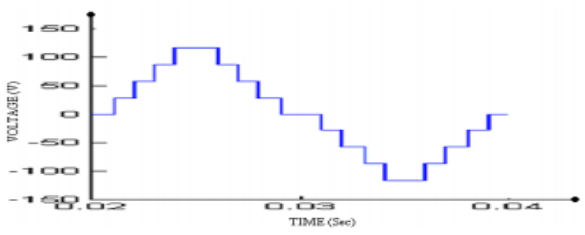

Figure 6(c) Desired AC output voltage V_{an} of cascaded H-bridge MLDCLI

RESULTS

A detailed circuit simulation was conducted to verify the operating principles of the proposed MLDCL inverters.

A. Nine level cascaded H-Bridge MLDCL Inverter with R load

A single-phase 9-level cascaded H-bridge MLDCL inverter was first studied for powering a resistive load, as shown in Figure 7. The load resistance is 30Ω and the voltage of each DC source is set at 30 V for an output frequency of 50 Hz.

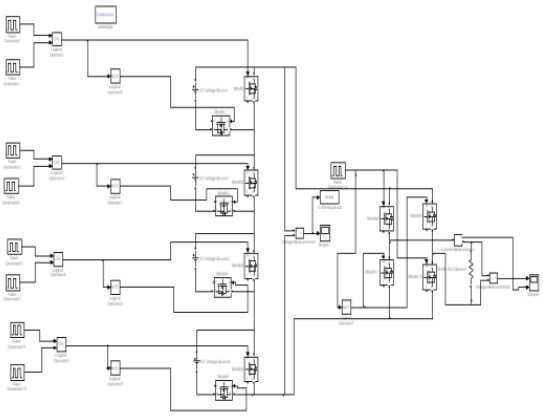

Figure 7 Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with resistive load

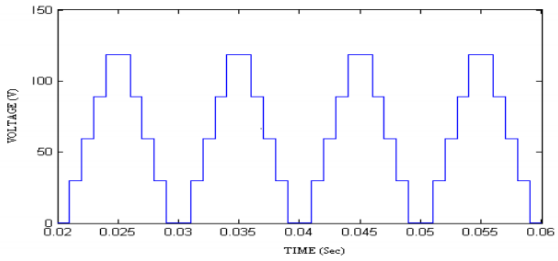

Figure 7 (a) Simulated DC bus voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

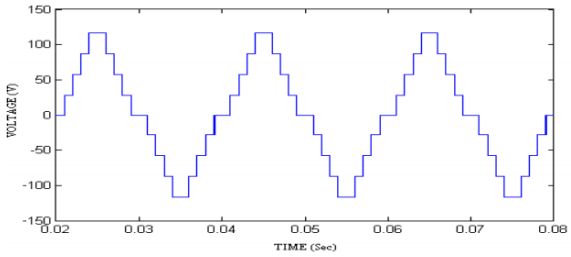

Figure 7 (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

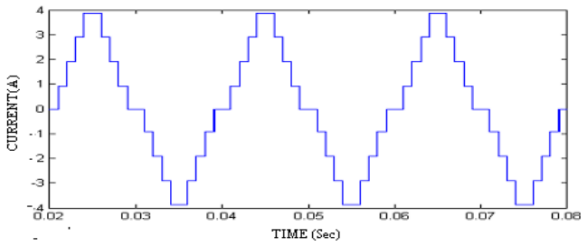

Figure 7 (c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

B. Nine level cascaded H-Bridge MLDCL Inverter with RL load

A single-phase 9-level cascaded H-bridge MLDCL inverter was studied for powering an inductive resistor load, as shown in Figure 8. The load resistance and inductance are 30 Ω and 90 mH and 150 mH. The voltage of each DC source is set at 25 V for an output frequency of 50Hz. The simulated DC bus voltage $V_{bus,}$ AC output voltage of the inverter $V_{an}$and AC output current i_{an} are shown in Figures 8(a), 8(b) and 8(c) respectively. These waveforms confirm the principle of operation of 9-level cascaded H-bridge MLDCL inverter described in section II-C with an inductive resistor load.

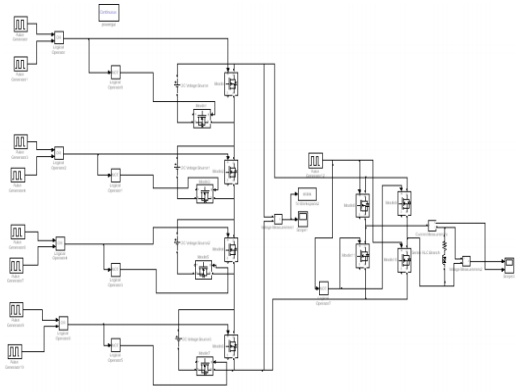

Figure 8 Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

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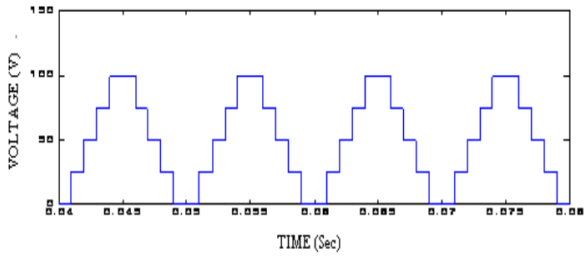

Figure 8 (a) Simulated DC bus voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

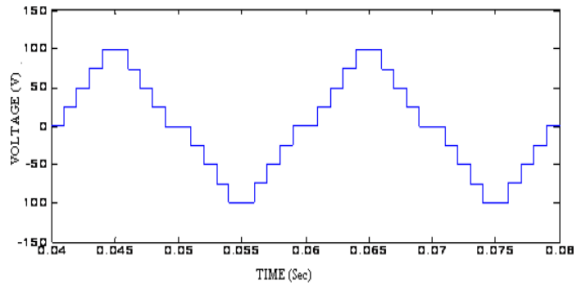

Figure 8 (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

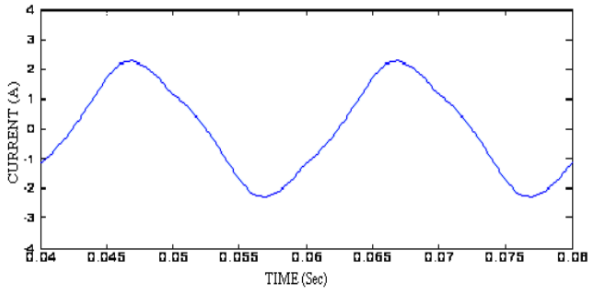

Figure 8(c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

The output voltage and current are in phase with each other for resistive load but there exists a phase lag between output voltage and current for an inductive resistor load due to presence of inductance in the load. The phase lag increases with the increase in inductance value. The simulated AC output current waveform with increased load inductance is shown in Figure 8(d).

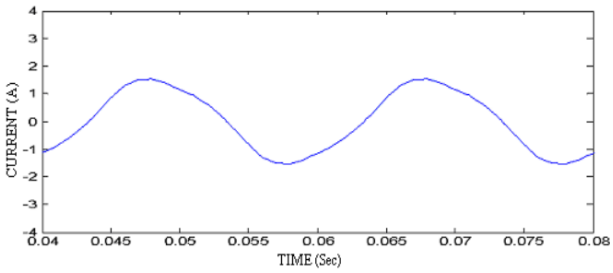

Figure 8(d) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load with increased load inductance.

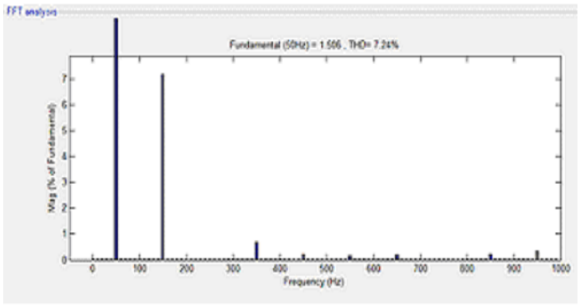

Figure 9 FFT analysis of output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

C. Nine level cascaded H-Bridge MLDCL Inverter with induction motor load

A single-phase 9-level cascaded H-bridge MLDCL inverter was studied for powering an induction motor load, as shown in Figure 10. The rating of the motor is power 1HP, voltage 230V. Main winding resistance and inductance are 2.02 Ω and 0.0074 H and auxiliary winding resistance and inductance are7.14 Ω and 0.0085 H. The voltage of each DC source is set at 80 V to get 220 V rms voltage required for motor to run for an output frequency of 50 Hz. The simulated AC output voltage of the inverter V_{an} and AC output current i_{an} are shown in Figures 10(a)and 10(b) respectively. These waveforms confirm the principle of operation of 9-level cascaded H-bridge MLDCL inverter described in section II-C with an induction motor load.

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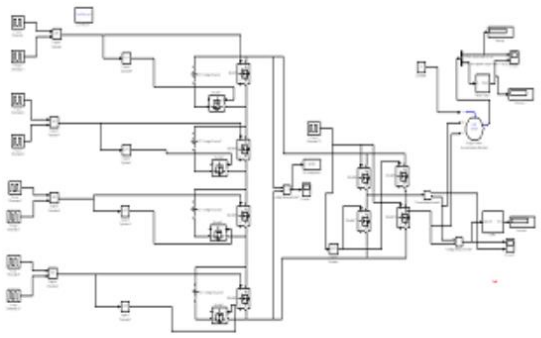

Figure 10 Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

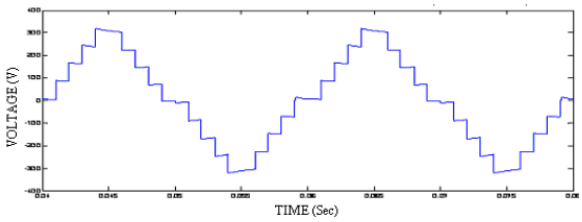

Figure 10 (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

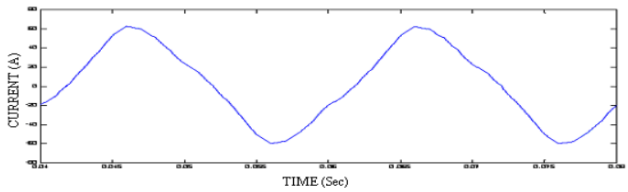

Figure 10 (c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load.

The line spectrum for the output current waveform is taken to determine the Total Harmonic Distortion present in the waveform. The Figure 11 shows the Total Harmonic Distortion is 10.77% for the output current of nine level cascaded H-Bridge MLDCL Inverter with induction motor load.

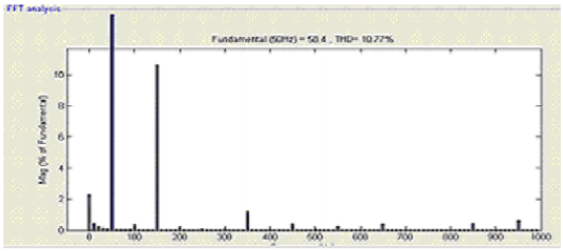

Figure 11 FFT analysis of output current waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

D. Comparison of the nine level cascade MLDCL Inverter and the existing MLI

From the previous discussions, it is demonstrated that the MLDCL inverters can significantly reduce the component count. Fig. 12 plots a chart for comparison of the required number of switches between the proposed MLDCL inverter and the cascaded H-bridge counterpart. As the number of voltage levels m grows, the number of active switches required is 2*(m-1) =16 for existing cascaded multilevel inverter and m+3 =12 switches are required for cascaded H-bridge MLDCL inverter.

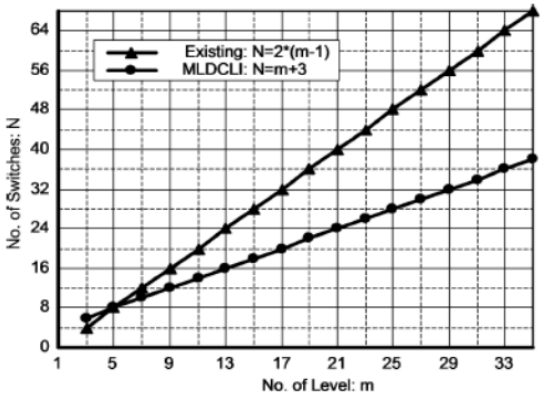

Figure. 12. Comparison of required number of switches.

CONCLUSION:

The presented nine level cascaded H-bridge MLDCL inverters can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume. One application area in the low-power range (• 100 kW) for the MLDCL inverters is in permanent-magnet (PM) motor drives employing a PM motor of very low inductance. The MLDCL inverter can utilize the fast-switching low-cost low-voltage MOSFETs in the half-bridge cells, and the IGBT's in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from

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the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photovoltaic cells.

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