ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Low Power Transmission Gate Full Adder in 22nm for Extended Region of Operation

L.V.Santosh Kumar Y
Assistant Professor,
Department of ECE,
Raghu Engineering College,
Visakhapatnam, A.P, India.

A.Gowthami
B.Tech (Pursuing),
Department of ECE,
Raghu Engineering College,
Visakhapatnam, A.P, India.

P.Varalaksmi
B.Tech (Pursuing),
Department of ECE,
Raghu Engineering College,
Visakhapatnam, A.P, India.

Ch.S.S.A.V.Ram
B.Tech (Pursuing),
Department of ECE,
Raghu Engineering College,
Visakhapatnam, A.P, India.

D.S.C.Dora
B.Tech (Pursuing),
Department of ECE,
Raghu Engineering College,
Visakhapatnam, A.P, India.

ABSTRACT:

Our main objective in this work is to design of full adder with low power, high speed for extended frequency ranges. In previous proposed full adder circuits with good power delay product are designed and verified for the extended frequency operations. Power delay product values are obtained. In this work, we design EX-OR/EX-NOR Nodes to operate with low power delay, low operating voltage with full voltage swing. From this EX-OR/EX-NOR a better optimized circuit is designed using transmission gate logic which operates at low power. The proposed circuit shows the best optimized results compared to previous works even in small scaling technologies we design and analyse the circuits in 22nm scaling technology, it is stimulated using Tanner tools V.13. The power and delay results are calculated using H-SPICE tool.

Key words:

Single gate, double gate, Transmission gate, power delay product.

I.INTRODUCTION:

To reduce the size of chip, the complexity in the circuits has increased drastically, because of that the power dissipation and performance of the circuit are being affected. So, there is concern towards circuits design in low power VLSI design to reduce the chip area and power dissipation. There are two types of power dissipations in MOSFET, namely static power and dynamic power dissipations.

In Static power dissipation sub-threshold leakage, gate direct tunneling leakage, reverse-biased junction leakageand gate induced drain leakage shows the major effect in various scaling parameters. In Dynamic power dissipation switching and short circuit power will have the effect. The static and dynamic power dissipations are calculated theoretically from the equations shown in 1 and 2 respectively.

$$P_s = I_{cc} * V_{DD} \ldots\ldots\ldots\ldots\ldots (1)$$

$$P_D = \frac{1}{2} C_L (\Delta V_0)^2 f \ldots\ldots\ldots\ldots (2)$$

Where, I_{cc} = Sum of leakage current
V_{DD} = Supply voltage
C_L = Load capacitance
ΔV_0 = Logic voltage swing
f = Frequency of switching

Power delay product (PDP=P_{AVG}*T) is a parameter we used for comparison between various circuits to estimate the optimised results which can be operated at different frequency regions. A full adder is the base in digital circuits employed for performing arithmetical and logical operations, compressors, comparators and parity checkers. In present world of VLSI system applications such as specific DSP architecture, Systolic array design, microprocessors, FIR Filters, perform fundamental operations. Full adder is a core element that determines the overall performance of arithmetic circuit. In this paper, we designed improved full adder which operates in 22nm scaling technology using transmission gate (TG) logic.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The organization of this paper is as follows, in section II the previous works on full adder designs are discussed, then in section III the improved full adder design which is being proposed is discussed and finally in section IV the simulation results are shown and discussed from the observations in waveforms and power delay product values of different circuits. From the obtained results, in section V the paper has been concluded.

II. PREVIOUS WORK

A. CMOS Full Adder:

Starting with basic CMOS full adder circuit which consists of 28 transistors [1] as shown in figure 1, its delay is less which signifies the speed of operation and also has good voltage swing which shows the performance of the circuit but its power dissipation is more because of high transistor count, and of course the area occupied by the circuit will also be more.

B. Single gate MOSFET Full Adder:

In order to reduce the transistors count in full adder, a circuit is designed by using single gate MOSFET consists of 10 transistors [2] as shown in figure (2). A complementary signal was produced to generate sum and carry which doesn't require supply voltage ( ), the output is obtained only from input transitions. The main drawback is, it doesn't give strong zero at carry and also at 'zero' transitions there will be leakage in carry output. XNOR/XOR sub-circuit doesn't provide stable output for applied zero inputs.

C. Double gate MOSFET Full Adder:

To increase the output voltage swing in Single gate MOSFET a double gate MOSFET is designed by connecting two single gate transistors parallel in such a way that source and drain of two single gate MOSFET transistors are connected together [2] as shown in figure (3).This circuit has 4 pairs of NMOS and 6 pairs of PMOS, which gives transient analysis similar to single gate. But the draw back in this case is that it consumes more power when compared to single gate MOSFET when same W/L ratio is maintained as in Single gate MOSFET, so to overcome it, without affecting the output voltage swing, for Double gate MOSFET W/L ratio is maintained as 1:1.

1.III. PROPOSED FA CIRCUIT:

Transmission Gate MOSFET is designed by connecting transistors parallel in such a way that source and drain of two transistors are connected together [3] as shown in figure (4). In this logic, one PMOS transistor and one NMOS transistor is connected back to back. This circuit has 4 pairs of Transmission Gates as shown in figure (4). The Transmission gates are used to increase the output voltage level of MOSFET's which drives their output as input to a particular MOSFET for increase in output voltage swing. It overcomes the drawbacks in pass transistor logic and above mentioned logics in section II. As transistor count is reduced without effect in performance, this circuit is preferred. It can be operated at different loads and at different frequency of operations.

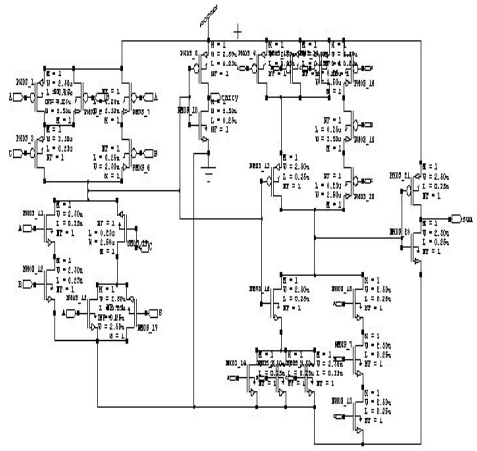

Figure 1: Basic CMOS full adder circuit

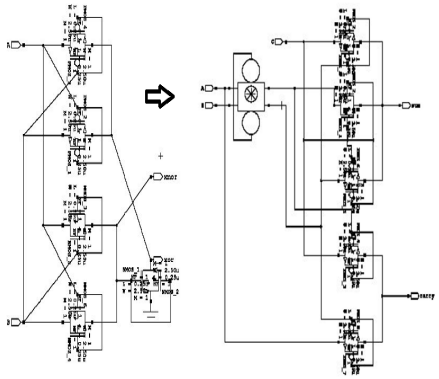

Figure 2: Single gate MOSFET full adder circuit

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

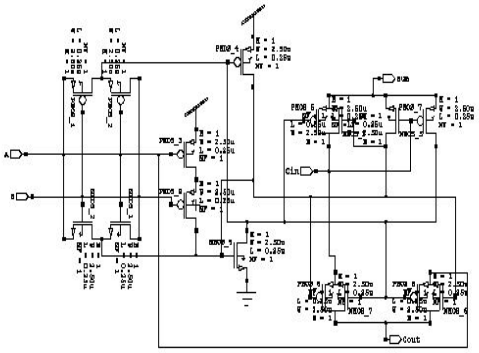

Figure 4: Transmission Gate full adder circuit

IV. SIMULATION RESULTS AND ANALYSIS:

In this Basic CMOS 22nm technology we apply supply voltage as 0.9V for better voltage swing. Here we maintain W/L ratio as 2:1. As shown in figure (5).In this single gate full adder we cannot get the output logic when =0.9V as shown in the figure (6). So that we increase input voltage up to 1.5V at that voltage we got the output it was shown in fig(7). Double gate MOSFET output logic is similar to the single gate MOSFET output logic as in figure (8) and (9).

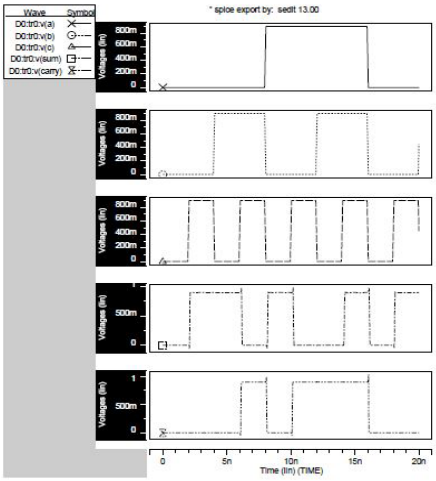

Figure 5: Basic CMOS full adder simulation results in 22nm

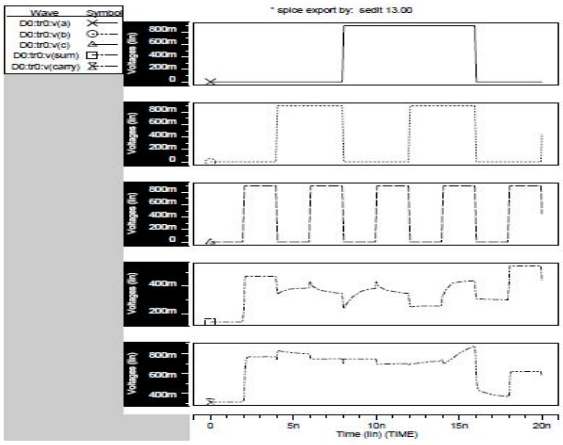

Figure 6: Single gate MOSFET simulation result in 22nm when VDD=0.9V

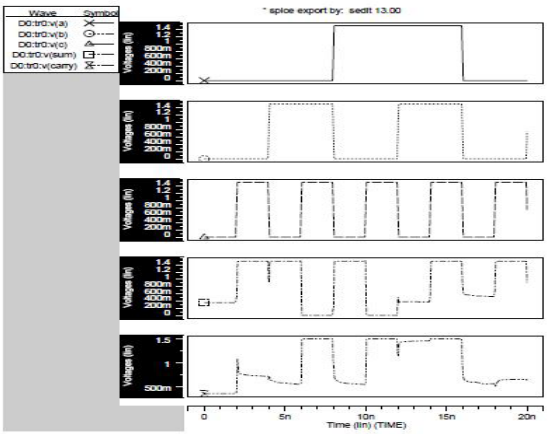

Figure 7: Single gate MOSFET simulation results in 22nm when VDD=1.5V

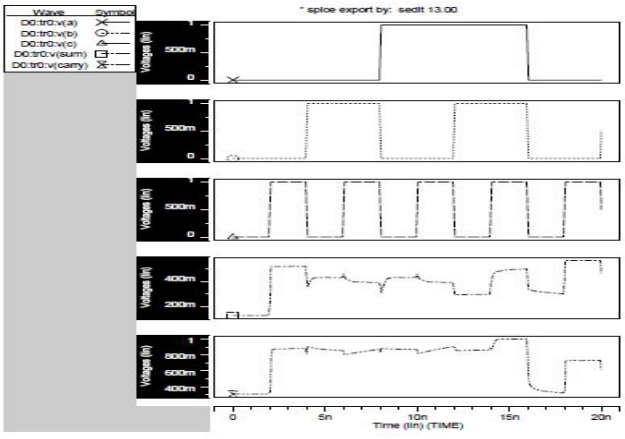

Figure 8: Double gate MOSFET simulation result in 22nm when VDD=0.9V

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

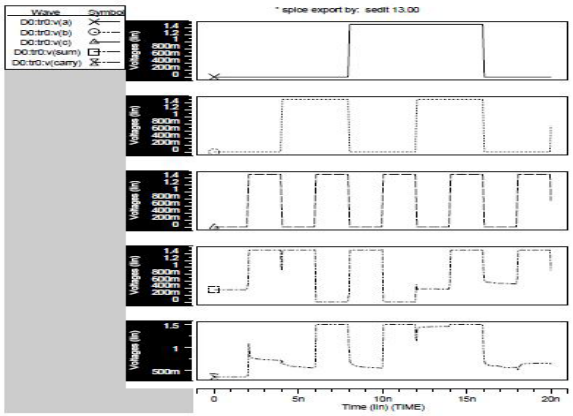

Figure9: Double gate MOSFET simulation results in 22nm when VDD=1.5V

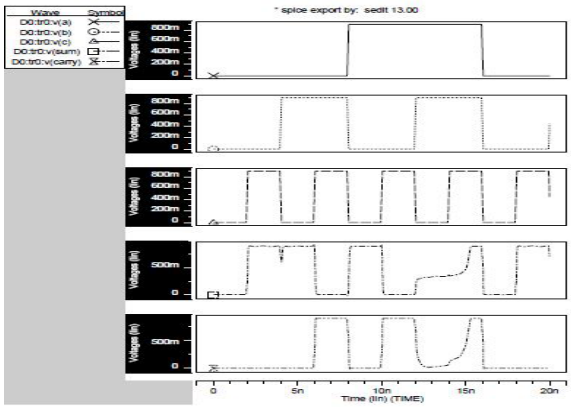

Figure 10: Transmission gate simulation result in 22nm

S.No	FULL ADDER	90 nm	45 nm	22 nm
1	Basic CMOS	1.132	5.16	0.0362
2	Single gate MOSFET	0.1854	0.787	0.0362
3	Double gate MOSFET	1.1124	0.63	1.19
4	Modified 16T	0.1549	0.408	0.02544

Table 1: Average power dissipation of full adders in micro watts (uW)

S.No	FULL ADDER	90nm	45nm	22nm
1	Basic CMOS	1.132	5.16	0.0362
2	Single gate MOSFET	0.1854	0.787	0.0362
3	Double gate MOSFET	1.1124	0.63	1.19
4	Modified 16T	0.1549	0.408	0.02544

Table 2: Power delay product of full adders in fecto joules(fJ)

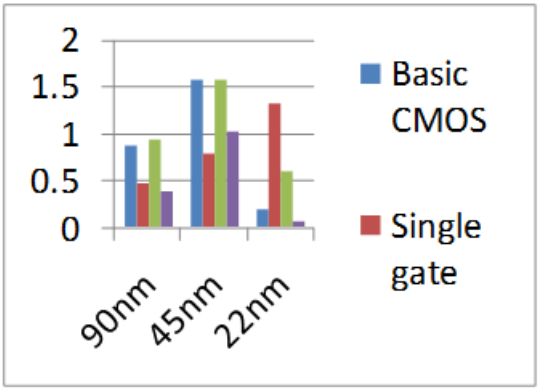

Figure 11: Comparison of Power dissipation w.r.t nanometer scaling technology

S.NO	Speed (MHz)	Basic CMOS	Modified circuit
1	50	0.7V	0.65V
2	300	0.8V	0.7V
3	500	0.9V	0.8V
4	1000	1V	1V

Table 3: Minimum supply voltage required at different frequencies

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

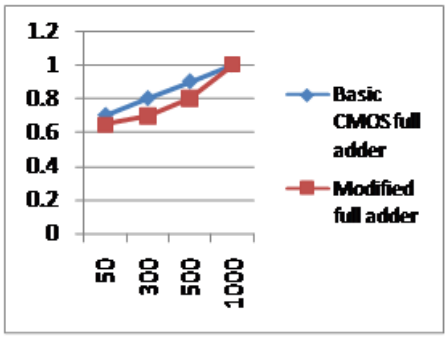

Figure 12: Comparison of Power delay product w.r.t nano meter scaling technology

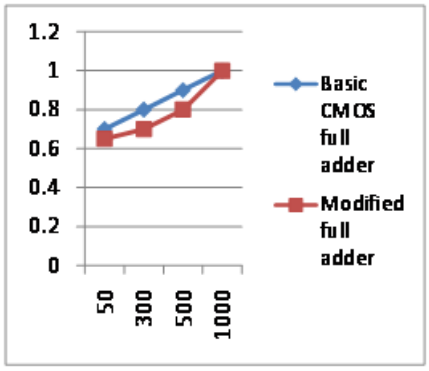

Figure 13: Comparison of required voltage w.r.t frequency

The average power dissipation in different nanometre scales of full adder circuits is shown in table 1. From the table, in 90nm and 22nm technology the modified full adder consumes less power. Coming to 45nm single gate MOSFET consumes less power but as mentioned in section II, "it doesn't give strong zero at carry at transition zero", as shown in figure (7). So, the proposed full adder has less power dissipation with good performance compared to remaining circuits.

Similarly, the power delay product analysis is done in table 2, the results shows that the proposed circuit had the best optimized results. In table 3, the results are taken by operating the full adder circuits with different frequencies and the minimum required supply voltages for operating with good voltage swings are tabulated.

In figure (11) and figure (12) the power dissipation and power delay product of the circuits are shown respectively. Figure (13) shows the comparison of required voltage to run the circuit with good voltage swing with respect to frequency.

V CONCLUSION:

Here by we would like to conclude our proposed full adder circuit dissipates low power with low delay without any degradation in performance. From the above simulation results when the circuit is operated without any load in 22nm both the power dissipation and power delay product are reduced by 10 times. Also in different frequency of operations the modified full adder can be operated at low voltages. The single gate and double gate MOSFET cannot be operated below 500MHz.

ACKNOWLEDGMENT:

We express my deep sense of gratitude and thanks Chairman sir Sri. Raghu Kalidindi, Dean Prof S. Veerabhadraiah, Head of the Department Mr. K.Phaninder Vinay and Principal Dr. R.Kameswara Rao sir of Raghu Engineering College Visakhapatnam, India for giving us this opportunity to carry out my project work at highly esteemed Organization.

REFERENCES:

[1] "Sleepy Keeper: a New Approach to Low-leakage", Se Hun Kim,2006.
[2] " Design of Full Adder circuit using Double Gate MOSFET", JagdeepKaurSahani, Shiwani Singh,2015.
[3] "An improved low power high speed full adder design with 28nm for extended region of operation", Deepak K Jena, ICECCE 2014. LSI Design"PHI Publications by Douglas A.Pucknell, Kamran Eshragian
[4] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE J. Solid-State Circuits, Vol. 27, No. 5, pp. 840-844, May 1992.
[5] C K Tung, S H Shieh and C H Cheng, "Low-power high-speed full adder for portable electronic application," Electronics Letters, The Institution of Engineering and Technology, Vol. 49, No. 17, August 2013.
[6] M Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Processing Systems, pp. 713–722, October 1999.
[7] C H Chang, J Gu and M Zhang, "A Review of 0.18-nm Full Adder Performances for Tree Structured Arithmetic Circuits," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 13, No. 6, June 2005.
[8] J M Rabaey, A Chandrakasan and B Nikolic, Digital Integrated Circuits-A design perspective, 2nd Edition, Prentice Hall, Englewood Cliffs,NJ,2002.