ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Efficiency Comparison of Synchronous Buck Converter with P, PI, PID Controllers

Mohammed Anwaruddin
Assistant Professor,
Dept of ECE,
NSAK College of Engineering and Technology, Hyderabad,
Telangana, India.

Khaleel Ahmed
Dept of EIE,
VNR Vignana Jyothi Institute of Engineering and Technology,
Hyderabad, Telangana,
India.

Mohd Anas Ali
Dept of ECE,
NSAK College of Engineering and Technology, Hyderabad,
Telangana, India.

Abstract:
This paper aims to design P, PI, PID compensators for the control of Synchronous Buck converter to improve its conversion efficiency under totally different load conditions. Since the diode rectifier is replaced by a high frequency MOSFET switch, the Synchronous control technique itself can be enough under serious load condition, to attain higher normal mode performance. However, this system does not hold well in light load condition, attributable to enhanced switching losses. A replacement control technique accompanied with P, PI, PID compensators is introduced within the paper can modify synchronous buck convertor to comprehend ZVS, while feeding light loads. This is often conjointly least price and extremely economical simple technique while not use of additional auxiliary switches and RLC components. This control technique conjointly proved to be efficient under input voltage variations. Simulation is done in MATLAB Simulink for proving stabilization provided by P, PI, PID compensators for synchronous buck converter.

Keywords:
Synchronous Buck Converter, ZVS, P, PI, PID.

1. Introduction:

The synchronous buck DC-DC device consists of two MOSFETs that are synchronized in operation. The auxiliary MOSFET is employed in place of freewheeling diode in order that physical phenomenon loss is reduced. Synchronous Buck converter is analogous to the traditional asynchronous buck converter except the freewheeling diode is paralleled with Synchronous switch Q2. It is known as a synchronous buck converter as a result of the Synchronous switch Q2 is synchronously turned on and off with the main switch Q1 operation and is shown in figure I. The primary idea of a synchronous buck converter is to utilize a MOSFET as a rectifier that has terribly low forward voltage drop compared to a diode rectifier. By lowering the forward voltage of diode, the efficiency for the conventional buck converter can be increased.

Thus, the synchronous buck topology has improved efficiency and synchronous rectifier (SR) switch (MOSFET Q2) needs a PWM signal that's the complementary of the first PWM signal. The SR switch Q2 is turned on once main switch Q1 is off and vice versa. This PWM format is termed Complementary PWM. The body diode of MOSFET Q2 acts as a slow rectifier and would add solely allowable losses. As a result of the synchronous rectifier switches with lower than a Voltage across itself, the switching losses are virtually zero. The MOSFET physical phenomenon losses are much lesser compared to the forward voltage drop of Schottky rectifier.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Synchronous Rectification will increment switching converter efficiency considerably with minimum cost. Throughout steady state situations, this switching of main and auxiliary MOSFETs ON and OFF complementary to every alternative maintains Vo to its desired worth. Therefore there is a desire to reduce switching losses using control techniques and to enhance the light load efficiency.

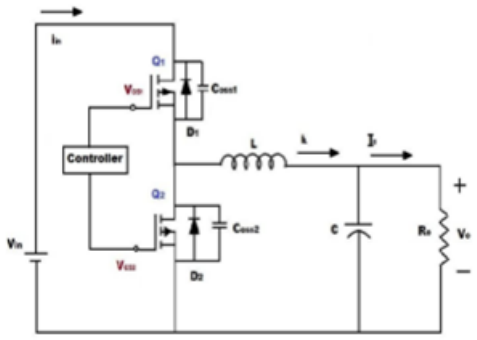

Fig. 1 Synchronous Buck DC-DC Converter

Many techniques are planned to scale back the switching losses arising from switching frequency. Pulse Width modulation (PWM), Pulse FM (PFM) Control and double-mode control with pulse width modulation (PWM) and pulse FM (PFM) are wide used. According to the previous researches, the PWM controlled device has lower conversion efficiency than the PFM-controlled device in light loads, whereas in heavy load condition, the PWM-controlled device possesses higher conversion efficiency compared to PFM. Therefore, some studies set to combine the benefits of each the control ways to create a replacement control methodology known as twin mode control. PFM is employed in light load condition, whereas PWM is chosen in high load condition. This methodology can do higher efficiency and additionally the nonlinear inductor is employed for lowering switching frequency at light load condition. However, giant output voltage transients and sub harmonic noise happens throughout transition between PWM and PFM. The change frequency is unpredictable and additionally needs sophisticated fabrication materials as a result of the variable frequency operation.

However alternative technique specifically resonant gate drive uses an inductor and two diodes provided to clamp and recover drive energy (clamped gate voltage). Additionally the circuit temporal order is adjusted to cycle electrical inductor current throughout driving transitions (fast driving speed). However the need of additional auxiliary switch and passive parts and gate-source voltage over drive are its disadvantages. Many techniques like zero voltage switching (ZVS) and digital control, are used, however the applications of those techniques appear to be a lot of sophisticated. ZVS and also the digital control technique have higher performance however want further auxiliary switches and RLC passive parts. Moreover, the controller used could be a digital system processor which is able to result overall cost to be high.

The new control strategy with P, PI, PID compensators during this paper allows an SR buck converter to possess increased light load potency with ZVS technique while not the need of additional auxiliary switches or RLC passive parts. This control methodology is of least price and also the technique is additionally straight forward. Moreover, the output voltage V(t) should be kept within nominal limits no matter the changes within the input line voltages and output loads. This is often accomplished by using negative- feedback system, wherever device output Vo is compared with its reference worth Vo,ref. The compensated error amplifier (P, PI, PID compensator network) produces the control voltage that is employed to regulate the duty cycle (d) of the switches within the converter.

2. Operating Modes:

The operation of a Synchronous buck convertor classified into eight stages based on the status of the two switches and load conditions. The oscillograph of the inductor current and control signals within the eight operative stages of Synchronous buck converter is shown in Fig. 3.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Based on the various load conditions whether heavy load or light load and according to the ways introduced here, there are two types of operating stage combinations. The primary operative stage combination is within the heavy load condition, i.e., Stage 1- Stage 2; whereas the second operative stage combination is in the light load condition, i.e., Stage 1- Stage 6.

The following assumptions are created to modify the analysis.

1. The output load voltage is assumed as constant voltage source owing to giant output capacitance.
2. No losses occur in any part of the circuit, i.e. all components in the circuit are assumed to be ideal.

2.1 Light Load Condition

A. Stage 1(t0 -t1):

In this state, the main switch Q1 is turned ON and the SR complementary switch Q2 is made to turn OFF. The path of conduction is shown in Fig. 2

$$i_L(t) = i_L(t_0) + \frac{(V_{in} - V_O)}{L}(t - t_0) \quad (1)$$

The inductive current equation is given above is same as that of stage 1 of heavy load condition.

B. Stage 2(t1- t2):

At the instant of t1, the SR complementary switch Q2 is switched ON and the main switch Q1 is made to turn OFF. The path of conduction is shown in figure II. The inductive current equation and the parasitic capacitive voltage equation is the same as that of stage 2 in heavy load condition and can be expressed as

$$i_L(t) = i_L(t_1) + \frac{(-V_O)}{L}(t - t_1)$$
$$v_{Coss1}(t) = V_{in} \quad (2)$$

C. Stage 3(t2- t3):

The current through the inductor has dropped to zero at the time instant t2. To avoid energy losses in the SR buck converter, the SR switch Q2 is made to turn OFF.

In this stage, the output inductor L begin to resonate with the parasitic capacitors Coss of switches Q1 and Q2 , which makes Coss1 to be discharged and other Coss2 to be charged. The inductive current iL(t) and parasitic capacitive voltage Vcoss1 can be given by:

$$i_L(t) = \frac{V_0}{Z} sin\omega(t - t_2)$$
$$v_{Coss1}(t) = (V_{in} - V_0) + V_0\ cos\omega(t - t_2) \quad (3)$$

Where

$$Z = \sqrt{\frac{L}{C}} \quad ; \omega = \frac{1}{\sqrt{LC}} \quad ; C = 2C_{OSS} = 2C_{OSS1} = 2C_{OSS2}$$

D. Stage 4(t3- t4):

In Stage 4, the main switch Q1 continued to be turned OFF, while the SR switch Q2 is turned ON. As a result, the voltage across the inductor is vL = -VO , which makes the inductor L to be energized and the inductive current increases linearly in opposite direction.

$$i_L(t) = -\frac{V_0}{L}(t - t_3) \quad (4)$$
$$v_{Coss1}(t) = V_{in}$$

E. Stage 5(t4- t5):

Stage 5 is the period for resonance. The main switch Q1 and the SR switch Q2, both are made to turn OFF. The SR rectifying switch Q2 is not conducted while the inductor current should be continuous. This current enables Coss1 to be discharged and Coss2 to be charged, until the voltage across the parasitic capacitor Coss1 of switch Q1 is discharged to zero, and the voltage across the parasitic capacitor Coss2 of switch Q2 is charged from zero to a voltage Vin. The inductive current iL(t) and parasitic capacitor voltage VCoss1(t) of switch Q1 are calculated as:

$$i_L(t) = \frac{V_0}{Z} sin\omega(t - t_4)$$
$$v_{Coss1}(t) = (V_{in} - V_0) + V_0\ cos\omega(t - t_4) \quad (5)$$

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Where

$$Z = \sqrt{\frac{L}{C}} \quad ; \omega = \frac{1}{\sqrt{LC}} \quad ; C = 2C_{OSS} = 2C_{OSS1} = 2C_{OSS2}$$

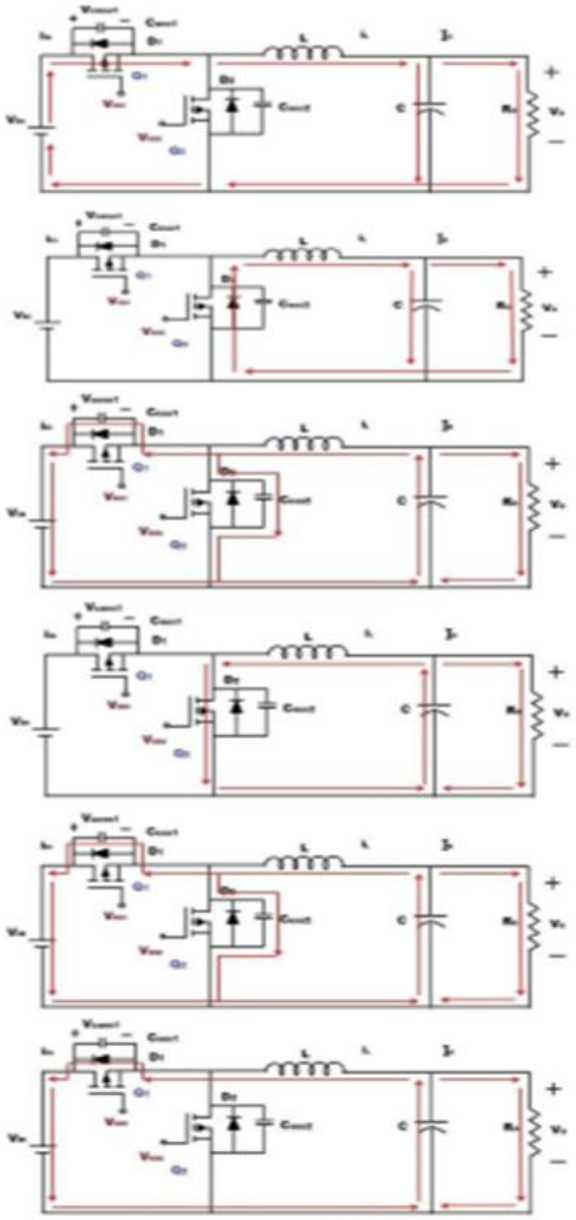

Fig. 2 Operating stages (stage1 –stage6)

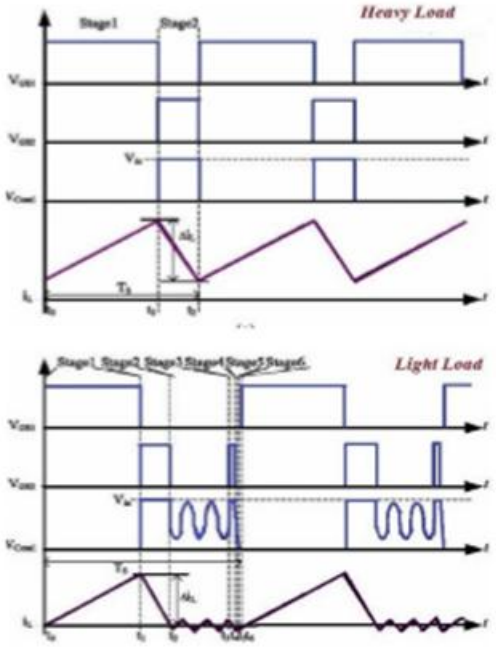

Fig. 3 Oscillogram of voltages and inductor current under different load conditions

F. Stage 6(t5- t6):

In Stage 6, the main switch Q1 and the SR rectifying switch Q2 are continued to be turned OFF. Though, the parasitic capacitance Coss1 has been already discharged in the previous stage, while Coss2 has been discharged by inductive current. The body diode D1 will be conducted. The zero voltage condition of Q1 has been achieved in this stage. iL(t) and vCoss1(t) of switch Q1 are given as:

$$i_L(t) = i_L(t_5) + \frac{(V_{in} - V_O)}{L}(t - t_5)$$
$$v_{Coss1}(t) = 0 \qquad (6)$$

According to the previous clarification, the synchronous buck convertor is operated in discontinuous mode (DCM) while operated in light load condition. Whereas the inductive current becomes lesser than zero, the SR rectifying switch Q2 continued to be conducted. This may lead to the decrease in conversion efficiency of the synchronous buck converter.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The SR rectifying switch Q2 is conducted at the second time in one switch cycle makes the main switch Q1 to be conducted with ZVS and increment the efficiency in light load condition. Finally, the control technique used here has the subsequent deserves. Under heavy loads, Synchronous technique is employed to cut back conductivity losses whereas under light loads, ZVS technique is achieved to cut back switching losses.

3. Control Strategy:

The control structural circuit diagram of the Synchronous buck converter is shown in Fig. 4. It is often conjointly seen that, there is another zero current detector (ZCD) circuit within the main frame, when put next with the traditional Synchronous buck converter. The ZCD circuit is especially used to sense the inductive current and to get the right signals for achieving ZVS in light load condition.

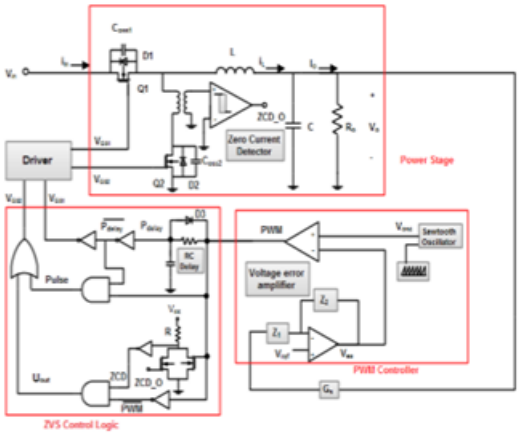

Fig. 4 Control circuit structural diagram of an SR buck converter

4. P, PI, PID Compensator Design:

A buck converter with voltage-mode control and voltage-mode error amplifier are often stable with the help of proportional-integral-derivative (PID) compensator. By keeping the ZVS logic circuit apart, the total circuit can be modeled with three blocks as painted in figure V. the power stage (Gp(s)) includes the power switches, the drivers and also the output inductor and output capacitor.

The model of the PWM generator is just represented by 1/ Vosc, wherever Vosc is that the peak to peak amplitude of the oscillator voltage (saw-tooth). The compensator block (H(s)) indicates the error-amplifier with the compensation network.

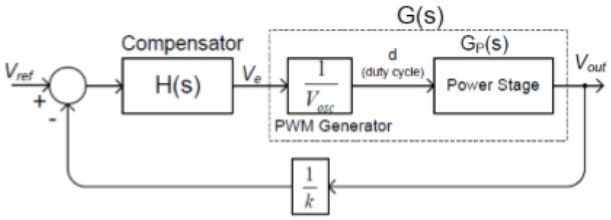

Fig. 5 The block diagram model of the synchronous buck converter

5. Simulation and Results:

The proposed synchronous buck DC-DC converter with P, PI, PID compensator control is simulated and the simulation model is presented in the MATLAB Environment.

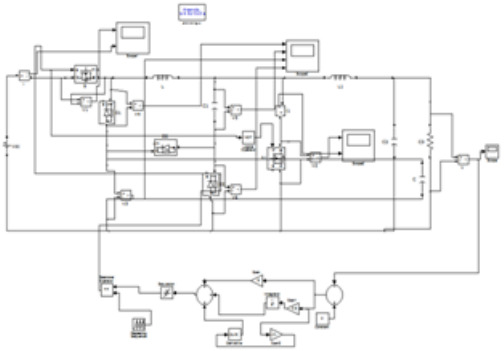

Fig. 6 Simulink model for the control of SR buck DC-DC converter with P, PI, PID Compensator

A. Sync Buck Converter with P compensator

Proportional controller gives the proportioned output value.

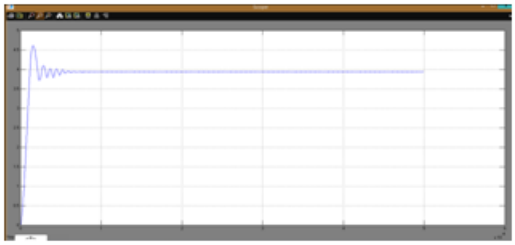

Fig 7. Response of Sync Buck Converter with P compensator

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

B. Sync Buck Converter with PI compensator:

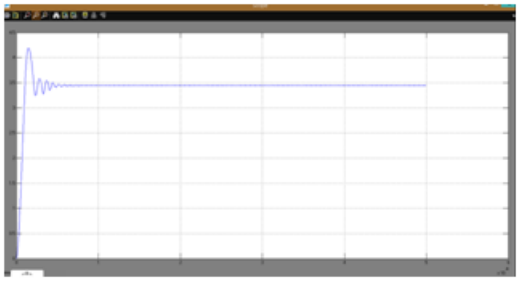

Fig 8. Response of Sync Buck Converter with PI compensator

C. Sync Buck Converter with PID compensator:

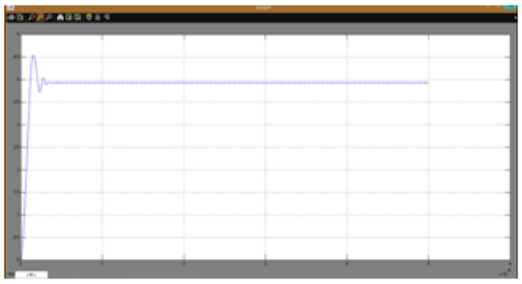

Fig 9. Response of Sync Buck Converter with PID compensator

Efficiency Comparison of Controllers:

S.no	Controller	Efficiency %	Power Loss %
1	P	85-96	4-15
2	PI	87-97	3-13
3	PID	90-98	2-10

Table 1. Efficiency comparison of controllers

6. Conclusions:

The P, PI, PID compensator network for the control strategy applicable to a Synchronous buck convertor below any load condition is intended and simulated by analyzing the convertor in operation principles. Under heavy load condition, Synchronous technique is used to reduced conduction losses whereas under light load conditions; ZVS technique is achieved to reduce the switch losses.

This is the control strategy adopted for Synchronous buck convertor to operate under any load conditions. This control technique has two advantages. First, due to the Synchronous technique, the diode of output rectifier is replaced by a MOSFET. This can facilitate to reduce conduction losses and increase the conversion efficiency of the convertor. Second, once the convertor is operated in light load condition, ZVS will be achieved successfully with none auxiliary switch or passive components(R, L, and C). In different words, there is no need to add additional cost in the convertor, and therefore the conversion efficiency of the converter may also be increased in light load condition. This new control strategy with Type III-A P, PI, PID compensator has higher conversion efficiency than the conventional control technique in light load condition. Simulation is completed showing the voltage mode control of Synchronous buck convertor stabilised with sort III-A P, PI, PID compensators and ZVS management logic circuit using MATLAB/SIMULINK.

References:

[1] Jian Min Wang, Sen Tung Wu and Gwan Chi Jane, “A Novel Control Scheme of Synchronous Buck Converter for ZVS in Light Load Condition", IEEE Trans. on Power Electronics, Vol. 26, No. 11, pp. 3265-3273, 2011.

[2] O. Garcia, P. Zumel, A. de Castro, P. Alou, and J. A. Cobos,“Current self balance mechanism in multiphase buck converter," IEEE Transactions on Power Electronics,vol. 24, no. 6, pp. 1600-1606, June 2009.

[3] X. Zhang and D. Maksimovic, “Multimode digital controller for synchronous buck converters operating over wide ranges of input voltages and load currents,” IEEE Transactions on Power Electronics, vol. 25, no. 8, pp. 1958-1965, Aug. 2010

[4] H. Deng, X. Duan, N. Sun, Y. Ma, A. Q. Huang, and D. Chen “Monolithically integrated boost converter based on 0.5-m CMOS process," IEEE Transactions on Power Electronics, vol. 20, no. 3, pp. 628-628, May 2005.

[5] M. Siu, P. K. T. Mok, K. N. Leung, Lam, Y.-H. Lam, and K. WingHung,"A voltage-mode PWM buck regulator with end-point prediction," IEEE Transactions on Circuits Systems II ,vol. 53, no. 4, pp. 294-298, Apr. 2006.

[6] E. Adib and H. Farzanehfard,"Zero-voltage-transition PWM converters with synchronous rectifier,"IEEE Transactions on Power Electronics,vol.25, no.1, pp. 105-110, Jan. 2010.

[7] H. Mao, O. Abdel Rahman, and I. Batarseh,"Zero-voltage-switching DC−DC converters with synchronous rectifiers,"IEEE Transactions on Power Electronics,vol. 23, no. 1, pp. 369-378, Jan. 2008.

[8] H. Bae, J. Lee, J. Yang, and B. H. Cho, "Digital resistive current (DRC) control for the parallel interleaved DC−DC converters," IEEE Transactions on Power Electronics,vol. 23, no. 5, pp. 2465-2476, Sep. 2008.

[9] M. Barai, S. Sengupta, and J. Biswas, "Dual-mode multiple-band digital controller for high-frequency DC-DC converter," IEEE Transactions on Power Electronics,vol. 24, no. 3, pp. 752-766, Mar. 2009.

[10] S. Saggini, D. Trevisan, P. Mattavelli, and M. Ghioni,"Synchronous -asynchronous digital voltage-mode control for DC-DC converters,"IEEE Transactions on Power Electronics,vol. 22, no. 4, pp. 1261-1268, Jul. 2007.

Author's Details:

Mohammed Anwaruddin, Received B.Tech Degree in Electronics and Communication Engineering from JSN College of Engineering and Technology affiliated to JNTUH Hyderabad and M.Tech from JNTUA, Anantapur in 2011.He is presently working in Nawab Shah Alam Khan College of Engineering and Technology, Hyderabad.

Mohammed Khaleel Ahmed, Received B.Tech Degree in Electronics and Communication Engineering from JPN College of Engineering affiliated to JNTUH Hyderabad and M.Tech from VJIT, Hyderabad in 2016.

Mohd Anas Ali, Received B.Tech Degree in Electronics and Communication Engineering from Pujya Shri Madhavanji College of Engineering and Teconology affiliated to JNTUH Hyderabad and M.Tech from Nawab Shah Alam Khan College of Engineering & Technology in 2015.He is presently working in Nawab Shah Alam Khan College of Engineering and Technology, Hyderabad.