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Area Efficient Z-TCAM for Network Applications

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Abstract:

The memories using in network devices such as routers, switches etc. should be capable of performing high speed search operations. Ternary Content Addressable memories (TCAMS) have great applications in the network devices, but it has some limitations while comparing with the Static Random Access Memory (SRAM), such as low storage density, relatively slow access time, low scalability, complex circuitry. These limitations can be overcome by designing TCAM using SRAM memory cells which is known as Z-TCAM. So this paper proposes an area efficient architecture of Z-TCAM which can perform the functionality of TCAM. The Z-TCAM is implemented in Xilinx14.2 ISE. In order to prove the physical existence of the proposed design it is verified with Basys 2 FPGA board. Also in this design it is able to show that from which channel the address is fetched. The area and power analysis of the proposed design is included in this paper. Power is analysed by using Xilinx XPower Analyzer.

INTRODUCTION:

Content addressable memory (CAM) is a special type of memory which can be searched by contents rather than address. Traditional memories will use the memory address for searching purpose and the output will be the content in that particular address location. CAM is performing the reverse process, it is using the content or part of the content for searching and the output will be a list of addresses where the content is stored. CAM memories can have only binary results0 or 1.Ternary content addressable memory(TCAM) which is an improvised version of CAM which can have a third state, ‘X’. This can have any value which makes it perfect for network applications. TCAM can perform lookup operation in a single clock. But when comparing with the Static random access memory (SRAM) TCAM have certain limitations. Low storage density, relatively slow access time, low scalability, complex circuitry are some of the disadvantages of TCAM. To overcome these limitations a new memory design called Z-TCAM is developed by using SRAM memory cells. Since this new architecture is developed with SRAM as fundamental building blocks so it overcomes all the disadvantages mentioned above. High speed and high throughput can be achieved by using SRAM based TCAMS in network applications .The objective of this paper is to make the Z-TCAM area efficient. The design is developed by using VHDL and synthesis in Xilinx ISE 14.2 and design is simulated in Isim simulator. In order to prove the physical existence of the proposed area efficient Z-TCAM the design is implemented on Basys 2 Spartan 3E FPGA board.

II. RELATED WORK:

Many works were in the development of CAM using RAM,but these suffers from collisions and bucket overflow.Interruption occurring when one or more searching operation happening simultaneously is the reason for collision.In some memory organisation it isdivided into different buckets,so the content may be in more than one bucket and the search operation will take more time to search in different buckets.The method proposed in[1] suffers from the problem that it is only a binary CAM not a TCAM.The algorithm used in[3] consuming multiple clock cycles for the operation and also results in inefficient usage of memory. Our proposed memory is independent of data so it can perform deterministic search operations.

RAM based CAM presented in [4] has the problems such as the exponential increment of memory as the number of bits of CAM word is increasing.The method in [5] only works on ascended data bit but in typicalCAM applications the datas are totally random.So there must be a way to arrange the data, but the arrangement will disturb the original address, which is not implemented inthis method.

IIIPROPOSED ARCHITECTURE OF Z-TCAM:

The Z-TCAM memory cells are implementing using SRAM memory cells, the block diagram of SRAM is shown in Fig.1.It contains 3 blocks such as AND gate, D flip-flop and a Tri-State buffer.SEL_NOT is deciding when to enable the circuit and WR_NOT will decide whether it is a read operation or a write operation

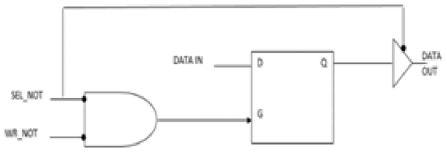


Fig.1. SRAM Memory Cell

A. Overall Architecture:

Fig.2 shows the overall architecture of Z-TCAM,it consist of input word ‘C’ which will be divided into N sub words.The sub word are of ‘w’ bits and they are fed to the layers. Each layer will produce an output address which called as potential memory address (PMA). From the PMA’s the CAM priority encoder will select the memory address (MA).

B. Layer Architecture:

Layer architecture is shown in Fig. 3. It consist of validation memory (VM) and the output is given to the 1 bit AND operation. The AND operation result will act as an activation signal and it will activate the original address table (OAT).The output of OAT to k bit AND operator which is followed by layer priority encoder (LPE).

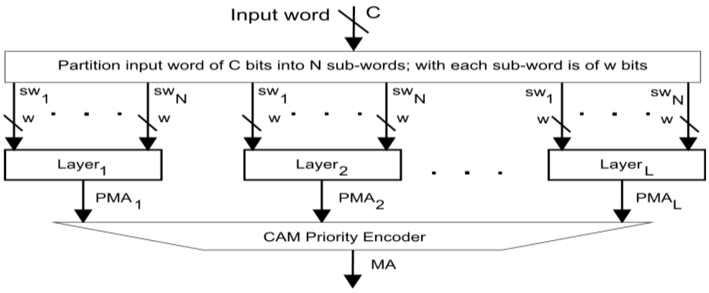

Input word
C
Partition input word of C bits into N sub-words; with each sub-word is of w bits
sw1
swN
w
Layer1
Layer2
LayerL
PMA1
PMA2
PMAL
CAM Priority Encoder
MA

Fig. 2. Architecture of Z-TCAM

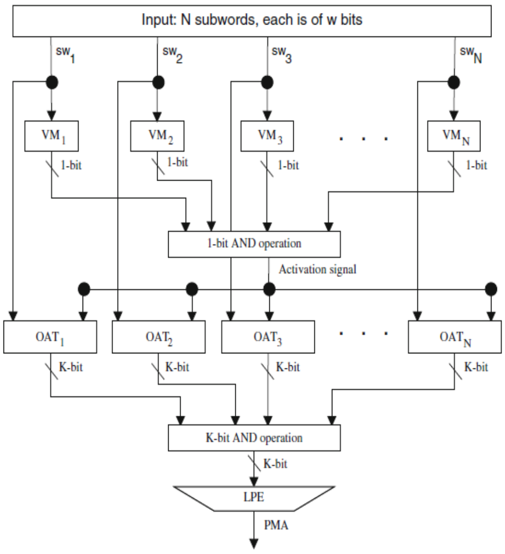


Fig. 3. Architecture of a layer in Z-TCAM

Validation Memory:

In the propose design 2 VMs are using in each layer. Input to the VM is the sub word which is obtained from the input keyword ‘C’.The VM size is 2^2bits, since the search keyword is of 4 bits. The number of rows in the validation memory is 4.The validation memory is validating the sub word,if the memory location invoked by the sub word in VM is high then the sub word is validated otherwise it will not be validated and stop the further actions.

1-bit AND Operation:

The output of all VMs are given for performing the AND operation. The operation performing here is a 1 bit AND operation. The output of this operation is deciding the further continuation of searching operation. If the output of AND operation is high then it will generate an activation signal which will activate the OAT block otherwise a mismatch will occur and stop the searching in that particular layer.

Original Address Table:

Size of each OAT is 2^w*k bits,‘w’is the number of bits in each sub word and 2^w is the number of rows and ‘k’ is the number of bits in each row. The activation signal is activating the OAT.OAT contains the original address.

K-bit AND Operation:

This performing a k bit AND operation which is a 2 bit AND operation according to the design the output of AND operation is fed to the LPE for further operations.

Layer Priority Encoder:

TCAM may have multiple results. The output of the k bit AND operation is given to the LPE for encoding the result of AND operation. The output of LPE is the PMA.

IV Z-TACM OPERATIONS:

The main two operations in the Z-TACM are mapping operation and searching operations. The mapping means first the data base or the memory should be assigned with the contents. This operation is actually a writeoperation. Once the mapping is implemented next step is the search operation, some algorithms are following in the search operations which is explained in the following sections

A. Data Mapping Operation:

In the design input word of 4 bits is using. So 2^2=4, i.e., 2 layers are using each layer consist of 2 VMs and 2 2 OATs.4 SRAM cells are using for each VM and 8 for OAT. .Data mapping operation is done as shown in the Fig.4.The validation memory is assigned with values as shown in the VM1and VM2.The output of this is actually assigned with values as shown in the second block. The output of this part will select the memory in OAT.

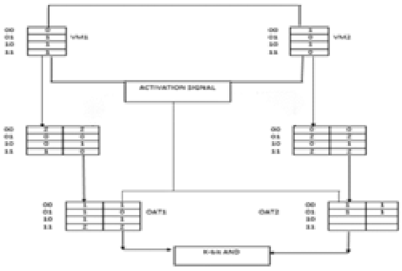
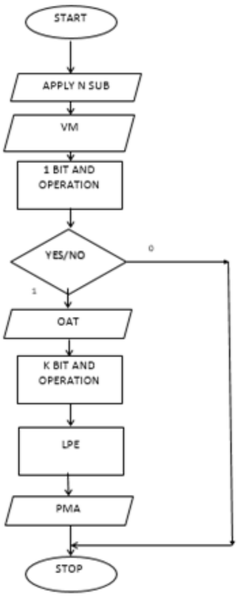


Fig.4 Mapping Operation

Search Operation

1) Searching in a Layer of Z-TCAM: Flow chartshown below describes the searching in a layer of Z-TCAM. N subwords are applied to the validation memories (VM) simultaneously. The VM will validate the subwords.The output of VM is given to the1 bit AND operator for generating the activation signal. If the VM is not validating the subword then the further searching will not takes place. The OAT will be activated by the activation signal. The address corresponding to the subword will be selected from the OATs. The outputs of OATs are given to the K bit AND operator which will perform bitwise AND operation.LPE will encode the output of AND operation and generate the PMA.

Flowchart for Searching In A Layer Of Z-TCAM



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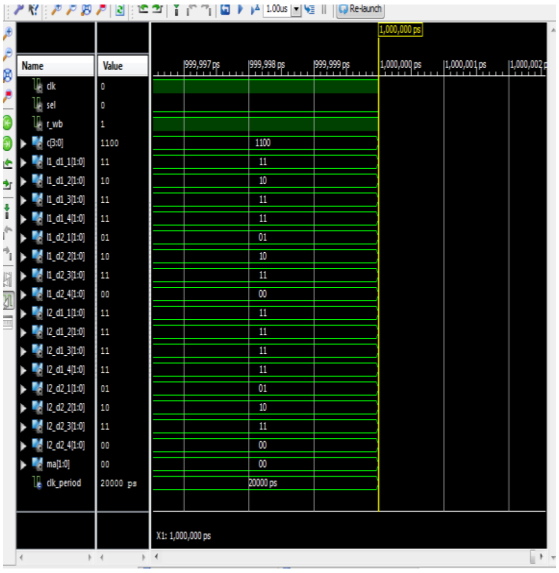
2) Searching in Z-TCAM:

In this searching process different layers are there inside Z-TCAM.In the proposed design 2 layers are using.The search keyword is applying to the Z-TCAM ,the keyword will be divided into subword and apply this to the layers.Thelayers will generate PMAs and CPE will select the MA from PMAs.

V. SIMULATION AND IMPLEMENTATION RESULTS

The proposed design is developed using VHDL and synthesized using XILINX 13.2 and is simulated in Isim Spartan-3E FPGA series. The simulation result of the ZTCAM is shown in Fig.5.Here the keyword is ‘1100’ and the matching address obtained is ‘00’.The RTL schematic view of the design is also shown in Fig.6.The Z-TCAM is developed for two layers and the searching operation will perform on these layers. There may be multiple results occur, so CAM priority encoder(CPE) is using to select the results properly.



Name	Value	
clk	0	
sel	0	
r_wb	1	
c[3:0]	1100	1100
l1_d1_1[1:0]	11	11
l1_d1_2[1:0]	10	10
l1_d1_3[1:0]	11	11
l1_d1_4[1:0]	11	11
l1_d2_1[1:0]	01	01
l1_d2_2[1:0]	10	10
l1_d2_3[1:0]	11	11
l1_d2_4[1:0]	00	00
l2_d1_1[1:0]	11	11
l2_d1_2[1:0]	11	11
l2_d1_3[1:0]	11	11
l2_d1_4[1:0]	11	11
l2_d2_1[1:0]	01	01
l2_d2_2[1:0]	10	10
l2_d2_3[1:0]	11	11
l2_d2_4[1:0]	00	00
ma[1:0]	00	00
clk_period	20000 ps	20000 ps

Fig.5 Simulation Result

The area improvisation can be proved by comparing the synthesis report of the existing design and the proposed design. The design summary of existing and proposed designs are shown in Fig.7 and Fig.8 respectively. From the comparison it is clear that the proposed system is efficient in terms of area.

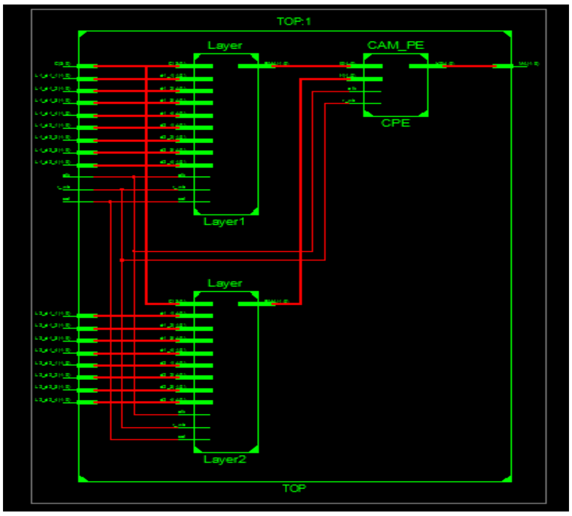
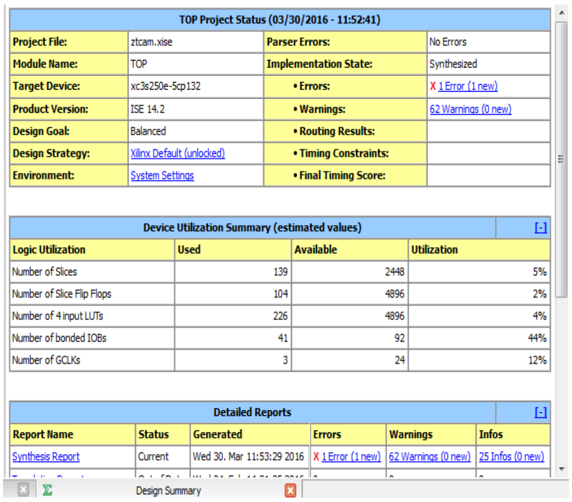


Fig.6 RTL Schematic View

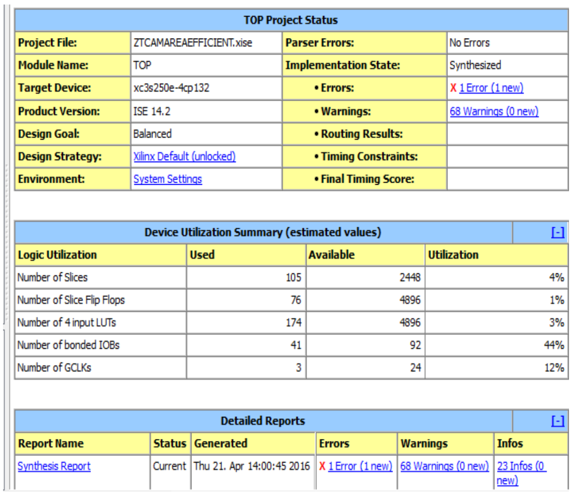


TOP Project Status (03/30/2016 - 11:52:41)			
Project File:	ztcam.xise	Parser Errors:	No Errors
Module Name:	TOP	Implementation State:	Synthesized
Target Device:	xc3s250e-5cp132	• Errors:	X 1 Error (1 new)
Product Version:	ISE 14.2	• Warnings:	62 Warnings (0 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	139	2448	5%
Number of Slice Flip Flops	104	4896	2%
Number of 4 input LUTs	226	4896	4%
Number of bonded IOBs	41	92	44%
Number of GCLKs	3	24	12%

Detailed Reports					[-]
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed 30. Mar 11:53:29 2016	X 1 Error (1 new)	62 Warnings (0 new)	25 Infos (0 new)

Fig.7 Design Summary of Existing Design



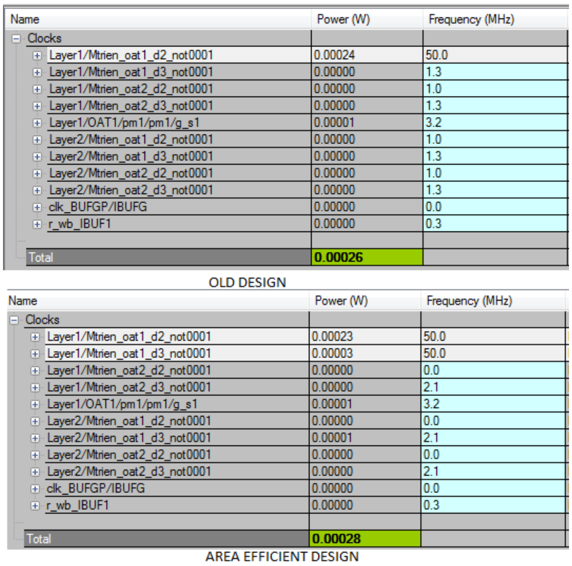
TOP Project Status			
Project File:	ZTCAMAREAEFFICIENT.xise	Parser Errors:	No Errors
Module Name:	TOP	Implementation State:	Synthesized
Target Device:	xc3s250e-4cp132	• Errors:	X 1 Error (1 new)
Product Version:	ISE 14.2	• Warnings:	68 Warnings (0 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	105	2448	4%
Number of Slice Flip Flops	76	4896	1%
Number of 4 input LUTs	174	4896	3%
Number of bonded IOBs	41	92	44%
Number of GCLKs	3	24	12%

Detailed Reports					[-]
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu 21. Apr 14:00:45 2016	X 1 Error (1 new)	68 Warnings (0 new)	23 Infos (0 new)

Fig.8.Design Summary of Proposed Design

Apart from the area analysis the power consumption of the design also analysed. The analysis is performed by using Xilinx XPowerAnalyzer.Power consumption for both existing design and area efficient design also performed. The results are shown in Fig.9.From the comparison it is clear that only a slight increase in the power consumption is there for the proposed area efficient design.



Name	Power (W)	Frequency (MHz)
Clocks		
Layer1/Mtrien_oat1_d2_not0001	0.00024	50.0
Layer1/Mtrien_oat1_d3_not0001	0.00000	1.3
Layer1/Mtrien_oat2_d2_not0001	0.00000	1.0
Layer1/Mtrien_oat2_d3_not0001	0.00000	1.3
Layer1/OAT1/pm1/pm1/g_s1	0.00001	3.2
Layer2/Mtrien_oat1_d2_not0001	0.00000	1.0
Layer2/Mtrien_oat1_d3_not0001	0.00000	1.3
Layer2/Mtrien_oat2_d2_not0001	0.00000	1.0
Layer2/Mtrien_oat2_d3_not0001	0.00000	1.3
clk_BUFGP/IBUFG	0.00000	0.0
r_wb_IBUF1	0.00000	0.3
Total	0.00026	

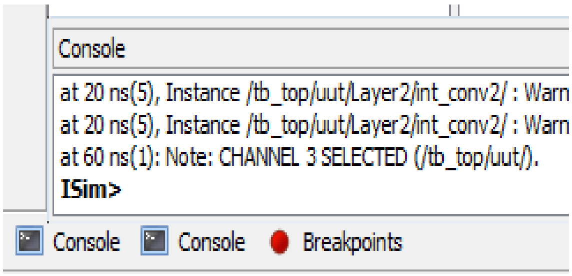
OLD DESIGN

Name	Power (W)	Frequency (MHz)
Clocks		
Layer1/Mtrien_oat1_d2_not0001	0.00023	50.0
Layer1/Mtrien_oat1_d3_not0001	0.00003	50.0
Layer1/Mtrien_oat2_d2_not0001	0.00000	0.0
Layer1/Mtrien_oat2_d3_not0001	0.00000	2.1
Layer1/OAT1/pm1/pm1/g_s1	0.00001	3.2
Layer2/Mtrien_oat1_d2_not0001	0.00000	0.0
Layer2/Mtrien_oat1_d3_not0001	0.00001	2.1
Layer2/Mtrien_oat2_d2_not0001	0.00000	0.0
Layer2/Mtrien_oat2_d3_not0001	0.00000	2.1
clk_BUFGP/IBUFG	0.00000	0.0
r_wb_IBUF1	0.00000	0.3
Total	0.00028	

AREA EFFICIENT DESIGN

Fig.9 Power Analysis of Designs

Also the proposed design is able to find from which channel the address is fetched. It is shown in Fig.10.



Console

```
at 20 ns(5), Instance /tb_top/uut/Layer2/int_conv2/ : Warn
at 20 ns(5), Instance /tb_top/uut/Layer2/int_conv2/ : Warn
at 60 ns(1): Note: CHANNEL 3 SELECTED (/tb_top/uut/).
ISim>
```

Fig.10.Channel Selection

VI. CONCLUSION:

The design of area efficient Z-TCAM is implemented by using the Xilinx 14.2 ISE and the results are verified by ISIM simulator. Power is analyzed by using Xilinx XPowerAnalyzer.Inorder to prove the physical existence of the design it is checked with Basys2 FPGA board.

Since the SRAM cells are used as the fundamental memory blocks it can perform better than conventional TCAM. So the developed Z-TCAM have more storage density, faster access time, high scalability etc. Also the proposed design is able to find from which channel the address is fetched. The Z-TCAM may have more advantages if we are able to modify it properly, so the future work is mainly focusing on the further improvement in terms of power or speed.

VII. REFERENCES:

[1]P. Mahoney, Y. Savaria, G. Bois, and P. Plante, "Parallel hashing memories: An alternative to content addressable memories," in Proc. 3rd Int. IEEE-NEWCAS Conf., Jun. 2005, pp. 223–226.

[2]Zahid Ullah, Manish K.Jaiswal, and Ray C.C>Cheung, "Z-TCAM: An SRAM-based Architecture for TCAM," in Proc. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION(VLSI)SYSYTEMS

[3]W. Jiang and V. Prasanna, "Parallel IP lookup using multiple SRAM based pipelines," in Proc. IEEE Int. Symp. Parallel Distrib. Process., Apr. 2008, pp. 1–14.

[4]S. V. Kartalopoulos, "RAM-based associative content-addressable memory device, method of operation thereof and ATM communication switching system employing the same," U.S. Patent 6097724, Aug. 1, 2000.

[5]M. Somasundaram, "Circuits to generate a sequential index for an input number in a pre-defined list of numbers," U.S. Patent 7155563 , Dec. 26, 2006.

[6]Kartalopoulos, "RAM-based associative content-addressable memory device, method of operation thereof and ATM communication switching system employing the same," U.S. Patent 6 097 724, Aug. 1, 2000. M. Somasundaram, "Memory and power efficient mechanism for fast table lookup," U.S. Patent 20 060 253 648, Nov. 2, 2006.

[7]M. Somasundaram, "Circuits to generate a sequential index for an input number in a pre-defined list of numbers," U.S. Patent 7 155 563, Dec.26, 2006.

[8].D. E. Taylor, “Survey and taxonomy of packet classification techniques,” ACM Comput. Surveys, New York, NY, USA:Tech. Rep .WUCSE-2004-24, 2004.

[9]. P. Mahoney, Y. Savaria, G. Bois, and P. Plante, “Transactions on high performance embedded architectures and compilers II,” in Performance Characterization for the Implementation of Content Addressable Memories Based on Parallel Hashing Memories, P. Stenström, Ed.Berlin, Germany: Springer-Verlag, 2009, pp. 307–325.

[10]. W. Jiang and V. Prasanna, “Scalable packet classification on FPGA,”IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 9,pp.1668–1680, Sep. 2012.

[11]. M. Becchi and P. Crowley, “Efficient regular expression evaluation: Theoryto practice,” in Proc. 4th ACM/IEEE Symp. Archit. Netw. Commun. Syst., Nov. 2008, pp. 50–59.

[12]. Xilinx, San Jose, CA, USA. Xilinx FPGAs [Online].Available:http://www.xilinx.com

[13]. W. Jiang and V. K. Prasanna, “Large-scale wire-speed packet classification on FPGAs,” in Proc. ACM/SIGDA Int. Symp . Field Program.GateArrays, 2009, pp. 219–228.

[14]. K. Pagiamtzis and A. Sheikholeslami, “Content-addressable memory(CAM) circuits and architectures: A tutorial and survey,” IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[15]. Xilinx, San Jose, CA, USA. Xilinx XpowerAnalyzer [Online]. Available:

[16]. http://www.xilinx.com

[17]. S.-J. Ruan, C.-Y.Wu, and J.-Y. Hsieh, “Low power design ofprecomputation-based content-addressable memory,” IEEE Trans. VeryLargeScaleIntegr. (VLSI) Syst., vol. 16, no. 3, pp. 331–335, Mar. 2008.H. Noda et al., “A cost-efficient high-performance dynamic TCAM withpipelined hierarchical searching and shift redundancy architecture,” IEEEJ. Solid-State Circuits, vol. 40, no. 1, pp. 245–253, Jan. 2005.

[18]. W. Jiang, V.K. Prasanna, N. Yamagaki, Decision forest: a scalable architecture for flexible flow matching on FPGA. In Proceedings of the2010 International Conference on Field Programmable Logic and Applications, FPL ’10, pp. 394–399 (2010).

[19]. Z. Ullah, K. Ilgon, S. Baeg, Hybrid partitioned SRAM-based ternary content addressable memory. Circuits Syst. I **59**(12), 2969–2979 (2012)