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Design of Low Power D-Flip Flop Using True Single Phase Clock (TSPC)

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ABSTRACT:
This paper enumerates a low power, high speed design of flip-flop having less number of transistors. In flip-flop design only one transistor is being clocked by short pulse train which is known as True Single Phase Clocking (TSPC) flip-flop. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. In this paper, an extensive comparison of existing designs of positive edge triggered True Single Phase Clocking Flip-flop is carried out. As True Single Phase Clocking (TSPC) flip-flop design has small area and low power consumption. And it can be used in various applications like digital VLSI clocking system, microprocessors, buffers etc. The analysis for various flip-flops for power dissipation and propagation delay has been carried out at different foundries. The designed flip-flops are compared in terms of power consumption and propagation delay and power delay product using DSCH and MICROWIND tools.

KEYWORDS: CMOS, TSPC flip-flop, Power, Delay, Figure of Merit (FOM).

I. INTRODUCTION:

Flip-flops are the basic building blocks of the data path structure. They allow for the storage of data, processed by combinational circuit and synchronization of operation at a given clock frequency. They are the fundamental building block of the digital electronics systems used in computers and many other types of systems. Flip flop can be either simple or clocked; simple devices are known as latches. A latch is level sensitive, and mainly used as storage element. And clocked devices are known as flip-flop. Flip-flop is edge sensitive means their output only changes on a single type of clock edge (positive or negative going edge). Flip-Flop is an electronic circuit that stores the logical state of one or more data input signal in response to a clocking pulse. They are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data [1].

Data is stored in flip-flop at each rising and falling edge of clock signal so that it can be applied as inputs to other combinational or sequential circuits, such flip-flops that store data on rising or falling edge of clock are referred as single edge triggered flip flops and the flip-flops that store data on both the rising and falling edge of a clock pulse are referred as double edge triggered flip-flops. In the earlier period, the VLSI designers were more bent towards the performance and area of the circuits. Cost and Reliability also gained core importance whereas power consumption was a peripheral consideration for them.

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In recent years, however, this has begun to change rapidly and power is being given equal importance in comparison to area and speed [2]. The main issues in the performance are- power dissipation and propagation delay. Power consumption is one of the basic constraints in any integrated circuit. There is always a trade- off between power and performance [3]. In CMOS circuit there are 3 sources of power dissipation, first static (leakage) power dissipation which is related to the logical states of the circuits and independent of switching activity. Second is short circuit power dissipation when both NMOS and PMOS transistor in the circuit is turned on simultaneously for short duration of time during switching. And as a result direct current path between powers supply and ground is formed. And third is Dynamic (switching) power dissipation which is caused by power dissipation during switching activity [4].

Another important timing value for a flip-flop is the clock-to-output delay i.e. the time taken by a flip-flop to change its output after the clock edge. In digital electronics, the power-delay product which is also known as switching energy, is FOM (figure of merit) correlated with the energy efficiency of a logic gate. Power delay product is used to evaluate the performance of CMOS process. When the technology scales down, total power dissipation decreases and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide thickness, and load capacitance [5]. This paper is organized as follows. Section II discusses a brief literature review and presents the design and work on true single phase clocking flip-flop. Section III presents layout simulation of different design of TSPC flip-flop. Section IV presents result analysis of edge triggered TSPC flip-flop. Section V concludes the paper and presents the future directions.

II. LITERATURE REVIEW:

In literature many designs have been proposed for the flip-flops. Several techniques as well as various flip-flops have been proposed recently to reduce redundancy in clock system. There are many flip-flops given in the literature [8]-[10]. Many digital and computational circuits selectively use master – slave and pulsed triggered flip-flops [6]. The paper presents small area dynamic TSPCL (True Single Phase Clocked Logic) D flip-flops that were presented in [5] and [7]. These edge triggered flip-flops are small in area since they exhibit low transistor count. With a simple modification, the internal switching at some nodes of these flip-flops is minimized in order to reduce power consumption [7]. TSPCL dynamic logic style uses just a single clock signal for synchronization and it also reduces complexity.

In the design of TSPC flip-flop edge triggered (positive or negative) D flip-flop is used. The circuit consists of alternating stages called n-blocks and p-blocks and each block is being driven by the same clock signal. The schematic of original TSPC flip-flop is shown in Fig.1. In this design a single global clock signal needs to be generated and distributed in order to simplify the design. Fig.1 Shows the Conventional d flip flop in dsch schematic, Fig .2 shows the schematic of TSPC D flip-flop with 10 transistors, this edge triggered flip-flop uses just a single clock signal for synchronization. It is operated as when the clock signal clk is LOW, the input is isolated from the output. When clock makes a LOW-to-HIGH the output will latch the complement of the input.

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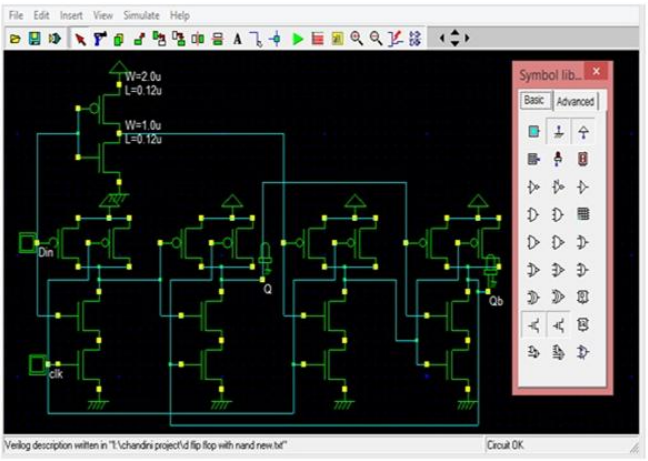

Fig.1 The Conventional d flip flop in dsch schematic

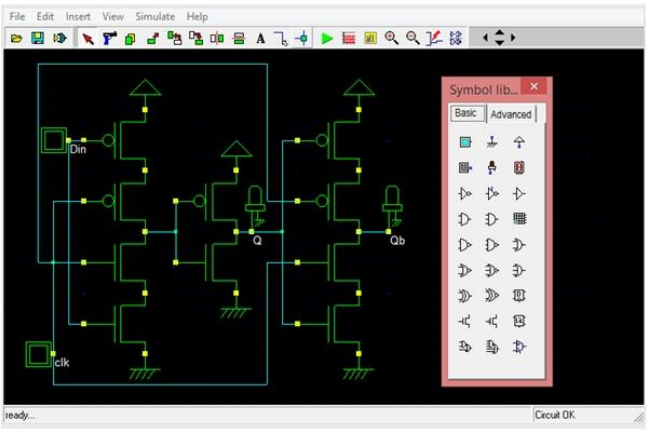

Fig.2. 10 Transistors TSPC D Flip-Flop

Fig.2 shows the positive edge triggered 10 transistors TSPC (True Single Phase Clocking) flip-flop. During the ON period whatever is the value of input it becomes output. Now another design of TSPC D flip-flop with 5 transistors. The schematic of 5 transistors TSPC D flip-flop is shown in Fig.3. This flip-flop is built using 3 NMOS and 2 PMOS transistors. This edge triggered flip-flop is small in area since it exhibit low transistor count only 5 transistors are used and it also reduces power consumption.

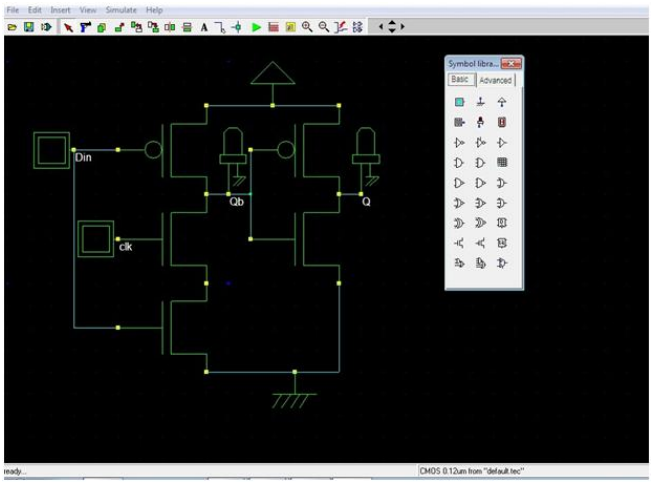

Fig.3. 5 Transistors TSPC D Flip-Flop

Fig.3 shows positive edge triggered 5 transistors TSPC D flip-flop. When clock clk and input is high then output is also high. During ON period of clock whatever the value of input it becomes output.

III. LAYOUT SIMULATION:

Performance analysis of both the designs of TSPC D flip-flop is presented in this section. Designs are simulated using DSCH and MICROWIND Tools at different technologies like 90nm, 70nm, 50nm. The layout design rule describes how the small features can be and how closely they can be packed in particular manufacturing process. Different logical layers are used by the designers to generate the layout. There are specific layers for metal, contacts or diffusion areas, polysilicon. In the layout design red color presents polysilicon, green color indicates n+ diffusion, light green color indicates p+ diffusion, light and dark blue color shows metal1 and metal 2 respectively. Now the layout of Conventional D Flip Fop with micro-wind software using λ based design rule is shown in the Fig.4 and the layout of D Flip Fop with 11 transistors TSPC D flip-flop with micro-wind software using λ based design rule is shown in the Fig.5 using 90nm technologies.

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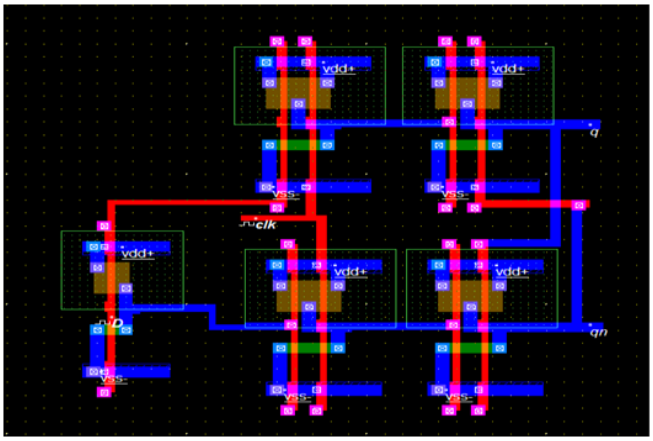

Fig 4 Conventional d flip flop layout in Microwind

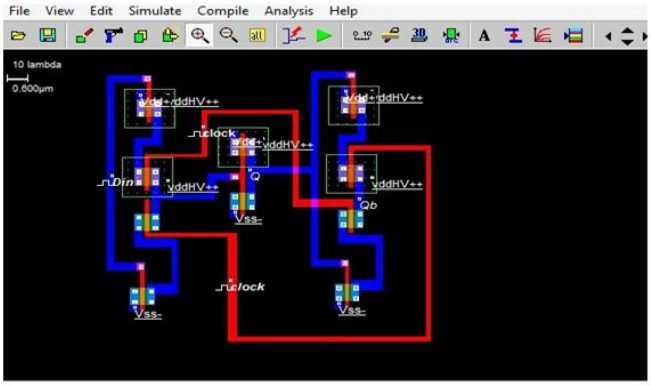

Fig.5. Layout of 11 transistors TSPC D flip-flop

The layout design for 5 transistor TSPC D flip-flop using 90nm technology is shown in Fig.6

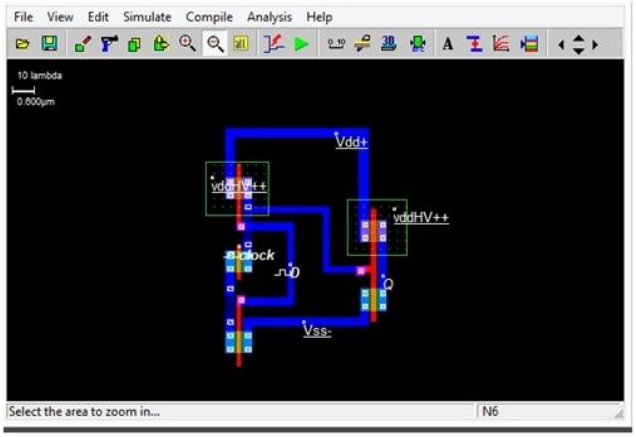

Fig.6. Layout of 5 transistor TSPC D flip-flop

The simulation is performed on MICROWIND software; result of simulation includes parameters such as power dissipation, delay and power delay product (PDP). The results indicate the comparative study of edge triggered TSPC D flip-flop with 10 transistors and with 5 transistors using different technologies like 90nm, 70nm, 50nm.

IV. RESULT ANALYSIS:

On the basis of the simulation results, now we will prepare a comparison table. This table presents comparative study of simulation parameters for the design of edge triggered TSPC D flip-flop with 10 transistors and with 5 transistors.

Factor description:	Conventional d flip flop:	Proposed d flip flop:
Number of transistors	10 T	5T
Power dissipation	8.46 µW	4.775µW
delay	10ps	16ps

V. CONCLUSION:

Since Flip flops are one of the most complex and power consuming component among the various building blocks in digital designs and Clocking network and flip flops consume about 30 to 70 % of total power in the system out of which 90 % is consumed by flip flop. In some circuits it is the main aim to reduce the area and reduce the delay, at that time the 5T Flip Flop is preferred. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. As True Single Phase Clocking (TSPC) flip-flop design has small area and low power consumption. And it can be used in various applications like digital VLSI clocking system, microprocessors, buffers etc. The analysis for various flip-flops for power dissipation and propagation delay has been carried out at different foundries. The designed flip-flops are compared in terms of power consumption and propagation delay and power delay product using DSCH and MICROWIND tools.

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