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Design of Reversible Arithmetic and Logic Unit (ALU) Using VERILOG HDL

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ABSTRACT:

In low power circuit design, reversible computing has become one of the most efficient and prominent techniques in recent years. In this paper, reversible Arithmetic and Logic Unit (ALU) is designed to show its major implications on the Central Processing Unit (CPU).In this paper, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analyzed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design. we exploring the design of a 16 bit reversible Arithmetic Logic Unit (ALU) with 15 operations is presented by making use of Double Peres gate, Fredkin gate, Toffolli gate, DKG gate and NOT gate. A first single bit reversible ALU and second single bit ALU are designed and Then 16 single bit ALU's are cascaded together taking carry out of ALU performing LSB operation as an input to carry in of ALU performing next LSB operation. Design is implemented and verified in Verilog HDL in Xilinx 14.4.

I.INTRODUCTION

For the past decades, there were numerous of difficulties and problems occurred in the development of conventional computing technologies. The major problem of the conventional computing technologies is power dissipation which is an important issue in today's computer chip [1]. The advancement in Very Large Scale Integrated (VLSI) designs especially in portable device technologies lead to faster, smaller and more complex electronic system design [2]. In VLSI design, the conventional logic circuits dissipate more power. In the conventional logic circuits, every bit of information loss will generate kTlog2 joules of heat energy [3]. In the conventional logic circuit design, information loss occurs due to the total number of output signals is less than the total number of input signals applied to the logic circuit.

Reversible computing is a promising method in low power dissipating circuit design for current technologies such as low power Complementary Metal Oxide Semiconductor (CMOS) design, cryptography, optical information processing, quantum computing and nanotechnology [4]. Reversible logic can be defined as thermodynamics of information processing. Hence, it is used to reduce the power dissipation by preventing the loss on information. It is shown in[5, 6] that the circuit which designed using reversible logic can eliminate the heat dissipation due to information loss. This is due to the amount of energy dissipated in a system which bears a direct relationship to the number of bits erased during computation. The difference between the reversible circuits and

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conventional logic circuits is that the reversible circuits are built from reversible logic gates.

Arithmetic and Logic Unit (ALU) works as a data processing unit which is an important part in the central process unit (CPU) of any computer architecture. ALU is a multi-functional circuit that performs one of a few possible functions on two operands and which depends on the control inputs [7]. ALU needs to continually perform during the life-time of any computational devices such as a computer or a hand held device such as hand phone. Thus, reversible logic can be implemented in designing ALU to reduce the power dissipation and propagation delay in the circuits [8]. In this paper, two new reversible ALU designs are proposed using two different reversible full adder logic circuits. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed reversible ALU design 1, Peres Full Adder Gate (PFAG) is used in the design, HNG gate [9] is used as an adder logic circuit in the proposed reversible ALU design 2. The proposed designs
are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. A short review on few existing reversible gates is detailed in section-II of the paper. Section-III introduces the proposed ALU designs. The 16 bit ALU shown in section-IV The simulations results are shown in section-V.The conclusion and references section-VI.

II.REVERSIBLE LOGIC GATES:

A reversible logic circuit is said to be reversible if the number of inputs is equal to the number of outputs [10]. In order to achieve a synthesised low power circuit, the reversible logic circuits should have the following specifications which are minimum number of reversible gates or gate count, minimum number of garbage outputs, minimum propagation delay and minimum quantum cost [11]. In the proposed ALU designs, R-I, Feynman, Fredkin and Peres reversible gates are used. The quantum implementations of the three gates are described in the following subsections.

Feynman gate:

Feynman gate is also known as Controlled-Not gate (CNOT). It is a reversible of 2*2 gate with 2 inputs and 2 outputs. The quantum cost of Feynman gate is one. This is proven since it has mapping input of A and B to output of P and Q as shown in the Fig.1 [12]. Feynman gate is made from one EX-OR gate.

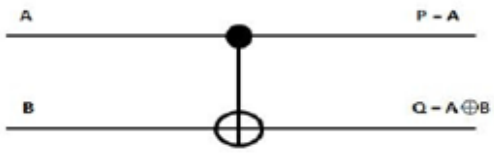

Fig.1: Quantum implementation of Feynman gate

Fredkin gate

Fredkin gate is a reversible of 3*3 gate with 3 inputs and 3 outputs. The quantum implementation of the gate is shown in the Fig.2 that the inputs (A, B, C) are mapped to the outputs (P, Q, and R) and the quantum cost of Fredkin gate is five. The two dotted rectangles in the Fig. 2 is equivalent to a 2*2 Feynman gate with the quantum cost of one for each dotted rectangle. The other 3 quantum cost comes from one V and two CNOT gates [12].

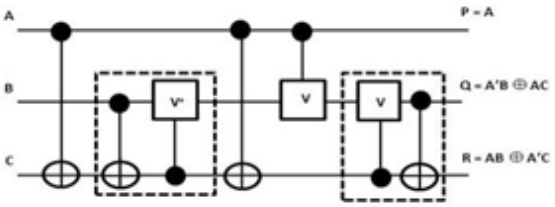

Fig.2: Quantum implementation of Fredkin gate

R-I gate

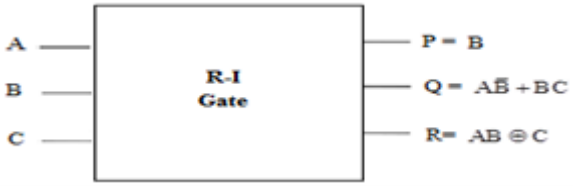

Fig.3: Quantum implementation of R-I gate

R-I gate is a reversible of 3*3 gate with three inputs and three outputs. The Fig. 3 shows the proposed R-I reversiblegate. The outputs are defined by P=B, Q=

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AB + BC , R= ABÅC . R-I gate requires only 7 transistors for the transistor level implementation. A single block of R-I gate can be realized as, Multiplexer, Demultiplexer, XOR, AND, OR, NOT etc. R-I gate is made from one EX-OR, one OR, one NOT and three AND gate.

DPG Gate

Double Peres Gate is 4*4 gate with quantum cost of 6. It is shown in the Fig.4

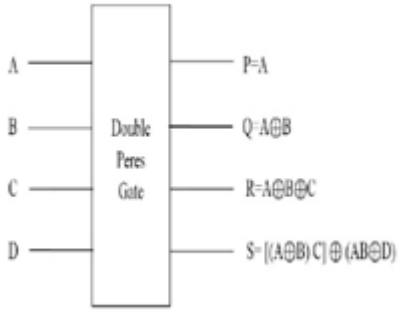

Fig.4. Double Peres Gate

DKG Gate

Itis 4* 4 reversible DKG gate [6] that can work singly as a reversible Full adder and a reversible Full subtractor is shown in Fig 5. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtractor.

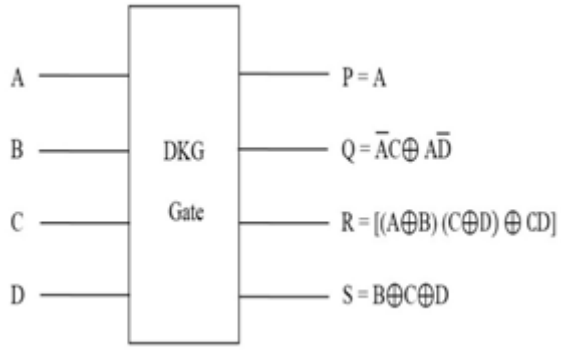

Fig.5. DKG Gate

III.REVERSIBLE ALU DESIGN:

ALU works as a data processing components which is an important part in the central process unit (CPU). Besides, it is the main performer in any computing devices. ALU is a multi-functional circuit that performs one of a few possible functions on two operands of A and B which is depending on the control inputs.

A. Conventional ALU Design:

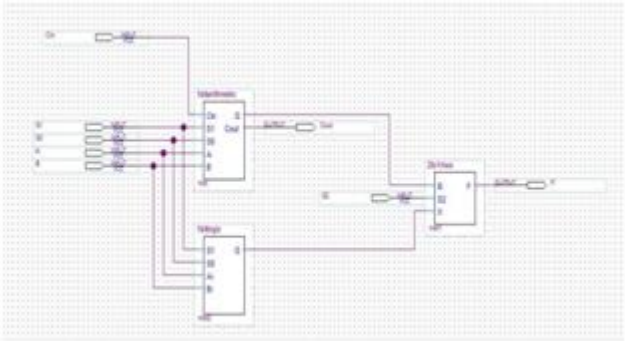

Fig.6: Block diagram of 1-bit conventional ALU design in Quartus II software

As show in Fig.4, the S2, S1 and S0 are the selection lines while Cin is the input carry. Input A and B are the data input for the ALU design. Based on the truth table shown in Table 1, when selection line S2 is equal to zero, the circuit performs eight arithmetic operations and when selection line S2 is equal to one, the circuit performs the logic operations of OR, EX-OR, AND and NOT functions.

Table 1: Function table for ALU

S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	F = A	Transfer A
0	0	0	1	F = A+1	Increment A
0	0	1	0	F = A+B	Addition
0	0	1	1	F = A+B+1	Add with carry
0	1	0	0	F = A+B'	Subtract with borrow
0	1	0	1	F = A+B'+1	Subtraction
0	1	1	0	F = A-1	Decrement A
0	1	1	1	F = A	Transfer A
1	0	0	X	F = A∨B	OR
1	0	0	X	F = A⊕B	EX-OR
1	0	1	X	F = A^B	AND
1	0	1	X	F = A'	NOT

Fig.6 is the logic circuit design for 1-bit conventional ALU which is implemented in Altera Quartus II software. 4-bits, 8-bits and 16-bits of conventional ALU design can be implemented by expanding 1-bit ALU design.

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Reversible ALU:

The proposed reversible ALU is designed to produce the same function as implemented by conventional ALU. Fig.7 is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the proposed design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) with a provision for realizing the eight arithmetic operations and four logic operations.

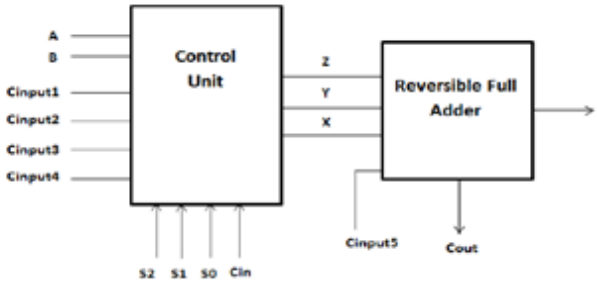

Fig.7: Block diagram of reversible ALU design

Control Unit

Control unit is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU. As shown in Fig.6, the proposed control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables S2, S1, S0 and Cin select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of S2. The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit.

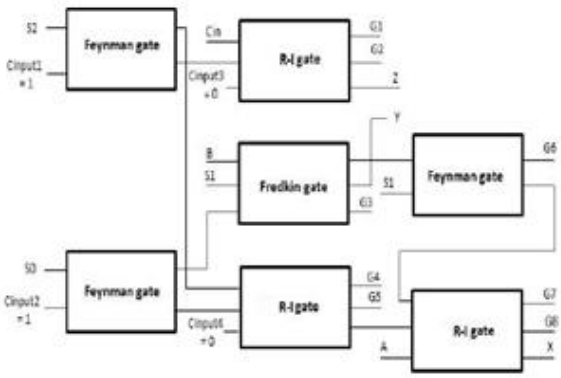

Fig.8: Block diagram of control unit

Reversible Full Adder

Full adder is the important building block in ALU unit. Compatible reversible adder implementations is required in the anticipated paradigm shift logic compatible with the optical and quantum. The outputs of the reversible adder are given in the following equations:

$$Sum=A\oplus B\oplus Cin \quad (1)$$

$$Cout= (A\oplus B)Cin\oplus AB \quad (2)$$

a) PFAGGate

The PFAG gate is 4x4 reversible gate. Outputs, P and Q are considered as the garbage outputs. The output, R and S are represented the function of Sum and Cout respectively. The quantum cost of PFAG is 8 since it made from 2 Peres gates [13]. Fig.9 is the logic circuit design of PFAG gate in Quartus II software.

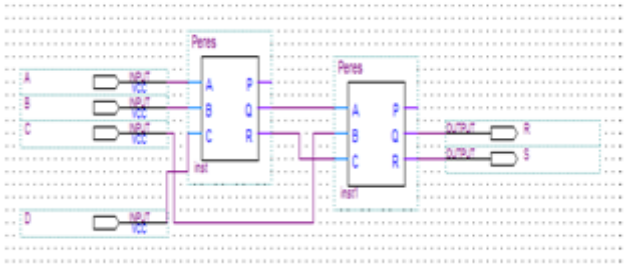

Fig.9: Logic circuit design of PFAG gate in Quartus II software

b) HNGGate

The HNG gate is 4x4 reversible gate. Outputs, P and Q are considered as the garbage output. The outputs, R and S are represented the function of Sum and Cout respectively. The quantum cost of HNG gate is 6 [14]. Fig.10 is the logic circuit design of HNG gate in Quartus II software.

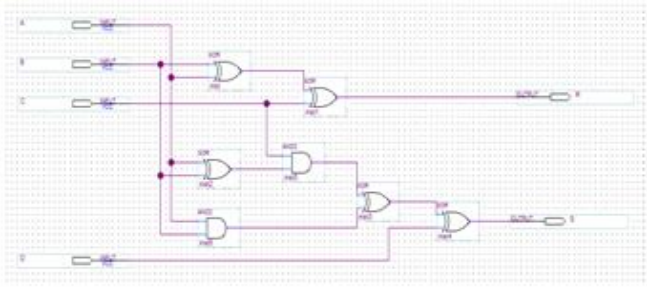

Fig.10: Logic circuit design of HNG gate in Quartus II software

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Proposed Reversible ALU Design 1

Shown in Fig. 11 is the block diagram of the proposed reversible ALU design 1. The proposed ALU design is implemented in Altera Quartus II software which is show in Fig.12.

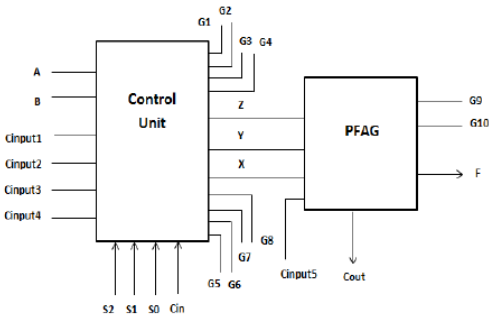

Fig.11: Block diagram of the proposed reversible ALU design 1.

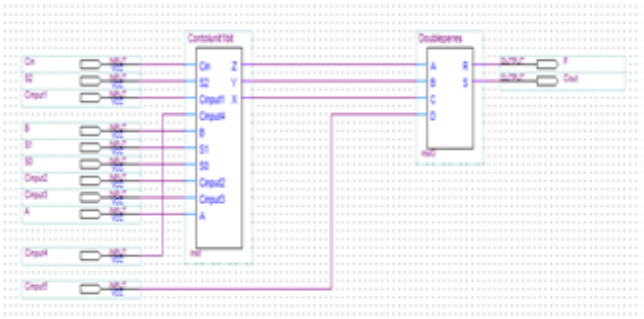

Fig.10: Logic circuit design of proposed reversible ALU design 1 in Quartus II software.

Proposed Reversible ALU Design 2

Shown in Fig. 12 is the block diagram of the proposed reversible ALU design 2.

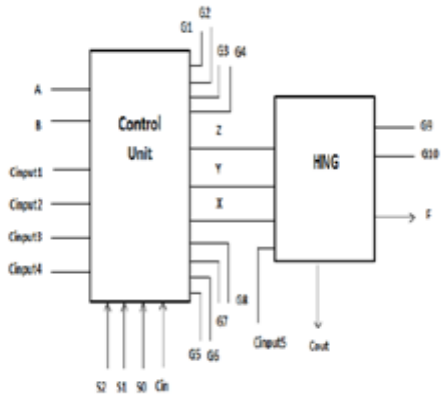

Fig.12: Block design of the proposed reversible ALU design 2

Shown in Fig.13 is the logic circuit design for 1-bit reversible ALU which is implemented in Quartus II software. 4-bits, 8-bits and 16-bits of reversible ALU design can be implemented from 1-bit ALU design.

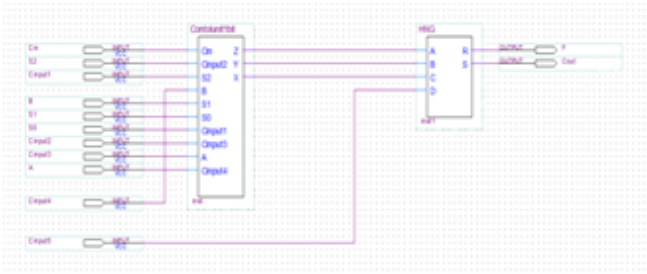

Fig.13: Logic circuit design of proposed reversible ALU design 2 in Quartus II software.

IV.16 BIT REVERSIBLE ALU

A. 1-BIT-ALU

The ALU that is proposed is 15-operations. ThereALU has 2 parts. 1st which has Double Peres Gate as base of the circuit and is selected when select line s3 is zero. The operations performed here are buffer, AND, OR, NAND, NOR, EX-OR, and EX-NOR. 2nd part has DKG Gate as base of the circuit and is selected when select line s3 isone. The operations performed here are add, increment, 2's complement, set, subtract, decrement, not, and clear.The operations selected depending on various select line are shown in the table-2

Table-2

S3	S2	S1	S0	Operations
0	0	0	0	AND
0	0	0	1	NAND
0	0	1	0	OR
0	0	1	1	NOR
0	1	0	0	BUFFER A
0	1	0	1	EX-OR
0	1	1	0	BUFFER B
0	1	1	1	EX-NOR
1	0	0	0	ADDITION
1	0	0	1	INCREMENT
1	0	1	0	2's COMPLEMENT
1	0	1	1	SET
1	1	0	0	SUBSTRACTION
1	1	0	1	DECREMENT
1	1	1	0	NOT
1	1	1	1	CLEAR

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The 2:1 Multiplexer is designed using Fredkin gate when we make A as select line and (B & C) as input. B orC is selected depending on A is 0 or 1 respectively. The Block diagram is shown in fig 14.

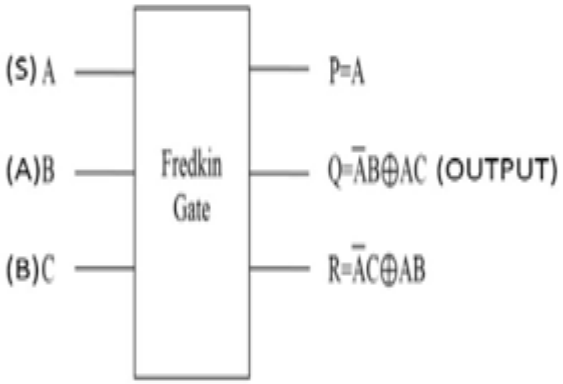

Fig.14. 2:1 MUX

Design of 1st1-bit ALU with 15 operations is shown in the fig 15.

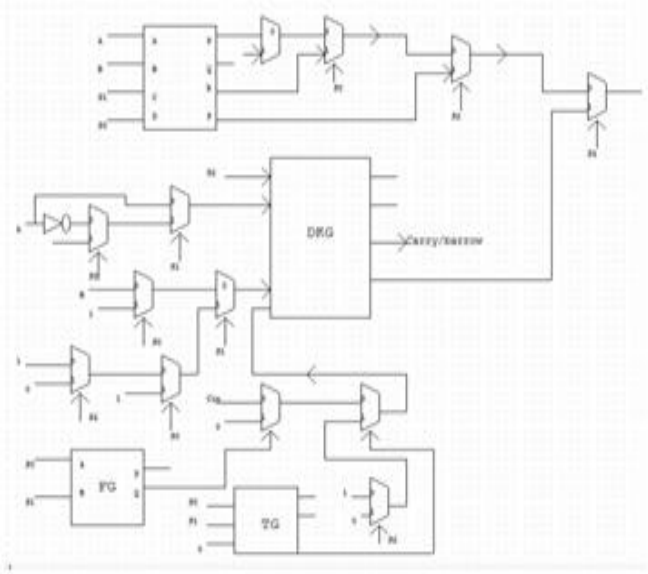

Fig.15. 1st 1-bit ALU

For designing of 16-bit ALU we cascade 16 1-BIT-ALU as shown in the fig 16. We need to note here that only 1st bit has to be added with one for increment and 2's complement or subtracted for decrement. There is slight change for SET and CLEAR operation also. Hence a different 1-BIT-ALU is designed as shown in fig 16 andcascaded from 2nd bit onwards till 16-bit. It is from (A1-A15) in the figure 17.

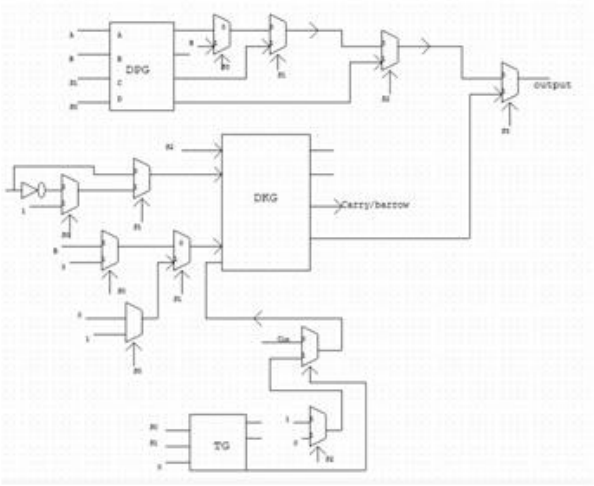

Fig.15. 2nd 1-BIT-ALU

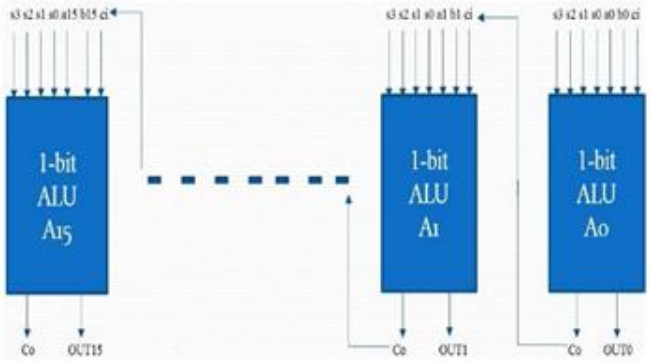

Fig.16. 16-BIT-ALU

V.SIMULATION RESULTS

Shown in Fig.17 is the simulation in QSim waveform simulator for both reversible PFAG and HNG gates and the function of the adder circuits can be verified through the simulations.

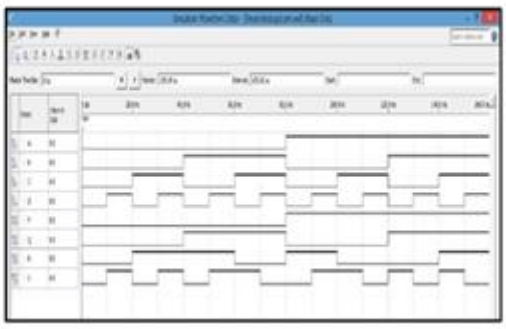

Fig.17: Simulation waveform for reversible full adder.

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Shown in Fig.18 is the output simulation in QSim waveform simulator for both reversible ALU designs. The output simulations satisfy the function Table 1 for A=0 and B=1.

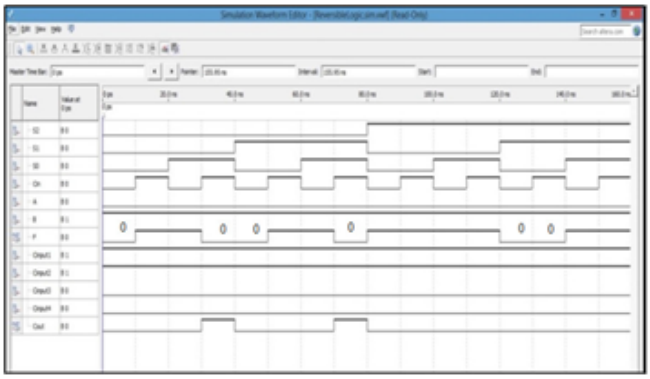

Fig.18: Simulation waveform for reversible ALU design.

The simulation result for code for 16-bit-ALU design written in Verilog and verified in model simaltera 6.6d is shown in fig 19.

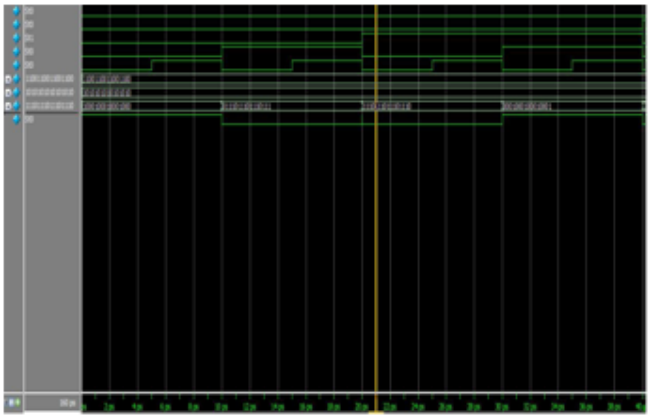

Figure-19. Result for 1st 4-operations (AND, NAND, OR and NOR)

VI.CONCLUSION

In this paper, the reversible ALU design is proposed with two unique design paradigms. The proposed reversible ALU designs are verified using Altera Quartus II software. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results illustrate that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design. This 16-bit reversible Alu is designed and implemented in Verilog using MODEL SIM ALTERA 6.6d. The main aim of the design in this paper is improve the ALU features by increasing it to 15-operations and increase width to 16-bit.

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