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A Low Cost Nine Level Cascaded H-bridge Inverter for High Frequency Distribution System

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ABSTRACT

The multilevel inverter utilization have been increased since the last decade. These new type of inverters are suitable in various high voltage & high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output.. This paper presents a multilevel inverter configuration which is designed by insertion of a bidirectional switch between capacitive voltage sources and a conventional H-bridge module. The modified inverter can produce a better sinusoidal waveform by increasing the number of output voltage levels. By serial connection of two modified H-bridge modules, it is possible to produce 9 output voltage levels including zero. Multicarrier phase-shifted pulse-width modulation method is used to achieve balanced power distribution among the power cells. The analysis of the output voltage harmonics is carried out. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.

Index Terms— Cascaded H-bridge multilevel inverter (CHB), multicarrier pulse-width modulation, phase shifted modulation, total harmonic distortion (THD).

INTRODUCTION

Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns, low switching losses, and high-voltage capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. In this paper, we are using a new topology of cascaded H-bridge multilevel inverter for producing nine output voltage levels and for that we are using multicarrier modulation technique.

PROPOSED SYSTEM

Nine-Level Cascaded H-Bridge Multilevel Inverter

The main disadvantage of the conventional cascaded H-bridge [5] is that when the voltage level increases, the

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number of semiconductor switches increases and also the source required increases. In order to overcome this introduced a new topology of cascaded H-bridge. The main advantage of this topology is that the number of switches required is reduced and also the number of sources. Figure 1 shows the new cascaded five level H-bridge multilevel inverter [6]. It has additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels.

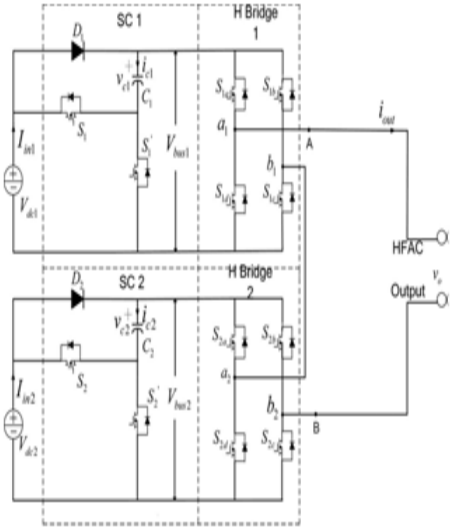

Fig. 1. Circuit topology of cascaded nine-level inverter ($N1 = 2$, $N2 = 2$).

Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter ($N1$ =2, $N2$ = 2), where $S1$, $S2$, S_1 , S_2 as the switching devices of SCcircuits (SC1 and SC2) are used to convert the series or parallelconnection of $C1$ and $C2$. $S1a$, $S1b$, $S1c$, $S1d$, $S2a$, $S2b$, $S2c$, $S2d$are the switching devices of cascaded H-Bridge. $Vdc1$ and $Vdc2$are input voltage. $D1$ and $D2$ are diodes to restrict the currentdirection. $i$out and vo are the output current and the outputvoltage, respectively.It is worth noting that the backend circuit of the proposedinverter is cascaded H-Bridges in series connection. It is significantfor H-Bridge to ensure the circuit conducting regardless ofthe directions of output voltage and current. In other words, HBridgehas four conducting modes in the conditions of inductiveand resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling

TABLE I
RELATIONS OF ON-STATE SWITCHES AND OUTPUT VOLTAGE

Mode 1			Mode 2		
On-state switches	Output voltage	Capacitor State	On-state switches	Output voltage	Capacitor State
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1, S_2$	$4V_{in}$	C_1, C_2 Discharging	$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1, S_2$	$4V_{in}$	C_1, C_2 Discharging
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2$	$3V_{in}$	C_2 Discharging	$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2$	$3V_{in}$	C_2 Discharging
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1' S_2'$	$2V_{in}$	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2$	$2V_{in}$	C_2 Discharging
$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'$	V_{in}	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'$	V_{in}	C_1, C_2 Charging
$S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2'$ or $S_{1c}, S_{1d}, S_{2c}, S_{2d}$	0	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2'$ or $S_{1c}, S_{1d}, S_{2c}, S_{2d}$	0	C_1, C_2 Charging
$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-V_{in}$	C_1, C_2 Charging	$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-V_{in}$	C_1, C_2 Charging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-2V_{in}$	C_1, C_2 Charging	$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2$	$-2V_{in}$	C_2 Discharging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2$	$-3V_{in}$	C_2 Discharging	$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2$	$-3V_{in}$	C_2 Discharging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1, S_2$	$-4V_{in}$	C_1, C_2 Discharging	$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1, S_2$	$-4V_{in}$	C_1, C_2 Discharging

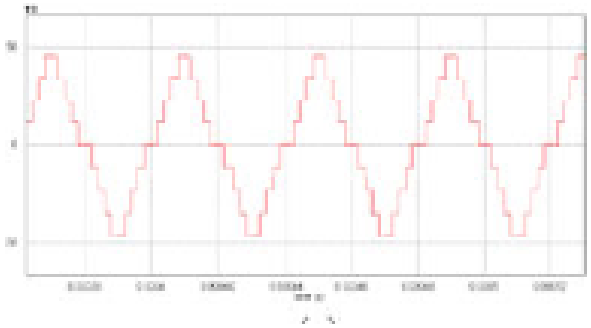

FIG.2. 9-LEVEL WAVE FORM

III.CONTROL STRATEGY

Capacitor Voltage Regulation

In the proposed topology of H-bridge Cascaded multilevel inverter, the dc sources are replaced by capacitors. Thereplaced capacitors must be regulated to a certain voltage in order to have the required voltage level in the outputvoltage of the converter. However, the power system operation and modulation scheme together have different effectson each capacitor so that they are

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not charged and discharged evenly leading to different voltages in each leg of eachphase. To achieve a high quality output voltage waveform, the voltages across all DC capacitors should maintain a constant value.
One challenging problem of the cascade multilevel inverter with a single DC source is the imbalance of the DCcapacitor voltages. The imbalance is caused by:
1) Different switching patterns for different H-bridges.
2) Parameter variations of active and passive components inside H-bridges.
3) Control resolution.

To achieve higher voltage quality, the switching patterns are usually different for different H-bridges in a phase. Thedifferences of switching patterns mean that H-bridges cannot equally share the exchanged power with the power system.

This causes uneven charging of DC capacitors. The parameter variations of components inherently cause different power losses of H-bridges.
The imbalance of DC capacitor voltages will degrade the quality of the voltage output. In severe cases, this could leadto the complete collapse of the power conversion system. Moreover, it will cause excessive voltages across the devices and an imbalance of switching losses. An adequate control strategy for avoiding the imbalance of DC capacitor voltages must meet the following requirements.
1) The impact on voltage quality should be as small as possible.
2) It can balance voltages when components of H-bridges have parameter variations.
3) It can balance voltages when H-bridges switch with different switching patterns.

In the previous topologies, to balance the capacitor voltages, redundant state selection (RSS) is an effective tool in balancing the DC capacitor voltages. In this method the capacitor balancing is going to be achieved by using the proper capacitor in each level in order to get the desired level dictated by SPWM. In each level if the current direction of the phase is tending to charge the capacitors the least charged ones should be used to maintain the desired level and if the current direction tends to discharge the capacitors the most charged capacitors come into play. However, the output
current of the inverter and the time duration of the redundant switching states greatly impact the charging or discharging patterns of the replacement capacitors.

CAPACITOR VOLTAGE REGULATION USING PHASE SHIFT MODULATION

This paper proposes a control method applicable to single dc- source cascaded H bridge multilevel inverters to improve their capacitor voltage regulation. The proposed method, phase shift modulation, is robust and does not incur muchcomputational burden. In this method, the main inverter switches at the fundamental frequency, and the auxiliaryinverter switches at the PWM frequency.

Regulating the capacitor voltage in the auxiliary H-bridge cell is a challenging task. In the method proposed here, capacitor voltage regulation is achieved by adjusting the active power that the main H bridge cell injects into the system. By shifting the voltage waveform generated by the main H-bridge cell to the left or right, one can inject more (or less) active power, which can be used to charge (or discharge) the capacitor on the auxiliary cell.

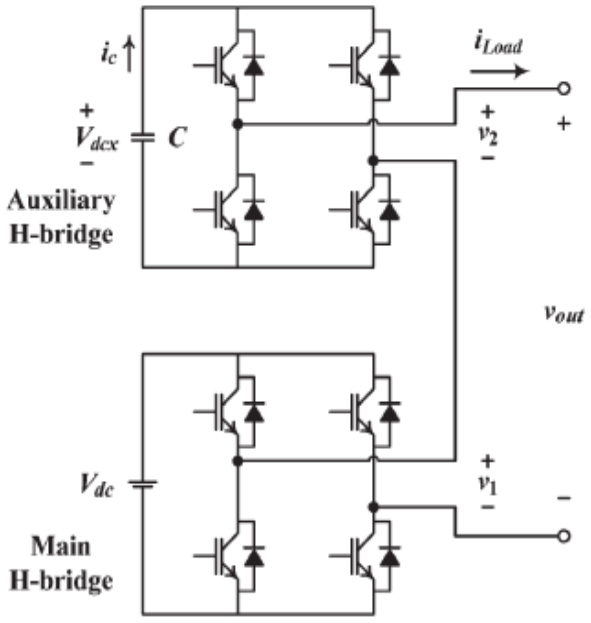

Fig. 3. Block diagram of a cascaded H-bridge inverter.

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The main H-bridge cell, which is supplied by *V*dc, generates a rectangular waveform (*v*1), the frequency of which equals that of the desired output voltage. Furthermore, the width of this rectangular waveform is chosen in such a way that the amplitude of its fundamental harmonic also equals that of the desired output voltage. In other words

$$\alpha = \cos{-1}(\pi Vm/\, 4Vdc)$$

Where α is the conduction angle of the main H-bridge cell From the phase shift modulation of cascaded multilevel inverter, the real power flow capacitor voltages are balanced by adjusting the phase of the waveform.

IV.SIMULATION RESULTS

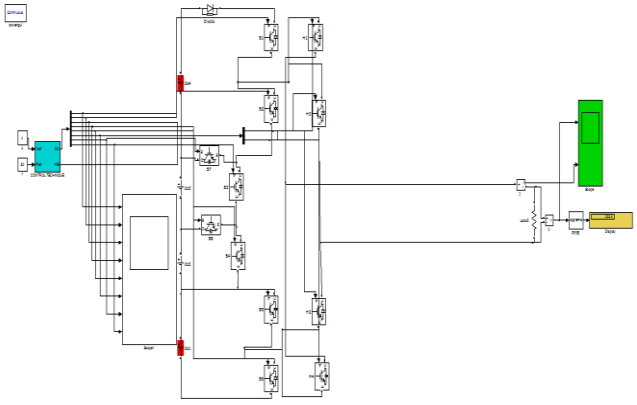

Fig.4 Simulation circuit

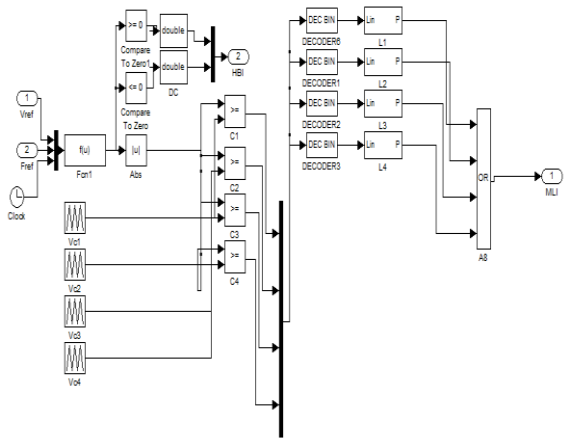

Fig.5 Control block

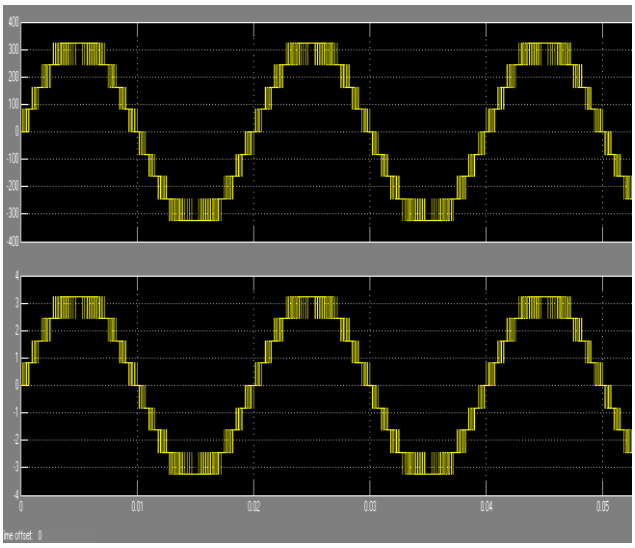

Fig.6 9 level output voltage & current

V. CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. This project deals with the design and implementation of single-phase nine-level Cascaded H-bridge multilevel inverter for RL load with multicarrier phase-shifted PWM modulation method. The simulation of 9-level cascaded H-bridge is done. Along with it, it's harmonic analysis was done. The simulation results shows that the developed nine-level Cascaded H-bridge Multilevel inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion and the THD obtained is 13.01%.

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