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# Implementation of Low Power and Efficient Fault Coverage Circuit with LFSR Design

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## Abstract:

Test Pattern generation has long been carried out by using Linear Feedback Shift Registers (LFSR's). LFSR's are a series of flip-flop's connected in series with feedback taps defined by the generator polynomial. The seed value is loaded into the outputs of the flip-flops. The only input required to generate a random sequence is an external clock where each clock pulse can produce a unique pattern at the output of the flip-flops.This random sequence at the output of the flip-flops can be used as a test pattern. The number of inputs required by the circuit under test must match with the number of flip-flop outputs of the LFSR. To reduce the power by maintaining the fault coverage in this project,three intermediate patterns between the random patterns is generated. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

## Keywords:
FPGA, BIST, LP-LFSR, Switching activity.

## I.INTRODUCTION:

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC.

Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test. In general, the power dissipation of a system in test mode is more than in normal mode [2]. Four reasons are blamed for power increase during test [3]. Real time imaging processes require intensive scientific computations for Digital Signal Processing (DSP). Fast and efficient parallel multipliers are required for DSP, General Purpose Signal Processing (GPSP) and application specific architecture for DSP. DSP algorithm implementation demands using Application Specific Integrated Circuits (ASICs); costs for ASICs are high as well as algorithms should be verified and optimized before realization. The contemporary Field Programmable Gate Arrays (FPGAs) have emerged as a platform for efficient hardware implementation of such complex and computation intensive algorithms.

•High switching activity due to nature of test patterns
•Parallel activation of internal cores during test
•Power consumed by extra design-for-test(DFT) circuitry
•Low correlation among test vectors

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. Built-In Self-Test (BIST) is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip.

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BIST is well known for its numerous advantages such as at-speed testing and reduced need for expensive external automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit). On the observation side, a multiple input signature register (MISR) compacts test responses received from primary outputs or scan chain outputs. Unfortunately,BIST-based structures are very vulnerable to high-power consumption during test. Test vectors, applied to a circuit under test at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern.The rest of the paper is organized as follows. In section II, previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII, the implementation details and the results are presented. Section VIII summarizes the conclusion.

## II. REVIEW OF PREVIOUS WORK:

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. For linear feedback shift register (LFSR), Giard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched [7]. S.K. Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce the average and peak power of a circuit during test [4]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR). Modifying the LFSR by adding weights to tune the pseudorandom vectors for various probabilities decreases energy consumption and increases fault coverage [7], [8].

A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [9]. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used to generate random single input charge sequences [9 & 10]. In [10 &11], it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5], it is proposed that 2m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

## II. BIST approach:

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a

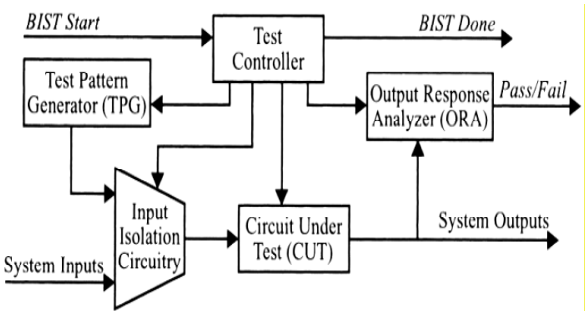


**Figure 1. BIST Basic block diagram**

counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR]. The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation[5]. It causes excessive power dissipation and results in delay penalty into the design[6].

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## BIST PATTERN GENERATION:

The following hardware pattern generation approaches have been used.
1. ROM. One method is to store a good test pattern set (from an ATPG program) in a ROM on the chip, but this is prohibitively expensive in chip area.
2. Linear Feedback Shift Register (LFSR) to generate pseudo-random tests. This frequently requires a sequence of 1 million or more tests to obtain high fault coverage, but the method uses very little hardware and is currently the preferred BIST pattern generation method.
3. Binary Counters. A binary counter can generate an exhaustive test sequence, but this can use too much test time if the number of inputs is huge.
4. Modified Counters. Modified counters have also been successful as test-pattern generators, but they also require long test sequences.
5. LFSR and ROM. One of the most effective approach is to use an LFSR as the Primary test mode, and then generate test patterns with an ATPG program for the faults that are missed by the LFSR sequence. These fe additional test-patterns can either be stored in a small ROM on the chip for a second test epoch, they can be embedded in the output of the LFSR, or they can be embedded in a scan chain in order to augment the stuck fault coverage to 100%.
6. Cellular Automaton. In this approach, each pattern generator cell has a few logic gates, a flip-flop, and connections only to neighboring gates. The cell is replicated to produce the cellular automaton.

## A.Classification of test strategies:

1. Weighted Pseudorandom: Testing: In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.
2. Pseudo exhaustive Testing: Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.
3. Pseudorandom Testing: Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.
4. Exhaustive Testing: Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT). It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.
5. Stored Patterns: Stored-pattern approach tracks the pre generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

## IV.Linear Feedback Shift Registers (LFSRs):

Linear feedback shift register (LSFR) is a shift register whose input bit is a linear function of its previous state. The only linear function of single bits is XOR, thus it is a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value flops. The initial value of the LFSR is called the seed, and the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. The seed is used to generate a test pattern and their corresponding test cube. Reseeding is a very powerful method for reducing test data. Most of the test data reduction is mainlyconcentrating on LFSR reseeding. The basic idea inLFSR reseeding is to generate deterministic test cubes by expanding seeds. A seed is an initial state of the LFSR that is expanded by running the LFSR in autonomous mode. An LFSR generates periodic sequence must start in a non-zero state, The maximum length of an LFSR sequence is 2n -1 does not generate all 0s pattern.

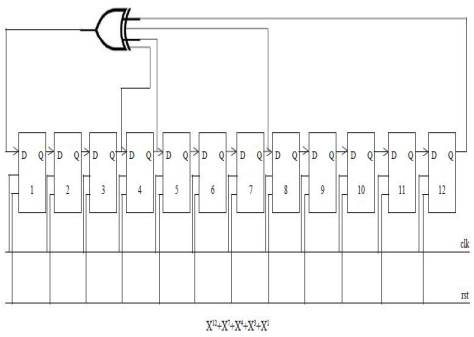


Fig 2 LFSR 12bit circuit

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To focus on reducing test pattern with effective Linear Feedback Shift Register (LFSR) reseeding. LFSR is a good pseudorandom pattern generator which generates all possible test vectors with the help of the tap sequence. It can achieve high fault coverage by reducing correlation between the test vectors. Reseeding is a powerful method for reducing the test data volume and storage. This study presents a new LFSR reseeding technique for efficient reductionof test pattern. A new encoding technique is proposed in this study which is used to reduce the size of the test data. Size of the test data can be reduced by LFSR clock which is inactive for several clock cycles after the input seed is given When the clock goes to inactive state, a rotate right shift operation is done on the seed to get all the remaining possible values. After getting all the possible values for that seed a new seed is given by making the clock active. Test data volume is reduced by storing the data only when the clock is active. With in the reduced clocks, rest of all the remaining test vectors was derived. A special Control logic is used to make the clock active as well as inactive.

## GENERATION OF PRIMARY INPUT SEQUENCE

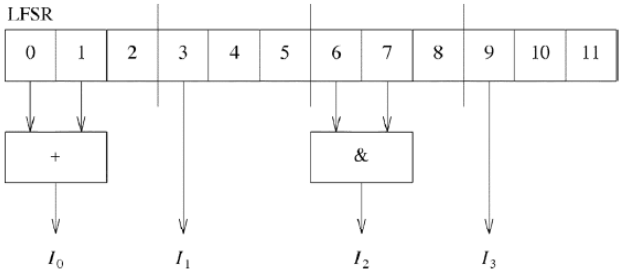
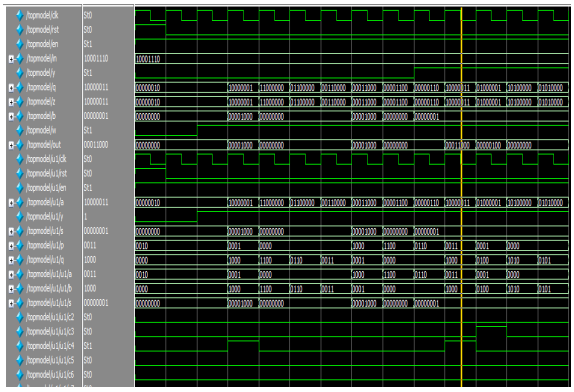


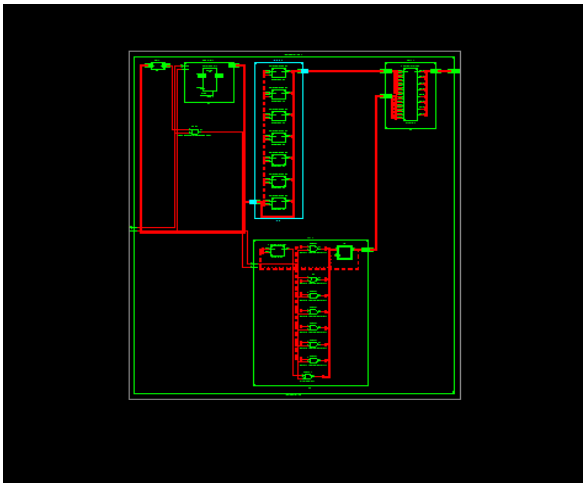

**Fig 3 Diagram for Primary Input Sequence**

The 12-bit LFSR is shown at the top of Fig. Bits0, 1 and 2 of the LFSR are used for producing the values of I0. The OR gate is driven by bits 0 and 1 of the LFSR. Bit 2 of the LFSR reduces the dependencies between the values of I0 and the values of I1. Bits 3, 4, and 5 of the LFSR are used for producing the values of I1 . Therefore,I1 is driven directly by bit 3of the LFSR. Bits 4 and 5 reduce the dependencies between the values of I1 and the values of I2.Bits 6, 7, and 8 are used for producing the values of I2. The AND gate is driven by bits 6 and 7. Bit 8 of the LFSR reduces the dependencies between the values of I2and I3.Finally, bits 9, 10, and 11 are used for producing the valuesof I3. Therefore, I3 is driven directly by bit 9 of the LFSR.

## V. IMPLEMENTATION AND RESULTS:

The proposed low power linear feedback shift register [LP-LFSR] designed using Verilog hardware description language and structural form of coding. The proposed system simulation results are as follows





## CONCLUSION & FUTURE SCOPE:

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns.

Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

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## REFERENCES:

[1] BalwinderSingh, Arun khosla and Sukhleen Bindra "Power Optimization of linear feedback shift register(LFSR) for low power BIST" , 2009 IEEE international Advance computing conference(IACC 2009) Patiala,India 6-7 March 2009.

[2] Y.Zorian, "A Distributed BIST control scheme for complex VLSI devices," Proc. VLSI Test Symp., P.4-9,1993.

[3] P.Girard," survey of low-power testing of VLSI circuits," IEEE design and test of computers, Vol. 19,no.3,PP 80-90,May-June 2002.

[4] Mechrdad Nourani,"Low-transition test pattern generation for BIST- Based Applications", IEEE TRANSACTIONS ON COMPUTERS, Vol57,No.3 ,March 2008.

[5] BOYE and Tian-Wang Li," A novel BIST scheme for low power testing," 2010 IEEE.

[6] R.S.Katti,X.Y.Ruan , and H.Khattri," Multiple-Output Low-Power Linear feedback shift register design," IEEETrans.circuitsSyst.I,Vol.53,No.7,pp-1487-1495,July 2006.

[7]P.Girard,L.Guiller,C.Landrault, S.Pravossoudo vitch,and H.J.Wunderlich," A modified clock scheme for a low power BIST test pattern generator," 19th IEEE proc. VLSI test Symp.,CA,pp-306- 311,Apr-May 2001.

[8] S.Wang and S.K.Gupta," DS-LFSR: a BIST TPG for low switching activity," IEEE Trans.computer-aided design of Integrated circuits and systems, Vol. 21,No.7,pp.842-851,July 2002.

[9] I.Voyiatzis,A.paschalis,D.Nikolos and C.Halatsis, "An efficient built-in self test method for robust path delay fault testing," Journal of electronic testing: Theory and applications Vol.8,No.2,pp-219-222,Apr-1996.

[10] S.C.Lei, J.Guo, L.Cao, Z.Ye.Liu, and X.M.Wang,"SACSR: A low power BIST method for sequential circuits,: Academic Journal of XI'AN jiaotongun iversity(EnglishEdition),Vol.20,no.3,pp.155- 159,2008.

[11] R.H.He,X.W.Li and Y.Z.Gong," A scheme for low power BIST test pattern generator," micro electronics & computer,no.2,pp.36-39 Feb.2003.

[12] S.C. Lei, X.Y.Hou ,Z.B.Shao and F.Liang," A class of SIC circuits: theory and application in BIST design," IEEE trans. circuits syst. II,