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A Novel Control Method of Multiband Hysteresis Modulation for Multilevel Inverter Applications

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Abstract:

In this paper, a frequency-domain method isproposed for the determination of net hysteresis bandwidth fora given desired maximum switching frequency of the inverter. A hierarchical switching algorithm has beensuggested for the modular cells of the cascaded multilevel inverter.a generalized multiband hysteresismodulation and its characterization have been proposed for thesliding-mode control of cascaded H-bridge multilevel-inverter(CHBMLI)-controlled systems.A smaller hysteresis band gives fast dynamic performanceand accurate tracking characteristics. However, a smallerhysteresis band also leads to a high switching frequency.

Key words:
Multilevel inverter, multiband hysteresis modulation, static compensator.

I.INTRODUCTION:

There are various current control methods for two-level converters. Hysteresis control of power converters, based oninstantaneous current errors, is widely used for the compensationof the distribution system as it has good dynamiccharacteristics and robustness against parameter variations and load non-linearties.The cascaded H-bridge multilevel-inverter (CHBMLI) configuration has the advantage of its simplicity and modularity overa diode-clamped multilevel inverter or a flying-capacitor multi-levelinverter. Various improved modulation schemeshave been proposed for CHBMLI in the recent past. The complexities involved in the modulation of multilevelinverter under closed loop depend upon the number of levelsused and the topology of the cascaded multilevel inverter.

Applications of sliding-mode controlfor high-voltage and high-power applications require multilevel inverters or parallel inverters as VSIs. Severalmodulation methods have been proposed in the past for thecontrol of multi-level inverters under sliding mode.The hysteresis-based instantaneous method of control has beenwidely used for sliding-mode-controlled two-level inverters. The switching frequencies of high-power converters are limitedby the switching losses. The VSI needs to operateat finite maximum switching frequency in these high-powerconverters. The switching characterizationof VSI is an important requirement for the suitable design ofpower circuit and thermal management.Sliding-mode control is an important closed-loopmodulation being used for ac-load-voltage-control applicationsusing dc–ac converters. Examples include uninterruptible powersupplies, ac power supplies, and distribution static compensators(DSTATCOMs).

II.DSTATCOM:

The distribution system consists of a load that is suppliedfrom voltage source vs through a feeder (Rs, Ls), as shown inFig. 1. DSTATCOM consists of a VSI that is connected to theload through an interfacing inductance LT. Resistance RT representsthe equivalent resistance in the shunt path. Voltage Vdcrepresents the net dc-link voltage of the VSI. Filter capacitorCf is connected in the shunt. The currents flowing through thedifferent branches are source current is, load current il, currentthrough the filter capacitor icf, inverter output current iin, andcurrent injected in the shunt branch ish. The net controllablevoltage at the output of the VSI is uVdc, where u is definedas the control input and represents the switching logic ofthe inverter. It assumes discrete values between −1 and +1,depending upon the number of levels of the VSI, e.g., −1, −1/2,0, +1/2, and +1, for a five-level inverter.

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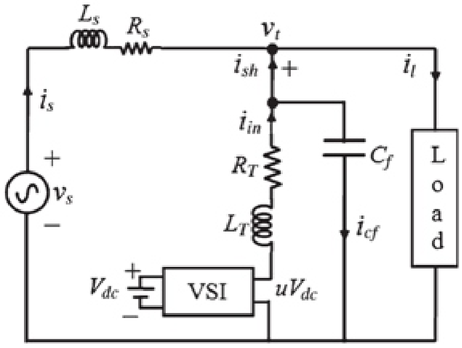

Fig 1: Equivalent circuit of compensator.

The switches used in the VSI need to be fully rated and operate at very high switchingfrequency for ideal sliding-mode control,. A multiband hysteresis modulation using a cascadedmultilevel inverter will be discussed hereinafter so as to bringthe device ratings into the limits of practical insulated-gatebipolar-transistor (IGBT) switches with the desired maximumswitching frequency.

III.CASCADED MULTILEVEL INVERTER:

Fig. 2shows a general n-level (n = 3, 5, 7. . .) cascaded multilevelinvertertopology. The basic building block of the cascadedinverter is an H-bridge.The switches Sw11, Sw12, . . . , SwN4shown in Fig. 2 represent an IGBT with an antiparallel diode.The number of such H-bridges required for an n-level inverteris N = (n − 1)/2. For higher voltage/power-rating applications,the switching frequency and device ratings are limited.Therefore, it is desirable to distribute the voltage and powerstress among the number of devices. For an n-level inverter, thevoltage stress on the semiconductor switches and the dc-linkcapacitor is 1/N times the net dc-link voltage Vdc required.

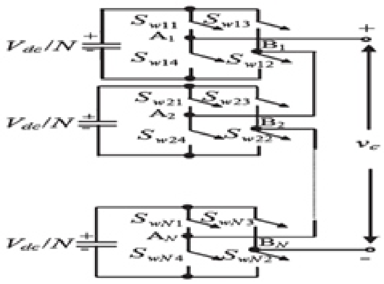

Fig 2: Cascaded n-level inverter

Five-Level Modulation:

For a five-level modulation, two H-bridges are required, asshown in Fig. 4(a). The corresponding multiband hysteresismodulation is shown graphically in Fig. 4(b). The detailed control algorithm for a five-level inverter basedon the multiband hysteresis modulation is described.

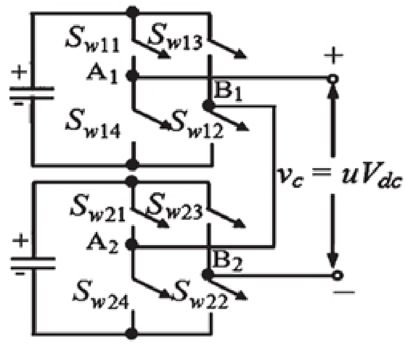

Fig 3: Five-level modulation

With this scheme, the modulator has five levels of output, i.e.,u = −1, −1/2, 0, +1/2, and +1. The time-domain representationof five-level hysteresis modulation, showing switchingfunction se(t) and five-level switching logic u(t).

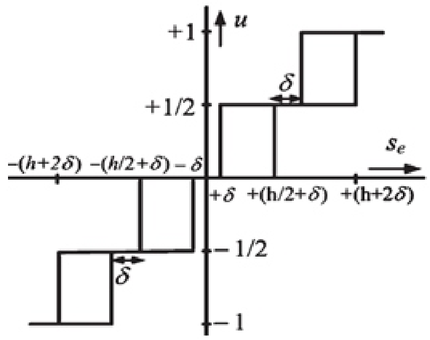

Fig 4: Multiband hysteresis modulation.

Hierarchical Switching strategy:

Aswitching scheme is proposed to follow the algorithm given for obtaining the five-level output, which can easily be extended to the further higher level inverter. The scheme leadsto a unique switching pattern corresponding to each level in theoutput. In this scheme, the switching stress of all the switchesof the same H-bridge is equal. For the five-level modulationdiscussed in the previous section, the following two hierarchies are chosen. Under steady-state condition, switching function se variesat the fundamental frequency. Therefore, the left-leg switchesoperate at this frequency for the positive half-cycle. The right-leg switches of the H-bridges, i.e., Sw13, Sw12,Sw23, and Sw22, operate at high switching frequency for thepositive half-cycle of switching function se, following themultiband hysteresis modulation.

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Each hierarchical bridge willoperate for that corresponding level of the output only. Theposition of switches in the other H-bridge will remain fixed inthis period.The hierarchical switching scheme can easily be extended toany higher level inverter modulation. For an n-level inverter,there are N hierarchical H-bridges. Each is assigned as level-3,level-5 . . . or level-n H-bridge.

IV.CONVENTIONAL SINGLE-PHASE SYSTEM:

The multilevel modulationand sliding-mode control proposed in the previous sectionsare verified for the operation of single-phase DSTATCOMusing a five-level cascaded inverter.The load is assumed to be a nonlinear rectifiertype with input impedance (Llac,Rlac). The output dc voltageof the full-bridge rectifier is fed to a resistive load Rldc supportedby a parallel dc capacitor Cldc. The single-phase nonlinear load draws fundamental, third order,and higher order harmonic components. As DSTATCOMregulates the PCC voltage to a 50-Hz sinusoid, any harmoniccomponent that is present in the nonlinear load must comefrom the compensator while controlling the voltage at the PCC.This is the reason for the presence of third and higher orderharmonic components, along with the switching components, in addition to the fundamental component.

Simulation results:

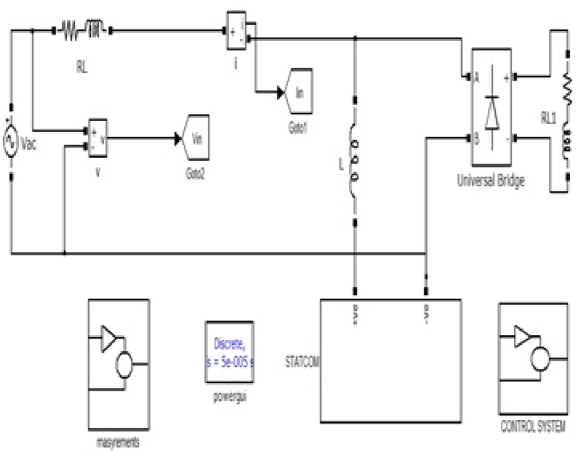

Fig 5: simulation design of 1-phase system

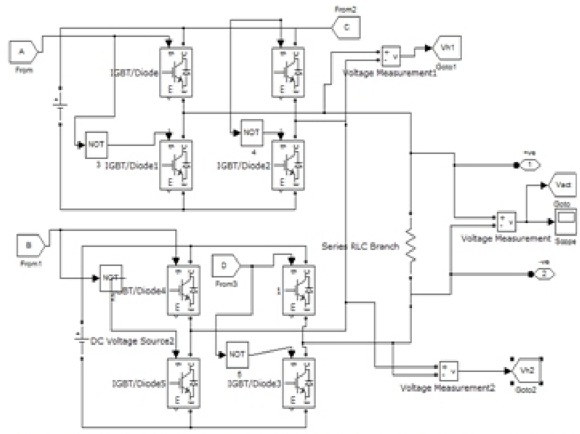

Fig 6: STATCOM design for 1-phase system

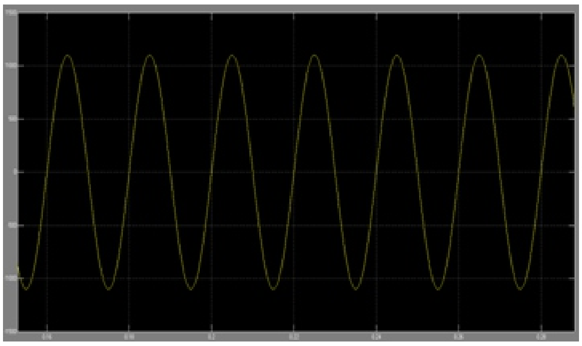

Fig 7: input voltage

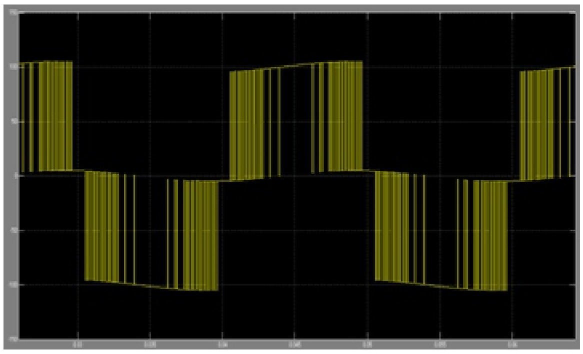

Fig 8: output voltage of H-bridge 1.

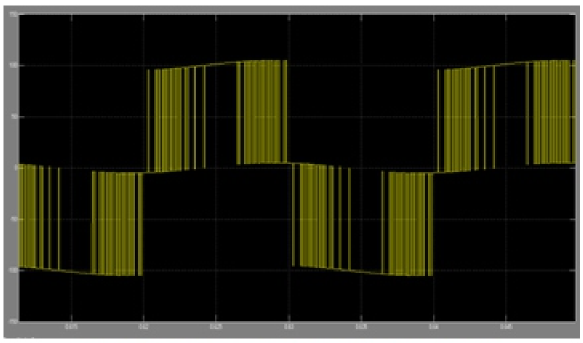

Fig 9: output voltage of H-bridge 2.

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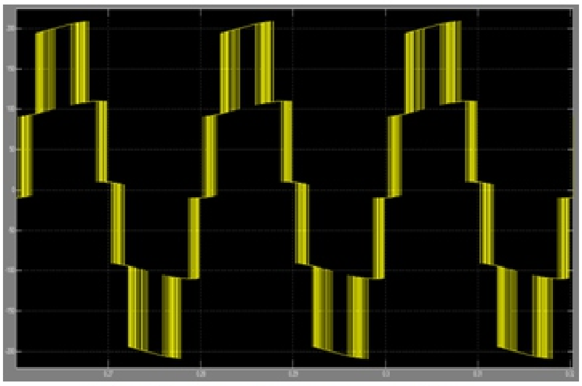

Fig 10: five-level output voltage

V.PROPOSED THREE-PHASE SYSTEM:

A five-level cascaded H-bridge topologyis used in DSTATCOM for a three-phase four-wire distribution system. The VSI requires a cascaded connection of two H-bridges for each of phases a, b, and c, for thefive-level inverter. Switches Swa11, Swa12, Swc24, represent an IGBT with an antiparalleldiode. The dc-link voltages for each H-bridge are representedby Vdca1, Vdca2, and Vdcc2 across dc-link capacitorsCdca1, Cdca2, Cdcc2, respectively. The output voltages foreach phase are cascaded at terminals Aa1Ba1−Aa2Ba2 forphase a, Ab1Bb1−Ab2Bb2 for phase b, and Ac1Bc1−Ac2Bc2for phase c. A common neutral ns from all the three phases isconnected to the system neutral (fourth wire).

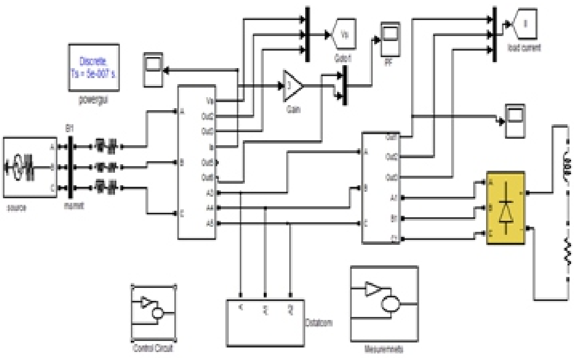

Fig 11: proposed three-phase system

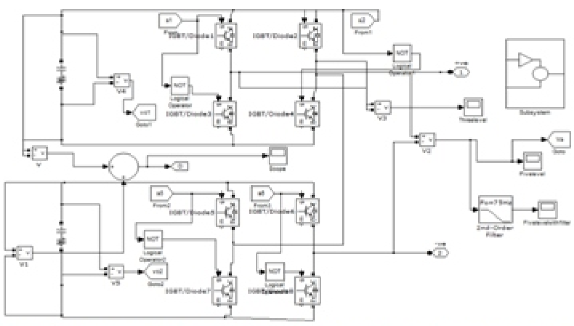

Fig12: cascaded multilevel inverter for phase A.

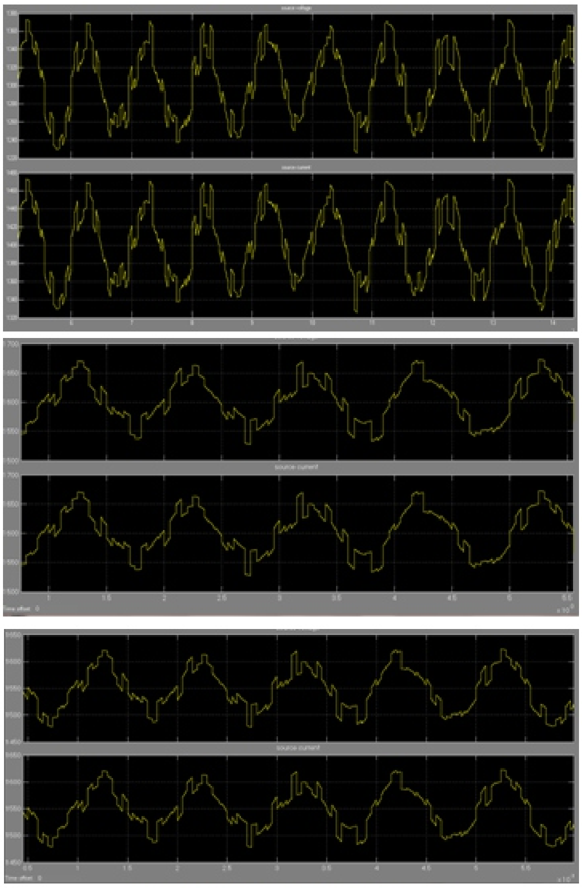

Fig 13: DC-link voltages

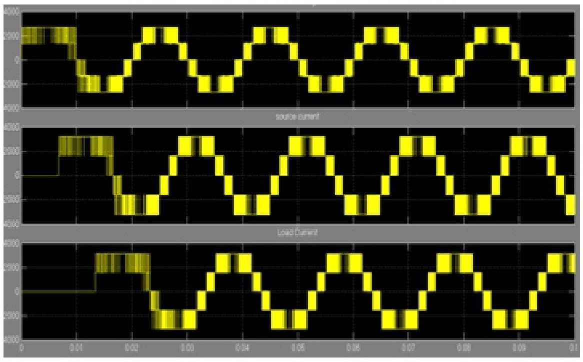

Fig 14: Five-level-inverter outputvoltages of three phases.

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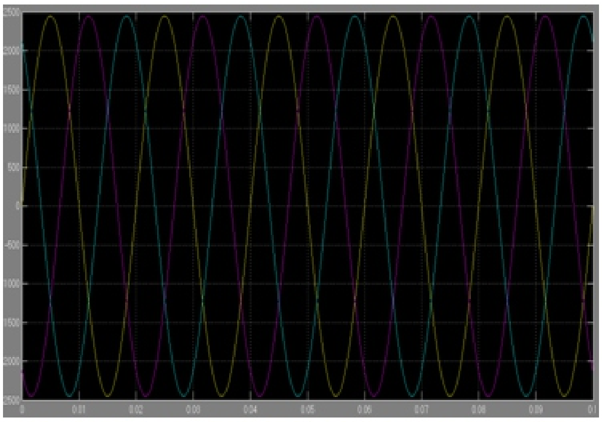

Fig 15: Voltage tracking characteristics of three phases.

A permanent magnet synchronous motor has been connected to at the load for verification of the system under machine load condition. The rotor speed of the PMSM is shown in fig 16.

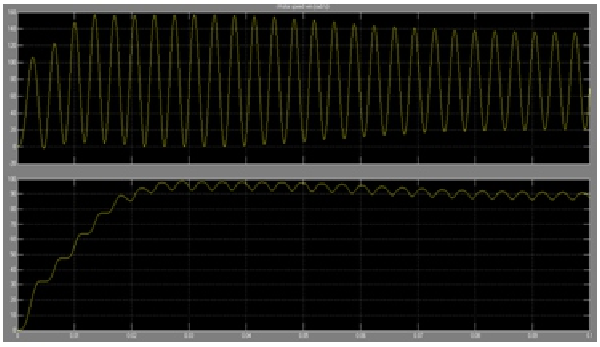

Fig 16: rotor speed of the PMS motor

VI.CONCLUSION:

The multiband hysteresis modulation proposed in this paper hasshifted the switching components toward higher frequenciesand has hence reduced the switching ripple content in theoutput controlled voltage.The proposed frequency-domain method of switching characterizationfor CHBMLI has estimated accurately the hysteresisbandwidth for the desired maximum switching frequency.The simulation verification of the derivedresults have been provided through a single-phase DSTATCOMmodel.

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