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Design and Implementation of Fault Coverage Circuits for All VLSI Elements

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Abstract:

A new fault coverage test pattern generator using a linear feedback shift register (LFSR) called FC-LFSR can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

Keywords:

LFSR, Optimization, Low Power, Test Pattern Generation, BIST.

INTRODUCTION:

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing [1]. Power dissipation is a challenging problem for today"s System-on-Chips (SoCs) design and test. The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small.

The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to 1. During switching, the power is consumed due to the short circuit current flow and the charging of load capacitances is given by equation:

$$P = 0.5VDD\ E\ (sw)\ CLFCLK \quad (1)$$

Where VDD is supply voltage, E(sw) is the average number of output transitions per 1/ FCLK, FCLK is the clock frequency and CL is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. Low correlation between consecutive test vectors (e.g. among pseudorandom patterns) increases switching activity and eventually power dissipation in the circuit. The same happens when applying low correlated patterns to scan chains. Increasing switching activity in scan chain results in increasing power consumption in scan chain and combinational block. The extra power (average or peak) can cause problems such as instantaneous power surge causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yield and lifetime. Large and complex chips require a huge amount of test data and dissipate a significant amount of power during test, which greatly increases the system cost. There are many test parameters should be improved in order to reduce the test cost. Parameters include the test power, test length (test application time), test fault coverage, and test hardware area overhead Automatic test equipment (ATE) is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. External testing using ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases. As the complexity of modern chips increases, external testing with ATE becomes extremely expensive.

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Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits since overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE.BIST perform self-testing and reducing dependence on an external ATE. BIST is a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster, more efficient and less costly. The important to choose the proper LFSR architecture for achieving appropriate fault coverage and consume less power. Every architecture consumes different power for same polynomial.

LFSR:

In computing, a linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state.The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. Both hardware and software implementations of LFSRs are common.The mathematics of a cyclic redundancy check, used to provide a quick check against transmission errors, are closely related to those of an LFSR.

Applications of LFSR:

•Pattern generator,
•Low power testing,
•Data compression, and
•Pseudo Random Bit Sequences (PRBS).

IV. BIST ARCHITECTURE:

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external ATE.Recently, techniques to cope with the power and energy problems during BIST have appeared. A brief overview of these techniques is given in Section 2. In this paper, we address the low power testing problem in BIST. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for automatic test equipment, and support during system maintenance. Moreover, with the emergence of core-based SOC designs, BIST represents one of the most favorable testing method since it allows to preserve the intellectual property of the design. In most complex SOC designs characterized by very poor controllability and observability, BIST is even probably the only practical solution for efficient testing.

A.Implementation of BIST:

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, it has been demonstrated in [5] that the switching activity in a time interval (i.e. the average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs (see above description in part 2.2). Among these techniques, the DS-LFSR proposed in [5] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG.

Inputs driven by the slow LFSR are those which may cause more transitions in the circuit. Although this technique reduces the average power consumption while maintaining a good fault coverage level, the peak power consumption cannot be reduced in practice (a full bit changing may occur at circuit inputs every d clock cycles where d = normal clock speed / slow clock speed). This point represents a severe limitation of the method as the peak power consumption is a critical parameter that determines the electrical limits of the circuit and the packaging requirements. A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit as shown in figure 1.

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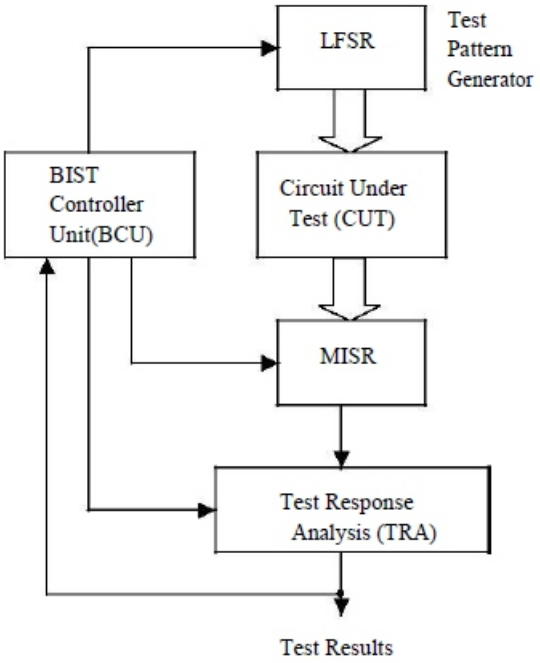

BIST Architecture:

CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output.Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching"s and power dissipation in test mode.

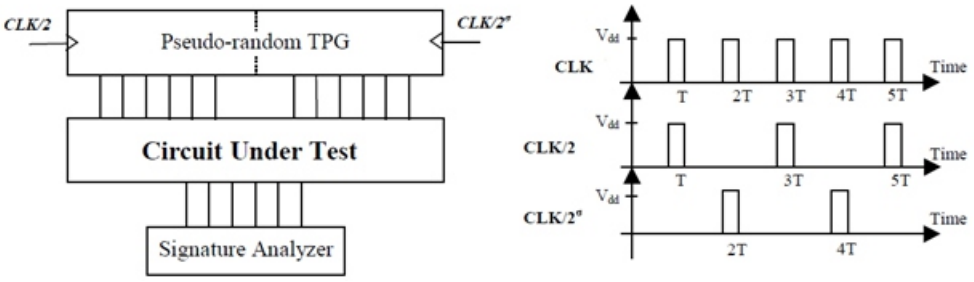

Figure 1: Basic scheme of the low power test pattern generator

The low power TPG :

The idea behind the use of such a low power TPG is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. Let us consider a CUT with n primary inputs. A n-stage primitive polynomial LFSR with a clock CLK would be used in a conventional pseudorandom BIST scheme. Here, we use a modified LFSR composed of n D-type flip-flops and two clocks CLK/2 and CLK/2_ , and constructed as depicted in Figure 2 (n=6 in the example of Figure 2).

As one can observe, this modified LFSR is actually a combination of two n/2-stage primitive polynomial LFSRs, each of them being driven by a single clock CLK/2 or CLK/2_ . The D cells belonging to the first LFSR (referred to as LFSR-1 in the sequel) are interleaved with the cells of the second LFSR (referred to as LFSR-2 in the sequel), thus allowing to better distribute the signal activity at the inputs of the CUT.

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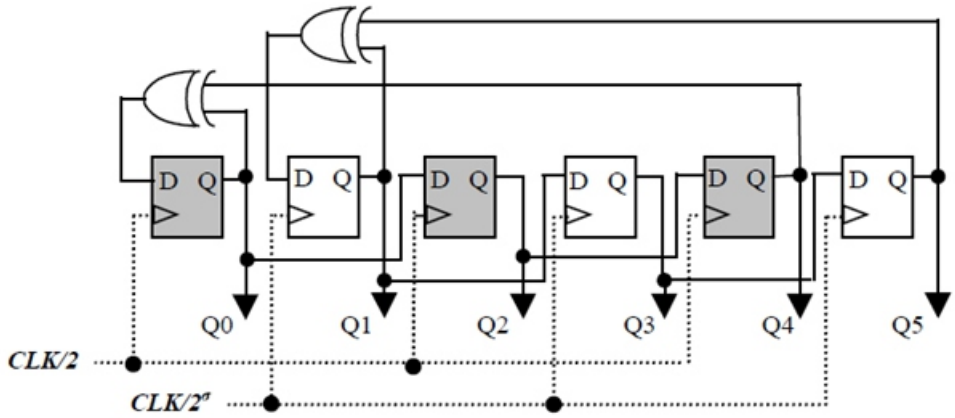

Figure 2: An example of the modified LFSR TPG

In order to better describe the functioning of the low power TPG, the timing diagram of the test sequence generated by the example TPG shown in Figure 2 is reported in Table 1. Assume that the seed <001> has been chosen for both LFSRs, such that the first vector applied to the CUT at time T is <100001>. Only LFSR-1 is active during the first clock cycle (LFSR-2 is in stand-by mode). This is illustrated in the two last columns of Table 1 in which a 8 grey cell represents the active LFSR in the corresponding clock cycle. During the next clock cycle, LFSR-2 is active (LFSR-1 is in stand-by mode) and vector <110000> is applied to the CUT.

A.Implementation of low transition test pattern:

The basic idea behind low power BIST is to reduce the PI activities. The paper proposes a new transition test pattern generation technique which generates three intermediate test patterns between each two consecutive random patterns generated by a conventional LFSR. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI‟s activities and eventually switching activities in the circuit under test. Let us assume that Ti and Ti+1 are two consecutive test patterns generated by a pseudorandom pattern generator (e.g. a conventional LFSR). The new low transition LFSR (LTLFSR) generates three intermediate patterns (Ti1, Ti2 and Ti3) between Ti and Ti+1. The total number of signal transition occurs between these five vectors are equivalent to the number of transition occurs between the two vectors. Hence the power consumption is reduced. Additional circuit is used for few logic gates in order to generate three intermediate vectors.

The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes.The three intermediate vectors (Ti1, Ti2 and Ti3) are achieved by modifying conventional flip-flops outputs and low power outputs.

B.Implementing algorithm for LT-LFSR:

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous, the generating test vector is Ti.

Step2: Both halves are idle First half sent to the output and second half‟s output is sent by the injection circuit, the generating test vector is Ti1.

Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is Ti2.

Step4:Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is Ti3.

After completing step 4 again goes to step1 for generating test vector Ti+1. The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip- flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the R Injection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns.

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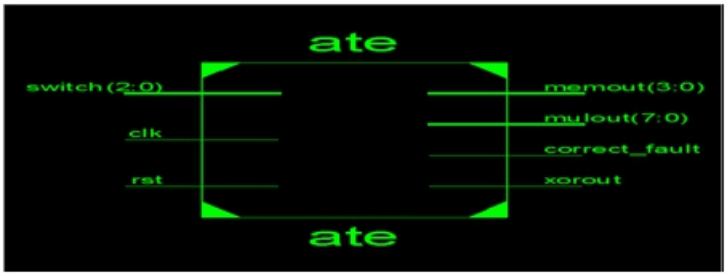
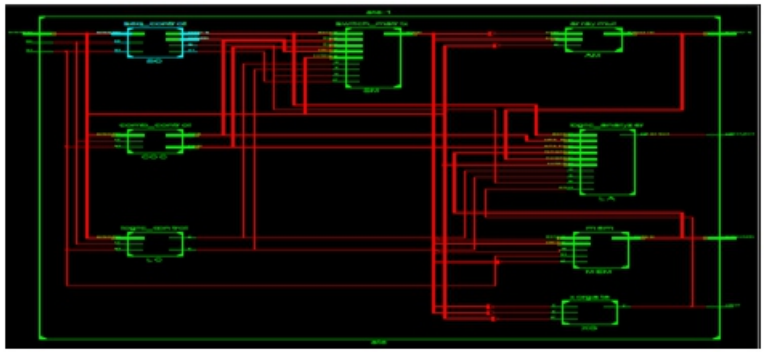
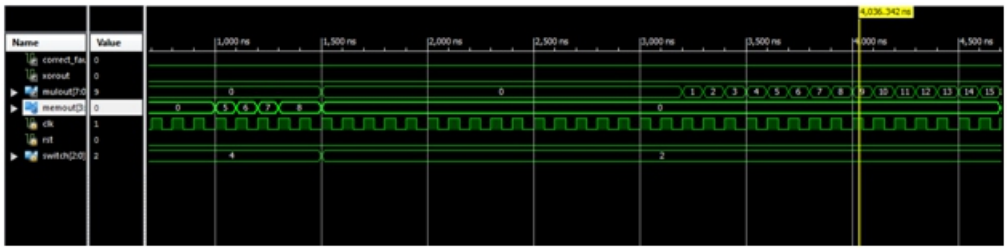
RESULTS



Schematic block diagram of ATE



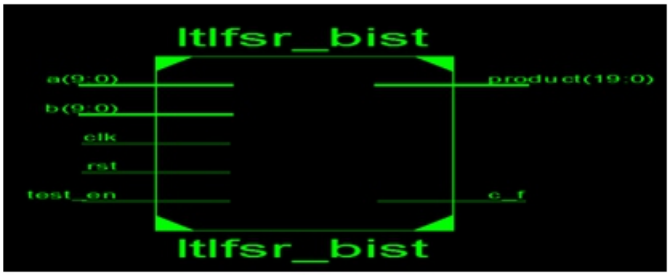
RTL SCHEMATIC OF ATE



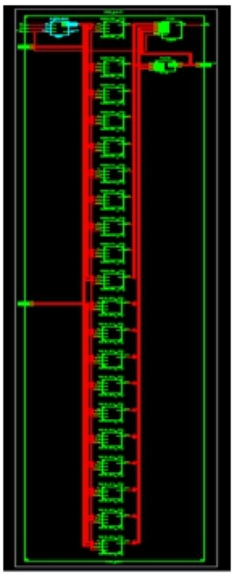
Waveform for ATE

```
Delay:               4.007ns (Levels of Logic = 2)
  Source:            COC/b_3 (FF)
  Destination:       COC/a_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

Delay for ATE



LTLFSR BOLCK DIAGRAM



RTL FOR LTLFSR

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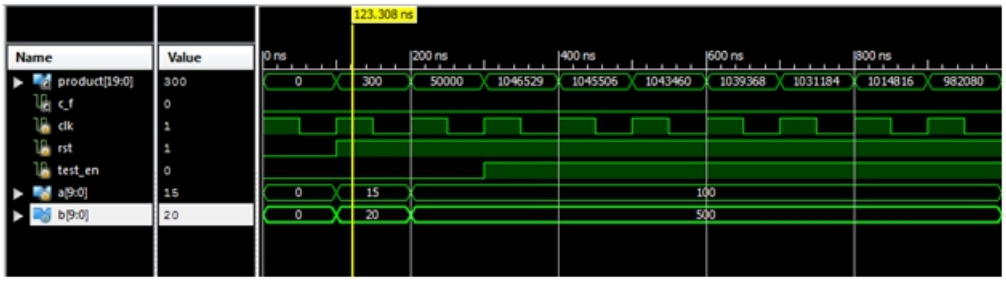
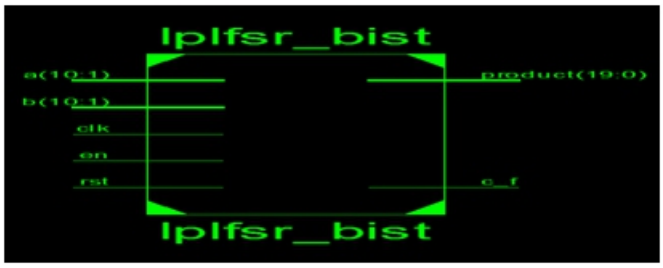


LTLFSR WAVEFORM

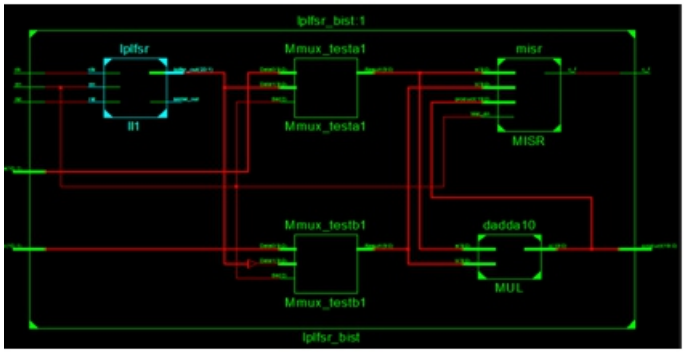
```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.269ns (Maximum Frequency: 440.723MHz)
   Minimum input arrival time before clock: 4.695ns
   Maximum output required time after clock: 34.295ns
   Maximum combinational path delay: 35.042ns
```

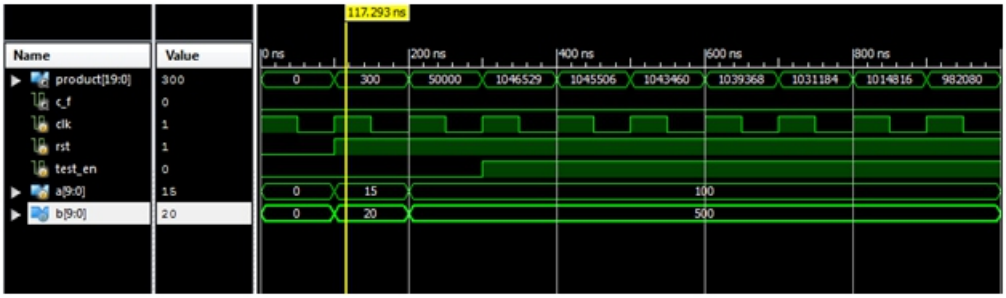
DELAY FOR LTLFSR



BLOCK DIAGRAM OF LPLFSR



RTL SCHEMATIC OF LPLFSR



WAVEFORM OF LPLFSR

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.812ns (Maximum Frequency: 355.568MHz)
   Minimum input arrival time before clock: 4.404ns
   Maximum output required time after clock: 27.857ns
   Maximum combinational path delay: 27.779ns
```

DELAY FOR LPLFSR

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CONCLUSION:

The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR. Comparisons of the number of test patterns (NP) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomial-independent. The required number of patterns provides target FC does not quadruples, and preserving randomness.

By using this low transition test pattern generator using LFSR for Test Pattern Generation (TPG) technique we conclude that power dissipation is reduced during testing. The transition is reduced by increasing the correlation between the successive bits, reduces the average and peak power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the PI activities, average and peak power of combinational and sequential circuits during the test mode with do not effect on FC.