

Implementation of Novel High Radix Multiplier Using KOGGE Stone Adder

P. Naresh
 M.Tech (VLSI-SD)
 Department of ECE
 Teegala Krishna Reddy
 Engineering College, (Meerpet),
 Hyderabad.

Ms. B. Ramya
 Assistant professor
 Department of ECE
 Teegala Krishna Reddy
 Engineering College, (Meerpet),
 Hyderabad.

Dr.P.Ram Mohan Rao
 FIE,CE(I), MISTE, MISH,
 MISCEE, MASCE(I), MISNT
 Principal,
 TKREC, (Meerpet),
 Hyderabad.

ABSTARCT

Higher radix values of the form $r = 2r$ have been employed traditionally for recoding of multipliers, and for determining quotient- and root-digits in iterative division and square root algorithms, usually only for quite moderate values of r , like 2 or 3. For fast additions, in particular for the accumulation of many terms, generally redundant representations are employed, most often binary carry-save or borrow-save, but in a number of publications it has been suggested to recode the addends into a higher radix. It is shown that there are no speed advantages in doing so if the radix is a power of 2, on the contrary, there are significant savings in using standard 4-to-2 adders, even saving half of the operations in multi-operand addition.

Keywords: *asymmetric high-radix signed-digit number, computer arithmetic, number system conversion, redundant number system, signed-digit numbers, VLSI design.*

INTRODUCTION

Addition is the most important and frequently used arithmetic operation in computer systems. Generally, two methods can be used to speed up the addition operation. One is to explicitly shorten the carry-propagation chain by using circuit design techniques, such as detecting the completion of the carry chain as soon as possible, carry look-ahead, etc. [1-3]. Another is to convert the operands from the binary number system to a redundant number system, e.g., the signed-digit number system or the residue number system, so that the addition become carry-free (CF) [2-5]. This

implicitly eliminates the carry-propagation chain so that fast addition can be done, at the expense of conversion between the binary number system and the redundant number system. In this paper we focus on exploring signed-digit (SD) numbers.

tems are defined for any radix $r \geq 3$ and for the digit set $\{-\alpha, \dots, -1, 0, 1, \dots, \alpha\}$, where α is an integer such that $r/2 < \alpha < r$. In an OSD number system, the redundancy index ρ , defined as $\rho = 2\alpha - r + 1$, ranges from the minimal redundancy $r/2 + 1$ to the maximal redundancy $r - 1$. The most important contribution of OSD is to explore the possibility of performing carry-free addition and borrow-free subtraction for fast parallel arithmetic, if enough redundancy is used. The OSD number system was later extended to the *generalized signed-digit* (GSD) number system [6-9]. The GSD number system for radix $r > 1$ has the digit set $\{-\alpha, \dots, -1, 0, 1, \dots, \beta\}$, where $\alpha \geq 0$ and $\beta \geq 0$. The redundancy is $\rho = \alpha + \beta + 1 - r$. So far, the most important contribution of the works on GSD [6-9] include unifying the redundant number representation and sorting the CF addition schemes for the GSD number system according to the radix r and redundancy index ρ . However, ideal single-stage CF addition has not been achieved, though two-stage CF addition has been shown to be doable for any GSD system with $r > 2$ and $\rho > 2$, or with $r > 2$ and $\rho = 2$ provided that $\alpha \neq 1$ and $\beta \neq 1$. For any GSD system with $r = 2$ and $\rho = 1$, or $\rho = 2$ and α or β equals 1, the limited-carry addition must be used.

There are many applications for the SD number representations, most notably in computer and digital signal processing systems. Specifically, the CF adder

has been investigated based on the redundant positive-digit numbers [10] and the symmetrical radix-4 SD numbers [11, 12] for high-speed area-efficient multipliers. The symmetrical radix-2 SD number representation has been used in the implementation of a RSA crypto-graphic chips [13], high-speed VLSI multipliers [14, 15], FIR filters [16], IIR filters [17], dividers [18], etc. Though arithmetic operations using these number representations can be done carry free, they have common difficulty in conversion to and from the binary number representation. Hence, in the past, many researchers have proposed specific architectures for number system conversion [15, 17, 19-22].

In this paper, we present the *asymmetric high-radix signed-digit* (AHSD) number system. The idea of AHSD is not new. A particular AHSD number system was called the radix- r stored-borrow (SB) number system in [7]. Most earlier works have focused on binary stored-borrow (BSB) number systems, where $r = 2$ [6, 14, 23-25]. Instead of proposing a new number representation, our purpose is to explore the inherent CF property of AHSD. The CF addition in AHSD is the basis for our high-speed addition circuits. The conversion of AHSD to and from binary will be discussed in detail. By choosing $r = 2^m$, where m is any positive integer, a binary number can be converted to its canonical AHSD representation in constant time. We will also present two simple algorithms for converting AHSD numbers to binary: the first stresses high speed and the other provides hardware reusability. Since the conversion from AHSD to binary has been considered the bottleneck of AHSD-based arithmetic computation, these algorithms greatly improve the performance of AHSD systems. For illustration, we will discuss in detail the example on AHSD(4), i.e., the radix-4 AHSD number system. The proposed approach is practical thanks to the simple conversion.

MULTI-OPERAND ADDITION

When adding a multiple of operands, say k of n digits, the fastest possible way to do it is to add them in a binary tree, each addition performed using a redundant representation of the intermediate sums, to allow

constant time addition at the nodes of the tree, with bounded carry-propagation between positions, i.e., without any “ripple-effect”. We will here concentrate on adding a pair of digits from two operands, where it alternatively is possible to accumulate several digits of the same weight in some redundant representation, and digits back into the wanted digit set, as suggested in [KS05] for decimal multi-operand addition. We are assuming that the initial operands are in some non-redundant representation, at most needing some constant time conversion or recoding of the non-redundant representation. The leaves of the tree must be able to add two such addends, with their sum in the chosen redundant representation employed internally in the tree. At the root of the tree, the final result must in general be converted back to some non-redundant representation, most likely the same as that of the original operands. The accumulation of k , n -digit operands can thus be performed in time $O(\log k)$, with final conversion in time $O(\log n)$. With radix $r = 2$, when the operand representation is employing the standard non-redundant digit set $D = \{0, 1, \dots, r-1\}$, very often the symmetric, maximally redundant digit set $D_0 = \{-(r-1), \dots, -1, 0, 1, \dots, r-1\}$ is used internally at the nodes, since then $d \in D \Rightarrow d \in D_0$. Then at most a simple modification of the digit encoding is necessary at the leaf nodes. This also permits some simple handling of sign-magnitude or complement representations of operands. Although this discussion applies to any value of $r \geq 2$, we will restrict the detailed analysis to situations where r is a power of 2. For $r = 2$ the situation is particularly simple, as a pairing of the bits of two operands provides an encoding of either their sum or difference in a redundant representation at the leaf nodes, also to be used at the internal nodes of the tree. Let $x = \sum_{i=0}^{n-1} x_i 2^i$ and $y = \sum_{i=0}^{n-1} y_i 2^i$ be two binary integers, then $x \pm y = \sum_{i=0}^{n-1} d_i 2^i$ with $d_i = x_i \pm y_i$ being a digit in the redundant digit set $\{-(r-1), 0, r-1\}$. The pair of bits (y_i, x_i) then provides an encoding of the digit d_i , where x_i has positive weight and y_i has negative weight. If the sum of the operands is wanted, y can easily be negated by inversion. We denote this the borrow-save encoding, and use the notation $d_i = (d_{ni}; d_{pi})$ with the component of negative weight in the first position. Alternatively,

with the same operands, $x+y = \sum_{i=0}^{n-1} s_i 2^i$, where $s_i = x_i + y_i - 2c_i$ is representing the digit sum, the digits can be encoded as the pairs $(x_i; y_i)$. This carry-save encoding can be employed in the rest of the tree.

But since there is no principal difference between the use of the carry-save and the borrow-save representation, we will generally consider the latter. Actual implementations of the internal radix 2, 4-to-2 addition nodes of the tree will be described in Section 4 below, but note that addition at the leaf nodes essentially comes for free, thus halving the number of operations to be performed, as well as saving space.

THE DIGIT-WISE ADDITION PROCESS

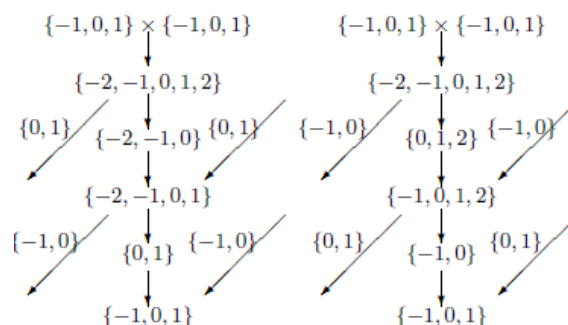
Adding two numbers digit-wise in the maximally redundant set $D = \{f \square 2r+1; 0; 2r \square 1g\}$ for radix $r = 2r, r \geq 2$, generates first an intermediate sum represented in the digit set $D_0 = \{f \square 2r+1+2 \ 2r+1 \square 2g\}$, from which carries in the set $C = \{f \square 1; 0; 1g\}$ are extracted, leaving behind digits from a much reduced digit set $D'' = \{f \square 2r+2 \ 2r \square 2g\}$. Note that this digit set must contain at least $2r$ different values. In a subsequent step, incoming carries are added into the positions, such that all digits now are in the same digit set D as the operands. Addition thus consists in a number of parallel digit-wise additions:

$$\begin{aligned}
 D \times D &= \{-2^r + 1, \dots, 2^r - 1\} \times \{-2^r + 1, \dots, 2^r - 1\} \\
 D' &= \{-2^{r+1} + 2, \dots, 0, \dots, 2^{r+1} - 2\} \\
 C &= \{-1, 0, 1\} \\
 D'' &= \{-2^r + 2, \dots, 0, \dots, 2^r - 2\} \\
 D &= \{-2^r + 1, \dots, 0, \dots, 2^r - 1\}
 \end{aligned}$$

Figure 1. Maximally redundant radix $2r$ addition for $r \geq 2$

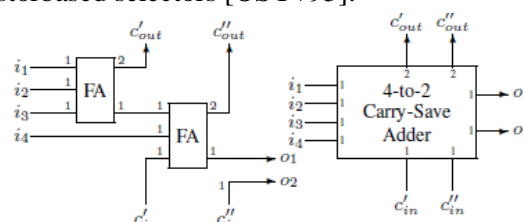
The first step consists in the digit-wise addition, the next in extracting the outgoing carry and modifying the digit accordingly. The last step is adding an incoming carry to the modified digit. The essential thing to observe is that the outgoing carry is independent of the incoming. Note that this process is possible for any value of $r \geq 2$, but not for $r = 1$, the binary borrow-save

representation with $D = \{f \square 1; 0; 1g\}$, as we shall discuss below. Also observe that it involves three sequential digit-wise add or subtract operations. However, the carry-extraction takes place at the most-significant end of the digit, and is thus in general faster than the add operations. Unless the encoding of the digit values themselves is redundant, these operations will be slower, the larger the digit set is. For radix 2, with the digit set $\{f \square 1; 0; 1g\}$, the situation seems more complicated. Following Avizienis [Avi61], the digit set conversion here must take place in two phases for a total of five steps, which takes two forms, depending on the sign of the incoming carry:



RADIX-2, 4-TO-2 ADDITION

Starting with the redundant radix 2 addition, several possible (e.g., two-bit [PGK01], and even three-bit [EL97]) encodings of the digits are possible, some of which were investigated in [Kor05]. All of these were shown to be feasible for addition in what has been denoted 4-to-2 adders, realizable by simple modifications of a carry-save, 4-to-2 adder for the addition of two operands over the digit set $\{f \square 1; 0; 2g\}$, as shown in Fig. 2. Using the two-bit encoding, with the digit value being the sum of the encoding bits, this type of adder was originally proposed by Weinburger in [Wei81]. There are several possible implementations of it, including some very efficient ones based on pass-transistor based selectors [OSY+95].



Employing the binary borrow-save encoding as a bit-pair $(x_n; x_p)$, where the left-most bit x_n has negative weight, the pair encodes the digit value $x = x_p \oplus x_n \cdot 2 \oplus 1; 0; 1g$. Addition of $(x_n; x_p)$ and $(y_n; y_p)$ can be realized by inverting some of the connections as shown in Fig. 3.

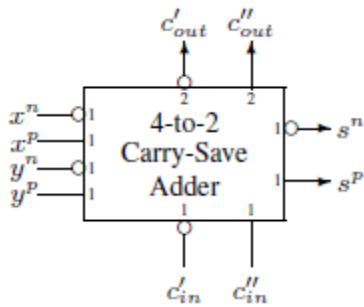


Figure 3. 4-to-2, borrow-save adder

Alternatively, the digit encoding could be 2's complement,

where a pair $(x_h; x_l)$ encodes the digit value $d = \lfloor 2x_h + x_l \rfloor \oplus 1; 0; 1g$ (the pair $(1; 0)$ excluded), with carry in borrow-save encoding. Fig. 4 shows an implementation, realized by a carry-save adder with some signals inverted.

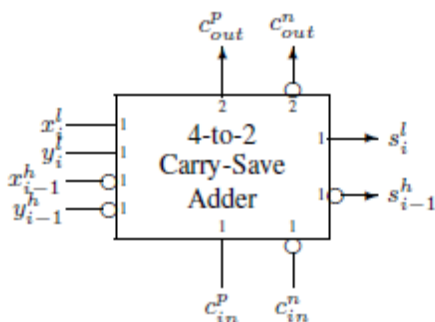


Figure 4. 4-to-2, 2's complement adder

As shown in [Kor05], it may be noted that in a multi-digit adder composed of a linear array of such adders, the inverters are not needed on the internal carry signals. Similarly, when such adders are connected in an array (or tree) for multi operand addition, the

inverters are not needed anywhere internally. This also shows that an implementation using borrow-save representation is identical to one using carry-save, except for some inverters at the boundary of the array

One such possibility for adding radix-16 digits, is combining four 4-to-2 borrow-save adders over the digit-set $\lfloor 1; 0; 1g$, which together provides an equivalent radix-16 digit adder over the same maximally redundant digit set as above. Since each digit now is encoded in 8 bits, compared to 5, a radix-16 digit adder now has 16 input and 8 output lines, compared to respectively 10 and 5. Thus the interconnect structure of the adders is more complex and requires more area. But note that only half as many such adders may be needed in a multi-operand addition array, since the sum of two standard non-redundant binary operands is simply obtained by pairing the bits of the operands, directly forming their sum in carry-save encoding (or by inverting one operand in borrow-save), to be used as further input. Expanding the 4-to-2 adders in terms of full adders with their interconnections, as an equivalent to the above digit adders in Fig. 5, using the borrow-save encoding we find Fig. 6, again not showing inversions on negative signals. For general r the delay of the circuit in Fig. 6 is independent of the radix $2r$, and identical to that of a single 4-to-2 adder.

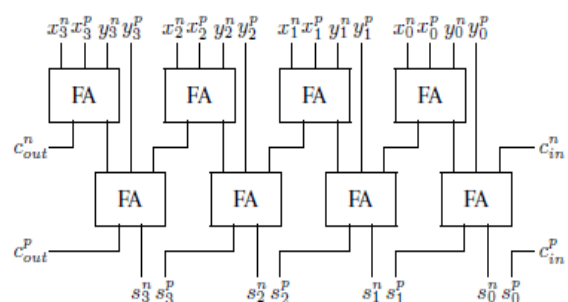


Figure 5. A radix 16 digit-adder design in 4-to-2 borrow-save encoding

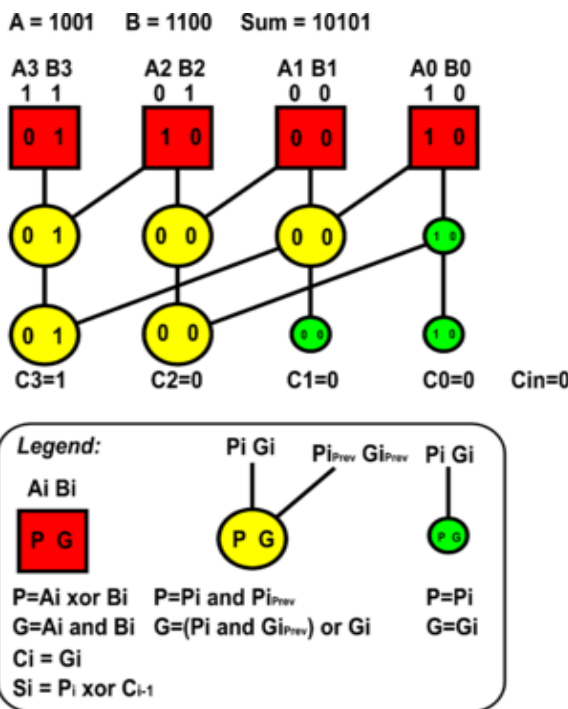
Extension: The Kogge–Stone adder is a parallel prefix form carry look-ahead adder. It generates the carry signals in $O(\log n)$ time, and is widely considered the

fastest adder design possible. It is the common design for high-performance adders in industry.

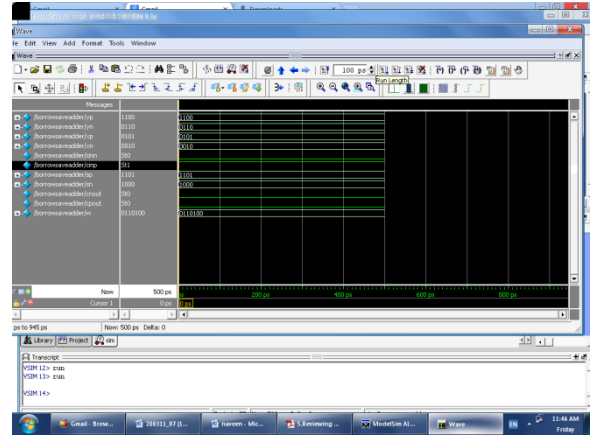
It takes more area to implement than the Brent–Kung adder, but has a lower fan-out at each stage, which increases performance. Wiring congestion is often a problem for Kogge–Stone adders as well.

An example of a 4-bit Kogge–Stone adder is shown to the right. Each vertical stage produces a "propagate" and a "generate" bit, as shown. The culminating generate bits (the carries) are produced in the last stage (vertically), and these bits are XOR'd with the initial propagate after the input (the red boxes) to produce the sum bits. E.g., the first (least-significant) sum bit is calculated by XORing the propagate in the farthest-right red box (a "1") with the carry-in (a "0"), producing a "1". The second bit is calculated by XORing the propagate in second box from the right (a "0") with C0 (a "0"), producing a "0".

The Kogge–Stone adder concept was developed by Peter M. Kogge and Harold S. Stone, which they published in 1973 in a seminal paper titled *A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations*.



RESULTS



CONCLUSIONS

It has been shown, that the proposed recoding of addends into a higher radix of the form $2r$ for $r \geq 2$, as in [Par93], [MI99], [JPG05], [JP07], [JG10], [GJ11], with digits encoded in non-redundant 2's complement representation, can not provide faster addition than using standard radix 2, carry-save or borrow-save adders applied directly on non-redundant binary addends. On the contrary, for multi-operand addition the delay is significantly larger when using such recoding into a higher radix, despite the claim "Ultrahigh-Speed" in the title of [JP07]. Furthermore, when employing the carry- or borrow-save encoding, half of the additions come for free, since just pairing two non-redundant binary numbers forms their sum in carry-save, or (with one of them inverted) in borrow-save. It is noted that (except for some inverters at the boundary) the logic of the adder array is identical, whether the carry-save or the borrow-save representation is used.

REFERENCES

- [Avi61] A. Avizienis. Signed-digit number representations for fast parallel arithmetic. IRE Transactions on Electronic Computers, EC-10:389–400, September 1961.
- [EL97] M.D. Ercegovac and T. Lang. Effective Coding for Fast Redundant Adders using the Radix-2 Digit Set $\{0; 1; 2; 3\}$. In Proc. 31st Asilomar Conf.

Signals Systems and Computers, pages 1163–1167, 1997.

[GJ09] S. Gorgin and G. Jaberipur. Fully Redundant Decimal Arithmetic. In Proc. 19th IEEE Symposium on Computer Arithmetic, pages 145–152. IEEE, June 2009.

[GJ11] S. Gorgin and G. Jaberipur. A Family of High Radix Signed

Digit Adders. In Proc. 20th IEEE Symposium on Computer Arithmetic, pages 112–121. IEEE, July 2011.

[HNN+87] Y. Harata, Y. Nakamura, H. Nagase, M. Takigawa, and N. Takagi. A High-Speed Multiplier Using a Redundant Binary Adder Tree. IEEE Journal of Solid State Circuits, pages 28–34, 1987.

[JG10] G. Jaberipur and S. Gorgin. An Improved Maximally Redundant Signed Digit Adder. Computers and Electrical Engineering, 36(3):491–502, May 2010.

[JP07] G. Jaberipur and B. Parhami. Stored-Transfer Representations with Weighted Digit-Set Encodings for Ultrahigh-Speed Arithmetic. IET Circuits Devices Systems, 1(1):102–110, February 2007.

[JPG05] G. Jaberipur, B. Parhami, and M. Ghodsi. Weighted Two-Valued Digit-Set Encodings: Unifying Efficient Hardware Representation Schemes for Redundant Number Systems. IEEE Transactions on Circuits and Systems, Regular Papers,

52(7):1348–1357, July 2005.

[KM06] P. Kornerup and J-M. Muller. Leading Guard Digits in Finite Precision Redundant Representations. IEEE Transactions on Computers, 55(5):541–548, May 2006.

[KM10] P. Kornerup and D.W. Matula. Finite Precision Number Systems and Arithmetic, volume 133 of Encyclopedia of Mathematics and its Applications. Cambridge University Press, Sept. 2010.