

## A Novel Solar Based Three-Level Neutral-Point-Clamped (NPC) Grid-Tied Inverter with Integrated Battery Storage



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### ABSTRACT:

The unbalance of the neutral point voltage is an inherent problem of three-level neutral-point-clamped (NPC) inverter, the effect of neutral point voltage balancing which is caused by voltage vector is analyzed, and the relationship of the voltage offset and neutral point voltage is studied in this paper. This paper proposes a novel neutral point balance strategy for three-level NPC inverter based on space vector pulse width modulation (SVPWM). A voltage offset is added to the modulation wave, and a closed-loop neutral point voltage balance control system is designed. In the control system, the dwelling time of synthesis voltage vectors for SVPWM is varied to solve the problem of the unbalance of the neutral point voltage, the sequence of the voltage vectors maintains unchanging. Simulation results show the neutral point voltage balancing control strategy based on SVPWM is effective.

### Key words:

space vector PWM, neutral point voltage.

### I. INTRODUCTION:

DUE to the world energy crisis and environmental problems caused by conventional power generation, renewable energy sources such as photovoltaic (PV) and wind generation systems are becoming more promising alternatives to replace conventional generation units for electricity generation [1], [2]. Advanced power electronic systems are needed to utilize and develop renewable energy sources. In solar PV or wind energy applications, utilizing maximum power from the source is one of the most important functions of the power electronic systems [3]–[5]. In three-phase applications,

two types of power electronic configurations are commonly used to transfer power from the renewable energy resource to the grid: single-stage and double-stage conversion. In the double-stage conversion for a PV system, the first stage is usually a dc/dc converter and second stage is a dc/ac inverter. The function of the dc/dc converter is to facilitate the maximum power point tracking (MPPT) of the PV array and to produce the appropriate dc voltage for the dc/ac inverter. The function of the inverter is to generate three-phase sinusoidal voltages or currents to transfer the power to the grid in a grid-connected solar PV system or to the load in a stand-alone system [3]–[5]. In the single-stage connection, only one converter is needed to fulfill the double-stage functions, and hence the system will have a lower cost and higher efficiency, however, a more complex control method will be required. The current norm of the industry for high power applications is a three-phase, single stage PV energy systems by using a voltage-source converter (VSC) for power conversion [4]. One of the major concerns of solar and wind energy systems is their unpredictable and fluctuating nature. Grid-connected renewable energy systems accompanied by battery energy storage can overcome this concern. This also can increase the flexibility of power system control and raise the overall availability of the system [2]. Usually, a converter is required to control the charging and discharging of the battery storage system and another converter is required for dc/ac power conversion; thus, a three-phase PV system connected to battery storage will require two converters. This paper is concerned with the design and study of a grid-connected three-phase solar PV system integrated with battery storage using only one three-level converter having the capability of MPPT and ac-side current control, and also the ability of controlling the battery charging and discharging. This will result in lower cost, better efficiency and increased flexibility of power flow control.

## II. PROPOSED SYSTEM:

As the switch is further away from the centre tap the switching time is shorter. Another difference between the conventional 2-level and multilevel NPC is the clamping diode. In case of 3-level NPC inverter, clamping diode, D1 and D4 clamped the DC bus voltage into three voltage level,  $+V_{dc}/2$ , 0 and  $-V_{dc}/2$ . Diode, D4 balances out the voltage sharing between S4in and S4out, with S4in blocking the voltage across C1 and S4out blocking the voltage across C2. The use of different parameters in the calculations and the regulations of the zero sequence signals complicate the control. The SVPWM scheme uses the nearest three vectors to synthesize the reference vector. Two methods can overcome the neutral point voltage problems: changing the vector switching sequence and changing the dwell times of the redundant states [7, 8]. Redundant states of the small vectors can be selected to maintain the neutral point voltage balance. Each small vector has two redundant states: positive small vector and negative small vector. These two states generate the same output voltage vector, however, they have the opposite control effect on the neutral point voltage. Therefore, redundant small vectors are used for neutral point voltage control [9].

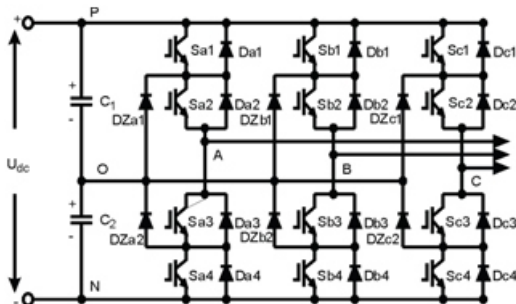


Fig. 1. Three-level NPC inverter structure diagram

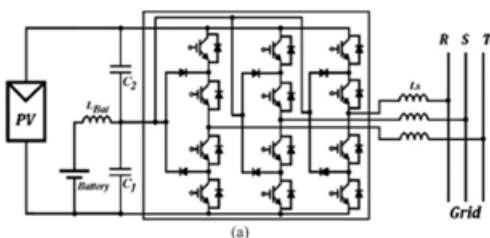


Fig. 2. Proposed configurations for integrating solar PV and battery storage: (a) basic configuration;

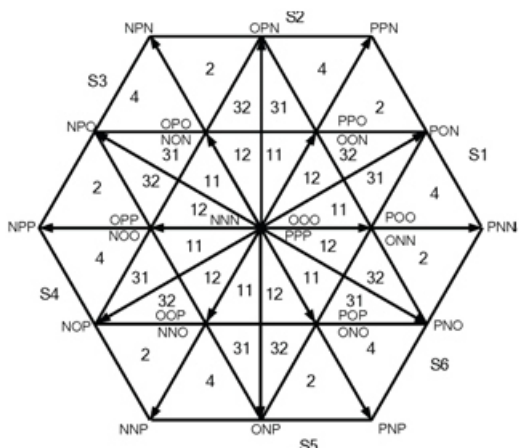
In the present paper, a neutral point voltage balance control strategy based on SVPWM is proposed. A voltage offset is added to the modulation wave in the regions of all the sectors as shown in Figure 2, and the neutral point voltage is controlled by changing the dwelling time of the synthesis voltage vectors. Simulation and experimental results show that the strategy has good capability for neutral point voltage balance.

## III. CONTROL STRATEGY: SVPWM scheme for NPC three-level inverter:

In the three-phase three-level NPC inverter, each phase has three output switching states “P”, “O” and “N”, which can be combined into a total of 27 possible switching states, the total 27 switching states correspond to 19 space voltage vectors, the space vector diagram is shown in Figure 2, it is composed of two hexagons.

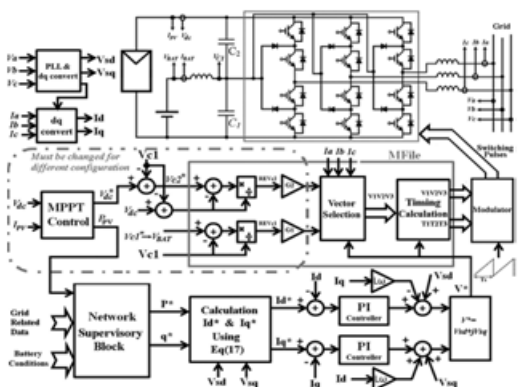
The plane is divided into six 60° sectors (S1, S2, S3, S4, S5 and S6) by large vectors. And each sector can be divided into four regions (R1, R2, R3 and R4, R1 contains two small regions R11 and R12, R3 contains two small regions R31, R32). For the nearest three vectors (NTV) SVPWM strategy, reference output voltage is synthesized by the nearest three vectors according to the equivalence of the volt-second integral.

Based on the vector magnitude, space voltage vectors can be divided into four types: large vectors, medium vectors, small vectors and zero vectors. The large vectors have the magnitude of  $2/3 U_{dc}$ , which are located at the vertices of the outer hexagon, the medium vectors have the magnitude of  $3/3 U_{dc}$ , which are located at the middle of the outer hexagon, the small vectors have the magnitude of  $1/3 U_{dc}$ , which are located at the vertices of the inner hexagon, and the zero vectors have the magnitude of zero. Each small vector has two switching states, one contains “P” state, which is called positive small vector, and the other contains “N” state, which is called negative small vector.



**Fig. 2. Voltage space vector distribution**

The four types of vectors have different effect on neutral point voltage deviation, it is summarized that the zero and large vectors do not affect the neutral point voltage; the medium vectors affect the neutral point voltage, but the influence depends on the operation condition the small vectors have specific effect on the neutral point voltage, the neutral point voltage will rise when positive small vector operates, and the neutral point voltage will drop when negative small vector operates in motoring mode. The power flow is from DC-link to the load when the system is in motoring mode; and the power flow is from the load to DC-link when the system is in regenerative mode. The mode depends on the direction of the DC-link current. In contrary, the neutral point voltage will rise when positive small vector operates, and the neutral point voltage will drop when negative small vector operates in regenerative mode.

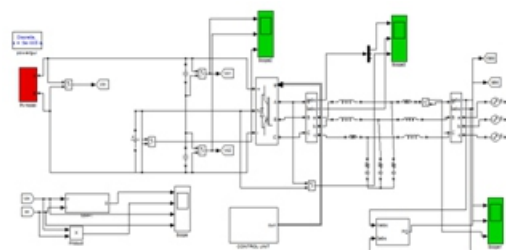


**Fig. 3. Control system diagram to integrate PV and battery storage**

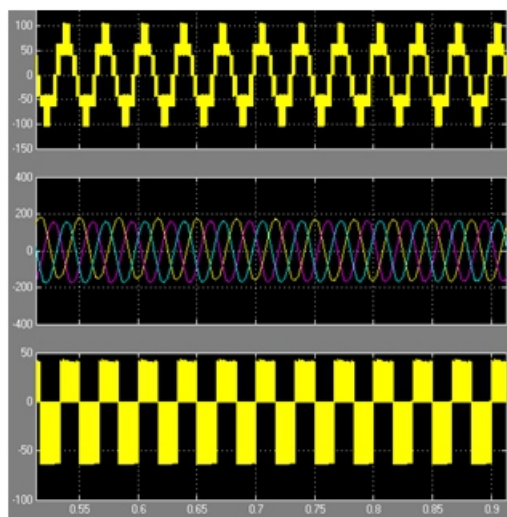
### 3. Neutral point balance control based on SVPWM:

In this paper, a SVPWM strategy is proposed to maintain the neutral point voltage balance. The switching sequence of this strategy is the same as that of conventional NTV SVPWM algorithm. The negative small vector is chosen to be the first given vector, Figure 3 shows the synthesis vectors sequence when the reference voltage vector  $v_{ref}$  is located in S1, R11. For the proposed neutral point voltage balancing strategy, in each region of the six sectors, a voltage offset is added to the adjusting phase  $u_k$  ( $k$  is a, b or c), and the dwelling times of operation vectors change. The adjusting phase  $u_k$  is the phase whose absolute value is the largest of three phases,

### IV. SIMULATION RESULTS:



**Fig. 4. Simulation circuit**



**Fig. 5. Phase-phase inverter voltage, inverter current and  $V_{a0}$**

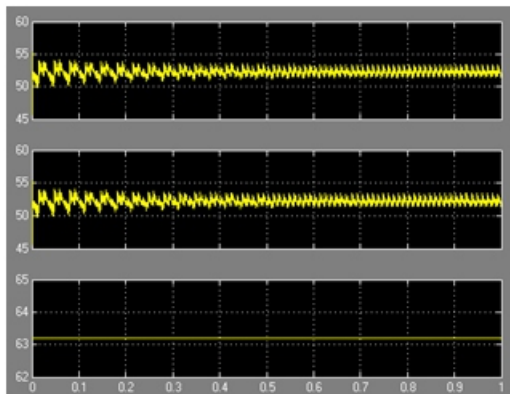


Fig.6 Dc capacitors and battery voltage

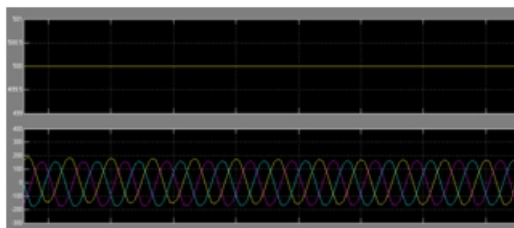


Fig.7 Output power and Grid Current

## V. CONCLUSION:

In this paper, a neutral point voltage balance control strategy based on SVPWM for three-level inverters is presented. This strategy maintains the neutral point voltage balance by adding a voltage offset to the modulation wave of the adjusting phase. The causes of the neutral point unbalance are studied in detail, and the influence of the voltage offset on neutral point balance is investigated, in motoring mode, when the voltage offset is positive, neutral point voltage will increase. In contrast, when the voltage offset is negative, neutral point voltage will decrease. In regenerative mode, neutral point voltage will increase when voltage offset is negative, and neutral point voltage will decrease when the voltage offset is positive. The new simple and effective strategy for neutral point voltage control is verified by simulation results.

## REFERENCES:

- [1] Celanovic N., Boroyevich D., A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Trans. Power Electronics* 15(2): 242-249 (2000).
- [2] Bruckner T., Bernet S., Guldner H., The active NPC converter and its loss-balancing control. *IEEE Trans. Industrial Electronics* 52(3): 855-868 (2005).

[3] McGrath B.P., Holmes D.G., Multicarrier PWM strategies for multilevel inverters. *IEEE Trans. Industrial Electronics* 49(4): 858-867 (2002).

[4] Qiang S., Wenhua L., Qingguang Y., Zhonghong W., A neutral-point potential balancing algorithm for three-level NPC inverters using analytically injected zero-sequence voltage. *Proc. IEEE 8th Annu. Conf. Applied Power Electronics*, Miami, USA, pp. 228-233 (2003).

[5] Ogasawara S., Akagi H., Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters. *Conf. Rec. IEEE 29th Annu. Meeting Industry Applications Society*, Toronto, Canada, pp. 965-970 (1993).

[6] Yongdong L., Chenchen W., Analysis and calculation of zero-sequence voltage considering neutral point potential balancing in three-level NPC converters. *IEEE Trans. Industrial Electronics* 57(7): 2262-2271 (2010).

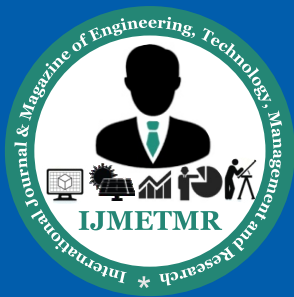
[7] Yamanaka K., Hava A.M., Kirino H., Tanaka Y., Koga N., Kume T., A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector. *IEEE Trans. Industry Applications* 38(6): 1572-1580 (2002).

[8] Tolbert L.M., Habetler T.G., Novel multilevel inverter carrier-based PWM method. *IEEE Trans. Industry Applications* 35(5): 1908-1107 (1999).

[9] Busquets-Monge S., Alepuz S., Rocabert J., Bordonau J., Pulse width Modulations for the Comprehensive Capacitor Voltage Balance of n-Level Three-Leg Diode-Clamped Converters. *IEEE Trans. Power Electronics* 24(5): 1364-1375 (2009).

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