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Enhanced Memory Reliability against Multiple Cell Upsets Using Decimal Matrix Code

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ABSTRACT:

Transient multiple cell upsets (MCUs) are becoming major issues in the reliability of memories exposed to radiation environment. To prevent MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, but the main problem is that they would require higher delay overhead. Recently, matrix codes (MCs) based on Hamming codes have been proposed for memory protection. The main issue is that they are double error correction codes and the error correction capabilities are not improved in all cases. In this paper, novel decimal matrix code (DMC) based on divide-symbol is proposed to enhance memory reliability with lower delay overhead. The proposed DMC utilizes decimal algorithm to obtain the maximum error detection capability. Moreover, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processes. ERT uses DMC encoder itself to be part of the decoder. The proposed DMC is compared to well-known codes such as the existing Hamming, MCs, and punctured difference set (PDS) codes. The obtained results show that the mean time to failure (MTTF) of the proposed scheme is 452.9%, 154.6%, and 122.6% of Hamming, MC, and PDS, respectively. At the same time, the delay overhead of the proposed scheme is 73.1%, 69.0%, and 26.2% of Hamming, MC, and PDS, respectively. The only drawback to the proposed scheme is that it requires more redundant bits for memory protection.

Index Terms:

Decimal algorithm, error correction codes (ECCs), mean time to failure (MTTF), memory, multiple cells upsets (MCUs).

INTRODUCTION:

AS CMOS technology scales down to nanoscale and memories are combined with an increasing number of electronic systems, the soft error rate in memory cells is rapidly increasing, especially when memories operate in space environments due to ionizing effects of atmospheric neutron, alpha-particle, and cosmic rays. Although single bit upset is a major concern about memory reliability, multiple cell upsets (MCUs) have become a serious reliability concern in some memory applications. In order to make memory cells as fault-tolerant as possible, some error correction codes (ECCs) have been widely used to protect memories against soft errors for years. For example, the Bose–Chaudhuri–Hocquenghem codes, Reed–Solomon codes, and punctured difference set (PDS) codes have been used to deal with MCUs in memories. But these codes require more area, power, and delay overheads since the encoding and decoding circuits are more complex in these complicated codes.

Interleaving technique has been used to restrain MCUs, which rearrange cells in the physical arrangement to separate the bits in the same logical word into different physical words. However, interleaving technique may not be practically used in content-addressable memory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures. Built-in current sensors (BICS) are proposed to assist with single-error correction and double-error detection codes to provide protection against MCUs. However, this technique can only correct two errors in a word. More recently, in 2-D matrix codes (MCs) are proposed to efficiently correct MCUs per word with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical.

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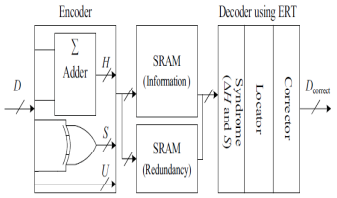
The bits per row are protected by Hamming code, while parity code is added in each column. For the MC based on Hamming, when two errors are detected by Hamming, the vertical syndrome bits are activated so that these two errors can be corrected. As a result, MC is capable of correcting only two errors in all cases. In an approach that combines decimal algorithm with Hamming code has been conceived to be applied at software level. It uses addition of integer values to detect and correct soft errors. The results obtained have shown that this approach have a lower delay overhead over other codes. n this paper, novel decimal matrix code (DMC) based on divide-symbol is proposed to provide enhanced memory reliability. The proposed DMC utilizes decimal algorithm (decimal integer addition and decimal integer subtraction) to detect errors. The advantage of using decimal algorithm is that the error detection capability is maximized so that the reliability of memory is enhanced. Besides, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because ERT uses DMC encoder itself to be part of the decoder.



METHODOLOGY:

This paper is divided into the following sections. The proposed DMC is introduced and its encoder and decoder circuits are present. This section also illustrates the limits of simple binary error detection and the advantage of decimal error detection with some examples. The reliability and overheads analysis of the proposed code are analyzed. In the implementation of decimal error detection together with BICS for error correction in CAM is provided. Finally, some conclusions of this paper are discussed and shared.SRAM reliability faces serious challenges from radiation induced soft errors in sub-100nm technologies [1]. SRAM cells are designed with minimum geometry devices to increase density and performance; however, a consequence is that the critical charge (Qcrit) that can upset such cells has become very small, potentially increasing the upset frequency. Therefore, it has become conventional to protect memories with the application of error correcting codes (ECC) such as single error- correcting (SEC) Hamming code, single-error correcting- double-error-detecting (SEC-DED) extended- Hamming, or SEC-DED Hsiao codes [2][3][4]. With increasing multi-bit upset (MBU) trends [5][6], conventional single-bit correcting ECC may not be sufficient to meet reliability goals. The problem is further exacerbated for space electronics where galactic cosmic rays carry heavy-ions with much higher linear energy transfer (LET) characteristics compared to terrestrial radiation sources. This work presents heavy-ion induced upset results for two prototype SRAM ICs designed in two characteristic 90nm processes revealing the extent of MBU in these processes. These results show that the multi-bit upsets in these processes can be as large as 13-bits, implying that current ECC architectures which use column interleaving by 2 or 4 with conventional SEC/SEC-DED codes ([7][8]) are not sufficient to mitigate the expected soft errors. This deficiency motivates the exploration of more powerful ECC implementations, such as double error correcting (DEC) BCH (Bose-Chaudhuri- Hocquenghem) codes. Commonly employed iterative BCH decoding schemes such as Berlekamp's-Massey,

Euclidian and Minimum Weight Decoding algorithms require a multi-cycle decoding latency [9][10][11], which is not tolerable for embedded memories. Therefore, a new parallel implementation approach is presented for DEC BCH codes. This parallel approach is suitable for SRAM applications where data is accessed in words on every transaction. In addition, a design space for various ECC techniques has been explored by implementing SEC Hamming, SEC-DED Hsiao, DEC and DEC-TED BCH codes using IBM's 90nm standard cell ASIC technology. The implementation results demonstrate the practicality of the proposed decoding implementation approach and also offer insights for various trade-offs for selecting soft error mitigation techniques. Accelerated irradiation test results on prototype SRAM ICs demonstrate the relative reliability efficiency of SEC-DED and DEC ECC techniques.Cosmic rays and high-energy particles are the dominant cause of soft errors in SRAMs and in digital circuits. In the mid-1990's, radiation induced soft errors were first reported in DRAMs. However, the changes in DRAM technology later made them more robust while SRAMs have become more vulnerable to soft errors as the technology scales. Soft errors can manifest as Single-Bit Upsets (SBU) of SRAM cells. Error Correction Codes (ECC) has been used for many years to mitigate SBU. The most common types of ECC for memories are Single-Error-Correcting (SEC) Hamming codes,

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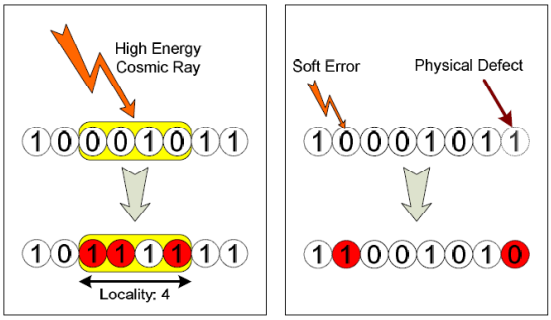
Single-Error- Correcting Double-Error-Detecting (SEC-DED) xtended Hamming codes, and Hsiao codes. Sometimes a single strike of a high-energy particle affects several adjacent memory cells, and causes Multi-Bit Upset (MBU). MBU was first observed in airplanes and space equipments which are more exposed to the galactic cosmic rays. Later, with technology scaling and the significant reduction in noise margins, MBU was observed in commercial electronics used for terrestrial applications. Recent studies show that MBU is the dominant contributor to the overall soft error rate and can be as large as 13 bits in a 90nm SRAM.

IMPLEMENTATION:

The CMOS technology scaling to nm, low cost, high density, high speed integrated circuits with low supply voltage has increased the probability of fault occurrence in the memories. This lead to the major reliability concern especially increases SRAM memory failure rate. Some commonly used mitigation techniques are triple modular redundancy, and error correction codes (ECCs). Soft errors are the major issue in the reliability of memories. Soft error will not damage the hardware, they only damage the data that is being processed. If detected, soft errors are corrected by rewriting corrected data in the place of erroneous data. Highly reliable system uses error correction approach, however in many systems it is difficult to correct data, or even impossible to detect error.To prevent soft errors from causing corruption in the data stored error correction codes are used such as matrix code, hamming etc.

when ECC is used, data are encoded when written in the memory and data are decoded when read from the memory. Thus the encoding and decoding process possess a vital impact on the memory access time and complexity. Multiple cell upsets have become the reliability concern in some application apart from single cell upset. The BCH code,reed Solomon code etc are used to deal with MCUs,but the area,power and delay overhead of these codes are high due to the complex encoding and decoding architecture. The decimal matrix code uses encoder reuse technique which uses encoder as apart of the decoder and thus reduces the area overhead and complexity.DMC enhances the reliability of the memory by improving the error correction capability. Reed-Muller codes are among the oldest known codes and have found widespread applications.

They were discovered by Muller and provided with a decoding algorithm by Reed in 1954. These codes were initially given as binary codes, but modern generalizations to q-ary codes exist. We will restrict our investigation to the binary case. One of the interesting things about these codes is that there are several ways to describe them and we shall look at two of these. One reason for doing this is to see how to move to the generalization even though we will not do so. Reed Muller codes are some of the oldest error correcting codes. Error correcting codes are very useful in sending information over long distances or through channels where errors might occur in the message. They have become more prevalent as telecommunications have expanded and developed a use for codes that can self-correct. ReedMuller codes were invented in 1954 by D. E. Muller and I. S.Reed. In 1972, a Reed Muller code was used by Mariner 9 to transmit black and white Photo graphs of Mars, see. Reed Muller codes are relatively easy to decode, and first-order codes are especially efficient.



A. Local (Burst) Error B. Two Global (Random) Errors

Local and global errors in an 8-bit SRAM caused by radiation or physical defects.Using the proposed definition, we can directly design codes for any desirable number of corrections of local and global errors. There is a significant difference between our proposed approach and available methods: In Gilbert codes, array codes, and product codes, the number of local error corrections depends on the size of the codeword; therefore, it is not feasible to design codes for any arbitrary number of local errors. For example, it is not possible to use any of the available methods to design a code that corrects four local and two global errors for 16-bit memories.

DISCUSSION

Types of Errors

- **Detection**
- **Correction**

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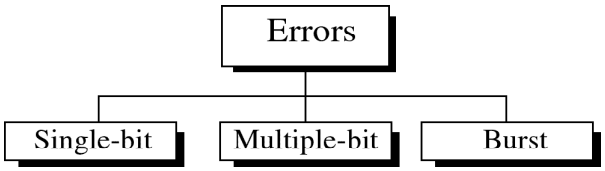
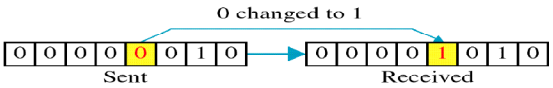
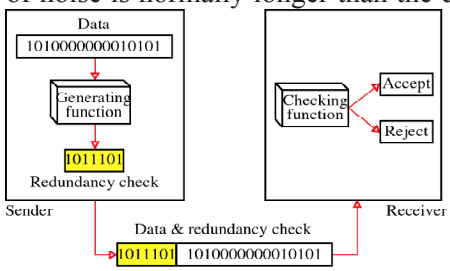
Data can be corrupted during transmission.For reliable communication, errors must be detected and corrected.Error detection and correction are implemented either at the data link layer or the transport layer of the OSI model



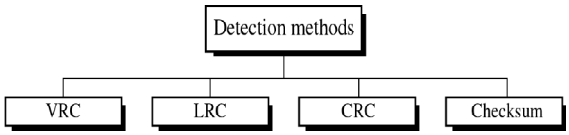
Single bit errors are the least likely type of errors in serial data transmission because the noise must have a very short duration which is very rare. However this kind of errors can happen in parallel transmission.



Burst errors do not necessarily mean that the errors occur in consecutive bits, the length of the burst is measured from the first corrupted bit to the last corrupted bit. Some bits in between may not have been corrupted. Burst error is most likely to happen in serial transmission since the duration of noise is normally longer than the duration of a bit.

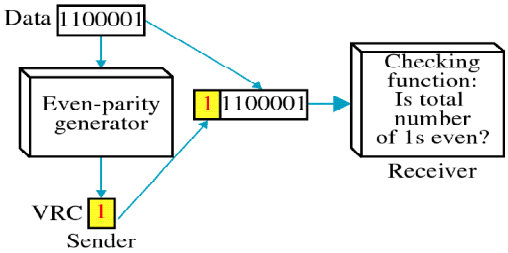


Four types of redundancy checks are used in data communications

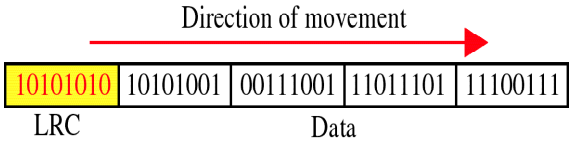


It can detect single bit error.

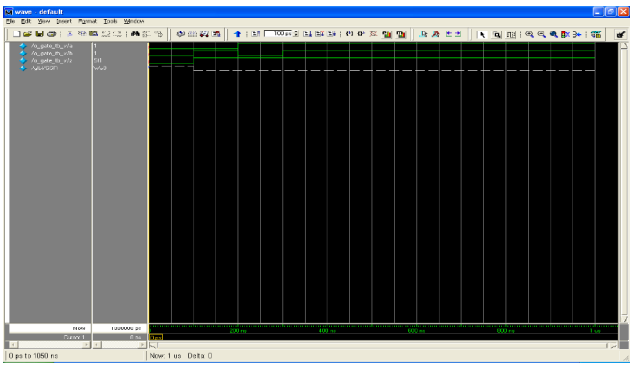
It can detect burst errors only if the total number of errors is odd.



If two bits in one data units are damaged and two bits in exactly the same positions in another data unit are also damaged, the LRC checker will not detect an error.



6. Experimental Results:



To save the simulation results, Go to the waveform window of the Modelsim simulator, Click on File -> Print to Postscript -> give desired filename and location. Note that by default, the waveform is "zoomed in" to the nanosecond level. Use the zoom controls to display the entire waveform. Else a normal print screen option can be used on the waveform window and subsequently stored in Paint. Behavioral Simulation output Waveform (Snapshot from ModelSim) For taking printouts for the lab reports, convert the black background to white in Tools -> Edit Preferences. Then click Wave Windows -> Wave Background attribute.

CONCLUSION:

In this paper, novel per-word DMC was proposed to assure the reliability of memory. The proposed protection code utilized decimal algorithm to detect errors, so that more errors were detected and corrected. The obtained results showed that the proposed scheme has a superior protection level against large MCUs in memory. Besides, the proposed decimal error detection technique is an attractive opinion to detect MCUs in CAM because it can be combined with BICS to provide an adequate level of immunity. The only drawback of the proposed DMC is that more redundant bits are required to maintain higher reliability of memory, so that a reasonable combination of k and m should be chosen to maximize memory reliability and minimize the number of redundant bits based on radiation experiments in actual implementation. Therefore, future work will be conducted for the reduction of the redundant bits and the maintenance of the reliability of the proposed technique.

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REFERENCES:

[1] D. Radaelli, H. Puchner, S. Wong, and S. Daniel, "Investigation of multi-bit upsets in a 150 nm technology SRAM device," IEEE Trans.Nucl. Sci., vol. 52, no. 6, pp. 2433–2437, Dec. 2005.

[2] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron induced soft error in SRAMs from an 250 nm to a 22 nm design rule," IEEE Trans. Electron Devices, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[3] C. Argyrides and D. K. Pradhan, "Improved decoding algorithm for highreliable reed muller coding," in Proc. IEEE Int. Syst. On Chip Conf.,Sep. 2007, pp. 95–98.

[4] A. Sanchez-Macian, P. Reviriego, and J. A. Maestro, "HammingSEC-DAED and extended hamming SEC-DED-TAED codes throughselective shortening and bit placement," IEEE Trans. Device Mater. Rel.,to be published.

[5] S. Liu, P. Reviriego, and J. A. Maestro, "Efficient majority logic faultdetection with difference-set codes for memory applications," IEEETrans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 1, pp. 148–156,Jan. 2012.

[6] M. Zhu, L. Y. Xiao, L. L. Song, Y. J. Zhang, and H. W. Luo, "New mix codes for multiple bit upsets mitigation in fault-secure memories," Microelectron. J., vol. 42, no. 3, pp. 553–561, Mar. 2011.

[7] R. Naseer and J. Draper, "Parallel double error correcting code design to mitigate multi-bit upsets in SRAMs," in Proc. 34th Eur. Solid-State Circuits, Sep. 2008, pp. 222–225.

[8] G. Neuberger, D. L. Kastensmidt, and R. Reis, "An automatic technique for optimizing Reed-Solomon codes to improve fault tolerance in memories," IEEE Design Test Comput., vol. 22, no. 1, pp. 50–58,Jan.–Feb. 2005.

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