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An Advanced Multilevel Cascaded H-Bridge Based Statcom with Power Quality Enhancement

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ABSTRACT:

This paper investigates subtle practical implementation issues which deteriorate the harmonic performance of this technique. The effects of non uniform dc bus voltages and capacitor voltage balancing strategies are investigated. Phase-shifted carrier (PSC) modulation has become an industry standard in its application to multilevel H-bridge static compensators (H-Stat Coms). The technique uses the cancellation of harmonics within each phase leg to significantly improve the harmonic performance relative to the switching frequency. Simulation results are presented which show that the harmonic performance of the PSC technique deteriorates as the number of voltage levels produced by the H-Stat Com increases.

Index Terms:

Control strategy, modulation strategy, multilevelconverters, static compensators, voltage balancing.

I.INTRODUCTION:

Multilevel converters have received more and moreattention because of their capability of high voltageoperation, high efficiency, and low electromagneticinterference. especially, multilevel converters havebeen used for STATCOM widely as it can improvethe power rating of the compensator to make itsuitable for medium or high-voltage high powerapplications[1-2]. There are many types ofmultilevel converters used for constructingSTATCOMs such as diode-clamp converter, flyingcapacitorbased converter, and cascaded H-bridgeconverter. cascaded H-bridge topologies is morepopular because of its many advantages: (1)it cangenerate almost sinusoidal waveform voltage fromseveral separate dc sources to reduce harmonics. (2)it can response faster because of eliminating theneed of a transformer to provide the requisitevoltage levels. (3)modularized circuit layout andpacking is very easy due to the simplicity ofstructure[3-4].

II.PROPOSED SYSTEM:

Fig. 1.1 Shows the circuit configuration for a 19-level (lineto-neutral) H-bridge StatCom (H-StatCom). Each stack ofH-bridges essentially forms one phase of a three-phase currentcontrolledvoltage source. The purpose of the H-StatCom isto modulate the voltage at the output of each stack so thatthe current through the inductors can be controlled to providepower factor correction, compensate for system harmonics, andalleviate other power quality problems.The earliest modulation scheme proposed for multilevelconverters is called staircase modulation. The voltagewaveforms produced using this technique are staircase approximationsto a sine wave.

This is an inherently visual techniquewhich has a simple hardware implementation and a minimumswitching frequency. One of the main disadvantages of thisscheme is the low-order harmonics which are induced bythe creation of the waveform. Selective harmonic elimination (SHE), pulsewidth modulation(PWM) is based on staircasemodulation, with the switching instants precomputed in sucha way as to enforce the elimination of particular harmonics. Theeliminationof specific harmonics improves thewaveform quality and decreases the total harmonic distortion(THD) of the converter current. SHE-PWM also retains thebenefits of a low switching frequency and a high efficiency.

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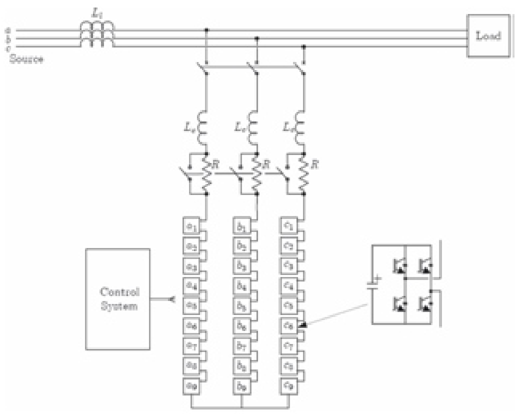

Fig. 1. Circuit configuration for a star-connected 19-level H-StatCom. investigated.

The harmonic performance of SHE-PWM is relatively goodfor converters of a low level number. However, when the levelnumber increases, the harmonic performance of an alternatetechnique named phase-shifted carrier (PSC) PWM increasesmore rapidly than that of SHE-PWM. This coupled withthe fact that solving the transcendental equations in SHE-PWM for a wide range of input conditions can be complex, has meantthat there has been limited use of this technique in industrialapplications, including H-StatComs.

PSC-PWM is based on the triangular wave comparison technique,which is employed extensively in two-level inverters. This technique uses a low-frequency reference waveformwhich is compared against a higher frequency triangularcarrier wave. Instants at which the two waveforms intersectcorrespond to the required switching instants for the H-bridge.The resultant train of output pulses from the bridge has afundamental component at the same frequency as the originalreference waveform.

III.CONTROL STRATEGY:
Phase Shifted PWM (PSCPWM):

In psc pwm all the triangular carriers have the same frequency and same peak-peak amplitude .but there is a phase shift between any two adjacent carrier waves.For m Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of θ=(360°/m-1).The gate signals are generated with proper comparison of carrier wave and modulating signal .

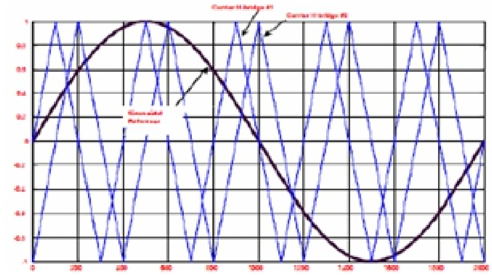

Fig. 2 Phase Shifted Carrier PWM

In this chapter performance analysis of phase shifted carrier basedpulse width modulation techniques is presented. The reference voltage iscontinuously compared with each of the shifted carrier signals. Each cell ismodulated independently using the PWM, which provides an even powerdistribution among the cells. A carrier phase shift of 180°/m for the cascadedinverter is introduced across the cells to generate a stepped multilevel outputwaveform with lower distortion, where ‘m’ is the number of full bridgeinverters in a multilevel phase leg. The PSCPWM technique is divided into two types, such as SH and SFO PWM techniques.For n-level converter, (n-1) phase shifted carrier signals are generated. The carriers between the full bridge inverters are phase shift180º/m. If the reference is greater than carrier signal, then the active device corresponding to that carrier is switched off.

IV.SIMULATION RESULT:

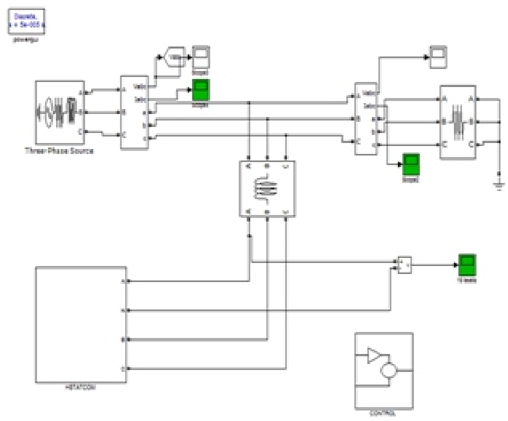

Fig 3 Simulation Circuit

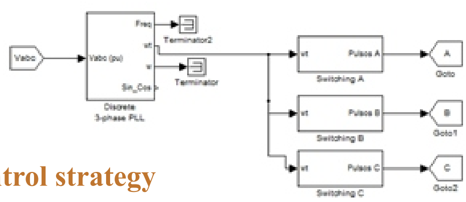

Fig 4.Control strategy

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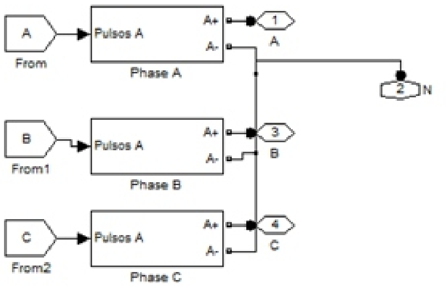

Fig 5.Hstatcom

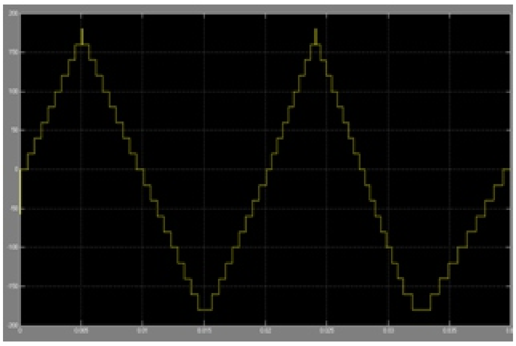

Fig6..19 level output

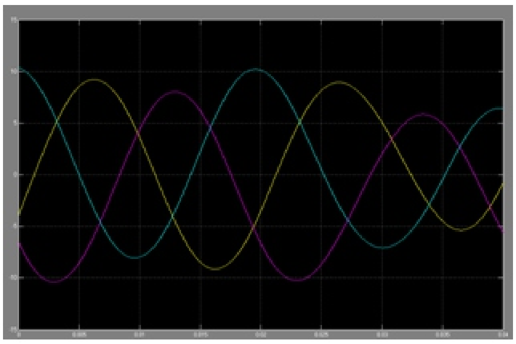

Fig7 source voltage

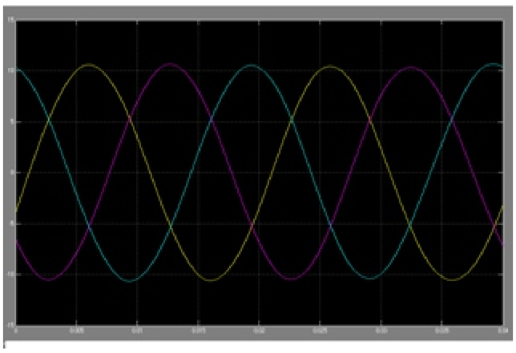

Fig 8 Load vloltage

V CONCLUSION:

This paper has investigated particular H-StatCom applicationand operational condition, namely, that of a 19-level H-StatCom, to calculate the practical performance of the phase shifted modulation technique. The results indicate that the harmonicperformance is not greatly affected when the nonuniformdc bus voltages are modeled..The simulation results showsuperior of the design controller, the DC voltagebalancing is accomplished, meanwhile , the systemhas very fast responses to the step commands.

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