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High Speed Low Power Multiplier using a Vedic Mathematical Approach

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ABSTRACT:

Multiplier design is always a challenging task; how many ever novel designs are proposed, the user needs demands much more optimized ones. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper we aim to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords:

Quantum Computing, Reversible Logic Gate, Urdhva Tiryakbhayam, Optimized Design, TRLIC.

1. INTRODUCTION:

Vedic mathematics is the ancient Indian system ofmathematics which mainly deals with Vedic mathematicalformulae and their application to various branches ofmathematics. Vedic mathematics was reconstructed from theancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirthaafter his research on Vedas. He constructed 16 sutras and16 upa sutras after extensive research in Atharva Veda. Themost famous among these 16 are Nikhilam Sutram, UrdhvaTiryakbhayam, and Anurupye. It has been found that UrdhvaTiryakbhayam is the most efficient among these.

The beautyof Vedic mathematics lies in the fact that it reduces otherwisecumbersome looking calculations in conventionalmathematics to very simple ones. This is so because the Vedicformulae are claimed to be based on the natural principles onwhich the human mind works. Hence multiplications in DSPblocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms whichcan be applied to various branches of engineering. Digital signal processing (DSP) is the technology thatis omnipresent in almost every engineering discipline. Fasteradditions and multiplications are the order of the day.Multiplication is the most basic and frequently used operationsin a CPU. Multiplication is an operation of scaling onenumber by another. Multiplication operations also form thebasis for other complex operations such as convolution,Discrete Fourier Transform, Fast Fourier Trans forms , etc.

With ever increasing need for faster clock frequency itbecomes imperative to have faster arithmetic unit. HenceVedic mathematics can be aptly employed here to performmultiplication.Reversible logic is one of the promising fields forfuture low power design technologies. Since one of therequirements of all DSP processors and other hand helddevices is to minimize power dissipation multipliers with highspeed and lower dissipations are critical. This paper proposesan implementation of Reversible Urdhva TiryakbhayamMultiplier which consists of two cardinal features. One is them fast multiplication feature derived from Vedic algorithmUrdhva Tiryakbhayam and another is the reduced heatdissipation by the virtue of implementing the circuit usingreversible logic gates. Energy loss is an important consideration in digitalcircuit design. A part of this problem arises from thetechnological non ideality of switches and materials. The otherpart of the problem arises from Landauer's principle for whichthere is no solution.

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Landauer's Principle states that logicalcomputations that are not reversible necessarily generatek*T*ln(2) joules of heat energy, where k is the Boltzmann'sConstant k=1.38xlO-23 J/K, T is the absolute temperature atwhich the computation is performed. Although this amount ofheat appears to be small, Moore's Law predicts exponentialgrowth of heat generated due to information lost, which willbe a noticeable amount of heat loss in next decade. Also by second law of thermodynamics any processthat is reversible will not change its entropy. On thermodynamical grounds, the erasure of one bit of information fromthe mechanical degrees of a system must be accompanied bythe thermalization of an amount of k*T*ln (2) joules ofenergy. The information entropy H can be calculatedfor any probability distribution. Similarly the thermodynamicentropy S refers to thermodynamic probabilities specifically.Thus gain in entropy always means loss of information, andnothing more.

Design that does not result in information loss iscalled reversible. It naturally takes care of heat generated due to information loss. Bennett showed that zero energydissipation would be possible only if the network consists ofreversible logic gates, Thus reversibility will become anessential property in future circuit design technologies. In the multiplier is designed using two units; oneis the partial product generation unit constructed using Fredkingates and other the summing unit constructed using 4x4 TSG gates. Presented a fault tolerant reversible 4x4 multipliercircuit. For construction of this circuit parity preserving FRGand MIG gates were used. Multiplier circuit was designed intwo parts. In second part of circuit MIG gates were usedinstead of half adders and full adders. Has proposed adesign of reversible multiplier which makes use of Peres gatefor generation of partial products as compared to , whichuses Fredkin gates. For the construction of adders the HNG gate was devised. Proposes low quantum cost realizationof reversible multipliers which mainly uses Peres full addergate (PF AG) for its design. It also uses Peres gates for thegeneration of partial products.

2. REVERSIBLE LOGIC:

Reversible logic is a promising computing designparadigm which presents a method for constructing computersthat produce no heat dissipation. Reversible computingemerged as a result of the application of quantum mechanicsprinciples towards the development of a universal computingmachine.

Specifically, the fundamentals of reversiblecomputing are based on the relationship between entropy, heattransfer between molecules in a system, the probability of aquantum particle occupying a particular state at any giventime, and the quantum electrodynamics between electronswhen they are in dose proximity. The basic principle ofreversible computing is that a bijective device with anidentical number of input and output lines will produce acomputing environment where the electrodynamics of thesystem allow for prediction of all future states based on knownpast states, and the system reaches every possible state,resulting in no heat dissipation.

A reversible logic gate is an N-input N-output logicdevice that provides one to one mapping between the inputand the output. It not only helps us to determine the outputsfrom the inputs but also helps us to uniquely recover theinputs from the outputs. Garbage outputs are those which donot contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of thecost of a primitive gate. Gate count is the number of reversiblegates used to realize the function. Gate level refers to thenumber of levels which are required to realize the given logicfunctions.

The following are the important design constraintsfor reversible logic circuits.

1.Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logicdepth or gate levels.
The basic reversible logic gates encountered duringthe design are listed below:

1.Feynman Gate : It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

2. Peres Gate : It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.

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3. Fredkin Gate : It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.

4.HNG Gate: It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

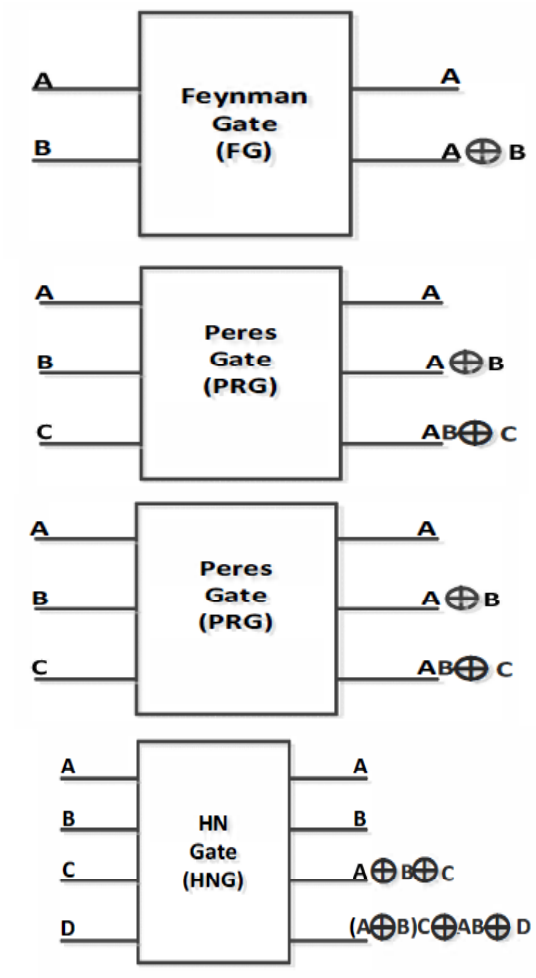


Figure 1: Reversible logic gates.

3. Urdhva – Tiryagbhyam:

Urdhva Tiryakbhayam (UT) is a multiplier based onVedic mathematical algorithms devised by ancient IndianVedic mathematicians. Urdhva Tiryakbhayam sutra can beapplied to all cases of multiplications viz. Binary, Hex andalso Decimals. It is based on the concept that generation of allpartial products can be done and then concurrent addition ofthese partial products is performed.

The parallelism ingeneration of partial products and their summation is obtainedusing Urdhva Tiryakbhayam. Unlike other multipliers with theincrease in the number of bits of multiplicand and/ormultiplier the time delay in computation of the product doesnot increase proportionately. Because of this fact the time ofcomputation is independent of c10ck frequency of theprocessor. Hence one can limit the c10ck frequency to a lowervalue. Also, since processors using lower lock frequencydissipate lower energy, it is economical in terms of powerfactor to use low frequency processors employing fastalgorithms like the above mentioned.

The Multiplier based onthis sutra has the advantage that as the number of bitsincreases, gate delay and area increases at a slow pace ascompared to other conventional multipliers.Urdhva – tiryagbhyam is the general formula applicable to all cases ofmultiplication and also in the division of a large number by another largenumber. It means.

Multiplication of two 2 digit numbers:

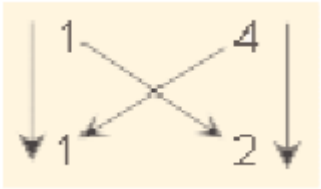
Ex.1: Find the product 14 X 12.

i)The right hand most digit of the multiplicand, the first number (14) i.e.,4 ismultiplied by heright hand most digit of the multiplier, the second number(12)i.e., 2. The product 4 X 2 = 8 forms the right hand most part of the answer.

ii) Now, diagonally multiply the first digit of the multiplicand (14) i.e., 4 and second digit of the multiplier (12) i.e., 1 (answer 4 X 1=4); then multiply the second digit of the multiplicand i.e.,1 and first digit of the multiplier i.e., 2 (answer 1 X 2 = 2); add these two i.e.,4 + 2 = 6. It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 6.

iii)Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplieri.e., 1 vertically, i.e., 1 X 1 = 1. It gives the left hand most part ofthe answer.

Thus the answer is 16 8.Symbolically we can represent the process as follows :



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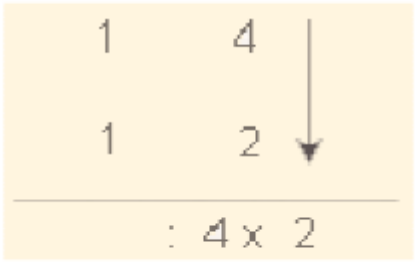
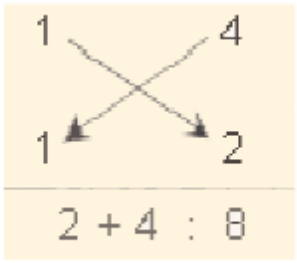
The symbols are operated from right to left .

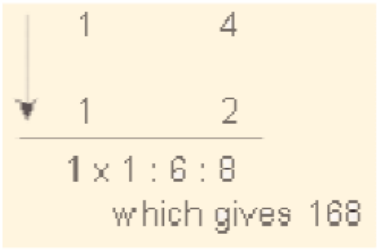
Step i) :



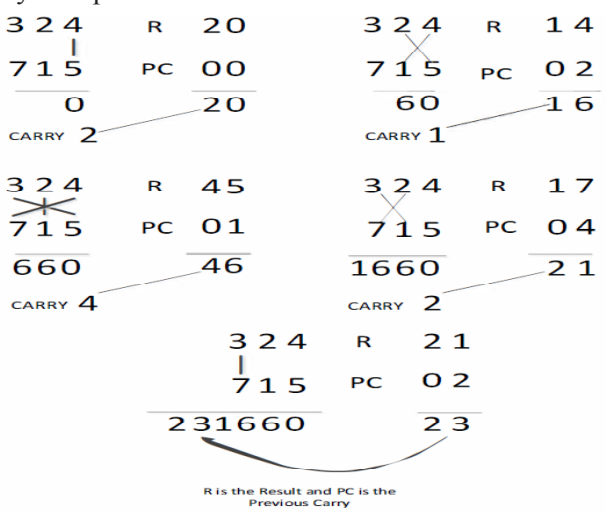
Step i i) :



Step iii):



The algorithm can be illustrated using the following visualwalkthrough. Figure 2 shows the application of the algorithmfor decimal multiplication and Figure 3 for binarymultiplication.



Flgure2: urdhva tiryakbhayam algorithm fordecimal-Multiplication.

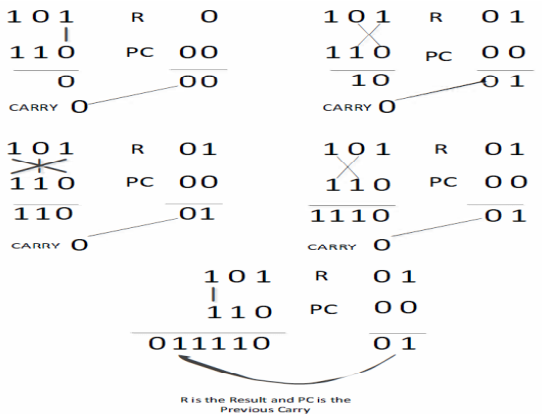


Figure 3: urdhva tiryakbhayamalgorithm for binary Multiplication.

4.ARCHITECTURE OF REVERSIBLE URDHVA TIRYAKBHA Y AM MULIPLI-ER:

The digital logic implementation of the 2X2 UrdhvaTiryakbhayam multiplier using the conventional logic gatesis as shown in figure 4. The expressions for the fouroutput bits are given under. The reversible implementation isas shown in figure 5. This design does not consider the fanouts.The circuit requires a total of six reversible logic gatesout of which five are Peres gates and remaining one is theFeynman Gate. The quantum cost of the 2X2 UrdhvaTiryakbhayam Multiplier is enumerated to be 21. The numberof garbage outputs is 9 and number of constant inputs is 4.The Reversible 4X4 Urdhva Tiryakbhayam-Multiplier design emanates from the 2X2 multiplier. Theblock diagram of the 4X4 Vedic Multiplier is presented in thefigure 6. It consists of four 2X2 multipliers each of whichproeures four bits as inputs; two bits from the multiplicandand two bits from the multiplier.

The lower two bits of theoutput of the first 2X2 multiplier are entrapped as the lowesttwo bits of the final result of multiplication. Two zeros areconcatenated with the upper two bits and given as input to thefour bit ripple carry adder. The other four input bits for theripple carry adder are obtained from the second 2X2multiplier. Likewise the outputs of the third and the terminal2X2 multipliers are given as inputs to the second four bitripple carry adder. The outputs of these four bit ripple carryadders are in turn 5 bits each which need to be summed up.

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This is done by a five bit ripple carry adder which generates asix bit output. These six bits form the upper bits of the finalresult. The ripple carry adder is consummated (realized) usingthe HNG Gate. The number of bits that need to be ripplecarried verdicts the number of HNG gates to be used. Thus a 4bit ripple carry adder needs 4 HNG gates and the 5 bit adderrequires 5 HNG gates. This design also does not take intoconsideration the fan out gates. For this design the quantumcost is computed to be 162, the total number of gates used willbe 37, the number of garbage outputs will be 62 and thenumber of constant inputs will be 29.

The Algorithm: Multiplication of 101 by 110.

l. We will take the right-hand digits and multiply themtogether. This will give us LSB digit of the answer.
2. Multiply LSB digit of the top number by the secondbit of the bottom number and the LSB of the bottomnumber by the second bit of the top number. Once wehave those values, add them together.
3. Multiply the LSB digit of bottom number with theMSB digit of the top one, LSB digit of top numberwith the MSB digit of bottom and then multiply thesecond bit of both, and then add them all together.
4. This step is similar to the second step, just move oneplace to the left. We will multiply the second digit ofone number by the MSB of the other number.
5. Finally, simply multiply the LSB of both numberstogether to get the final product.

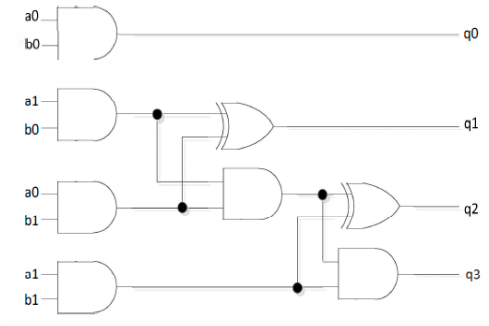


FIGURE 4: CONVENTIONAL LOGIC IMPLEMENTATION OF 2x2 ur MULTIPLIER

qO= aO.bO
ql= (a1.bO) xor (aO.bl)
q2= (aO.al.bO.bl) xor (al.bl)
q3= aO.al.bO.bl

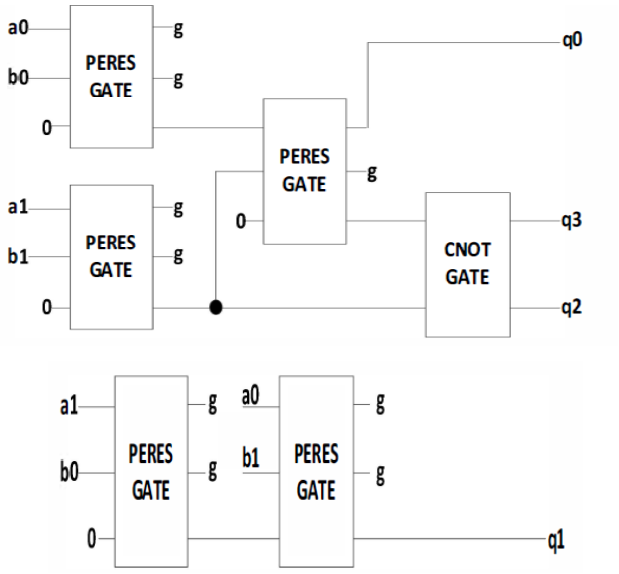
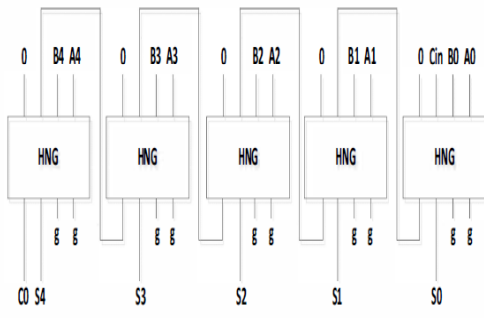
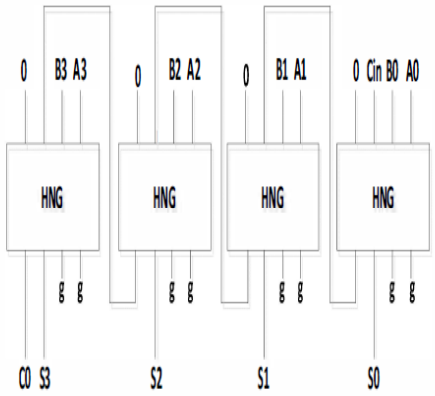


FIGURE 5: REVERSIBLE IMPLEMENTATION OF 2x2 urMULTIPLIER



5-BIT RIPPLE CARRY ADDER



4 BIT RIPPLE CARRY ADDER

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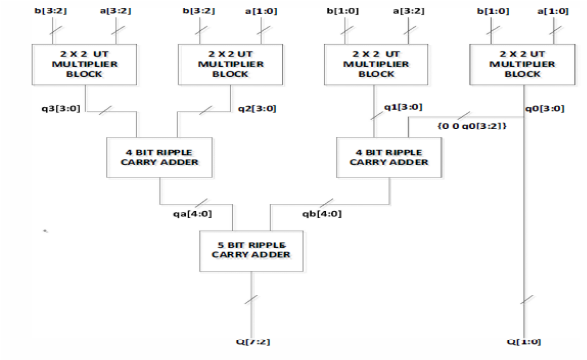


FIGURE 7: BLOCK DIAGRAM OF 4x4 UT MULTIPLIER.

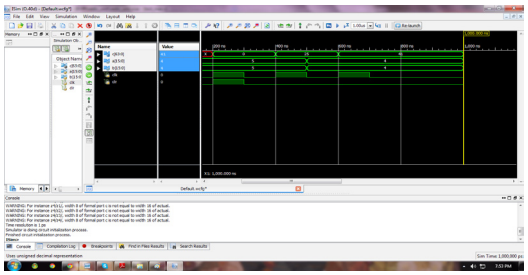
5. Concluding Remarks:

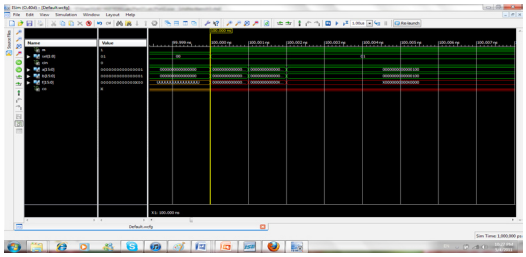
In this paper, a quantitative method to evaluate kinematic properties ofrobotic telesurgical manipulators using open surgical suturing and knot tying motion data recorded from experiments with expert surgeons is presented. Since open surgical motion data is used to evaluate the effectiveness ofthe system to perform suturing and knot tying tasks in minimally invasive setting, it might be desirable to segment the critical and non-critical parts ofthe recorded open surgical motion, especially to remove the segments corresponding to the parts ofthe motion when the instrument is not being actively used. This way, it possible to avoid over-conservative results. It is also important to note that this method cannot evaluate ifthe system will have the complete dexterity necessary, since it looks at the problem from a purely kinematic point ofview, and dexterity includes the dynamical properties ofthe manipulator as well as kinematics. This method not only provides the means to evaluate a kinematic design, but also helps to determine the requirements on various design parameters, such as joint ranges. In the analysis, it is also possible to move the robot with respect to the suturing site, to evaluate the suturing abilities ofthe system at different location and orientations in the workspace, and this can be used to find the optimal entry port location and robot configuration for optimal performance in suturing

6. Experimental Results:

The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figures 10 and 11 respectively. The following are the important design constraints for any reversible logic circuits.

1. Reversible logic circuits should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use a minimum number of reversible gates.





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