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Multi Modulus Low Power Flexible Divider in VLSI Technology

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Abstract

In this paper, a low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee, and IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers is proposed based on pulse-swallow topology and is implemented using a 0.18µm CMOS technology. The multiband divider consists of a proposed wideband multimodulus 32/33/47/48 prescaler and an improved bit-cell for swallow(S) counter and operates in 2.4 to 5 GHz resolution selectable from 1 to 25 MHz. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using vlsi technology.

*Index Terms—**DFF, multimodulus prescaler, dynamic logic, E-TSPC, frequency synthesizer, high-speed digital circuits, true single-phase clock (TSPC), wireless LAN (WLAN).***

INTRODUCTION

Over the last two decades, the continuous shrinking in the feature size of MOSFETs has increasingly attracted the research and development of low-power radio frequency CMOS integrated circuits [1], [2]. For mobile wireless communications, low-power operations are of crucial importance for the mobile units as the battery lifetime is limited by the power consumption and the low power consumption also helps to reduce the operating temperature resulting in more stable performance. For the modern transceiver architecture, a fully integrated frequency synthesizer with low power voltage-controlled oscillators (VCO) for quadrature signal generation and low power frequency dividers with multi-channel selection is always a topic of interest in research.

Phase-locked loops (PLLs) are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions.

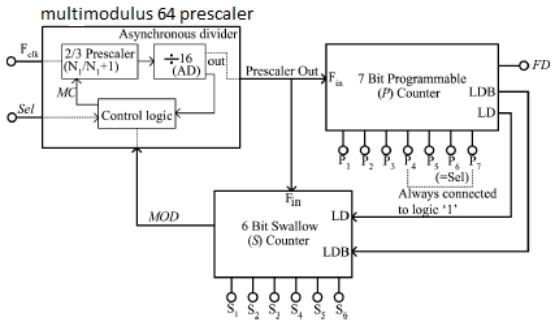

Figure.1.Proposed dynamic logic multiband flexible divider

The IEEE 802.15.4 standard has been specifically designed to cater for the needs of low cost, low power, low data rate and short range wireless networks. Few frequency synthesizers based on this standard have been reported in literature and the frequency synthesizer reported in [5] has the power consumption of 2.4 mW at 1.2-V power supply. In the previous design [1], a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler [4] and a wideband multimodulus32/33/47/48.

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In this paper a new method for designing a dynamic logic multiband flexible integer-N-divider has been proposed which was developed using a sleep transistor based and wideband multimodulus 32/33/47/48 prescaler with low-power wideband 2/3 prescaler and an integrated S counter as shown in Fig. 1.

A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply". The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit.

DESIGN CONSIDERATIONS

In the case of high-speed digital circuits propagation delay and power consumption are the important parameters. The maximum operating frequency of a digital circuit is given by,

$$F_{max}=\frac{1}{tpLH+tpHL} \qquad (1)$$

The tpLH and tpHL denote the propagation delays of the low- to-high and high-to-low transitions of the gates, respectively. The CMOS digital circuits total power consumption is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching}=\sum_{i=1}^{n} F_{clk} C_{li} V_{dd}^2 \qquad (2)$$

Where n is the number of switching nodes, fclk is the clock frequency, CLi is the load capacitance at the output node of the ith stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{sc} = I_{sc} * V_{dd} \qquad (3)$$

Where Isc is the short-circuit current. The short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-μmCMOS process.

Sleep Transistor Approach the most well-known traditional approach is the sleep approach [3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. By cutting off the power source, this technique can reduce leakage power effectively. However, the technique results in destruction of state plus a floating output voltage.

State-destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. These types of techniques are also called gated-Vdd and gated-Gnd (note that a gate dc lock is generally used for dynamic power reduction).Propose a technique they call Multi-Threshold Voltage CMOS (MTCMOS) which adds high-Vth sleep transistors between pull-up networks and Vdd and between pull-down networks and ground as shown in Figure 1while logic circuits use low-Vth transistors in order to maintain fast logic switching speeds. The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. However, the additional sleep transistors increase area and delay. Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values significantly impact the wake-up time and energy of the sleep technique due to the requirement to

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recharge transistors which lost state during sleep (this issue is nontrivial, especially for registers and flip-flops).

A Dual Stack Approach In dual stack approach [7], 2 PMOS in the pull- down network and 2 NMOS in the pull-up network are used. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Compared to previous approaches it requires greater area. The delay is also increased.

Figure 4 shows the configuration of dual stack method in case of a multiband flexible divider. In this method, there are two extra MOSFETS parallel to the sleep transistors. These extra MOSFET helps to retain state which is crucial for the operation of MFD. As the retention transistors are stacked they help to reduce leakage power. Its operation is similar to the case of logic circuits. We apply S=1 when the circuit is in active mode and S=0 when it is in sleep mode.

WIDEBAND 2/3 PRESCALER

The E-TSPC 2/3 prescaler reported in [1] consumes large short- circuit power and has a higher frequency of operation than that of TSPC2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design was reported in [2] which consists of two D-flip-flops

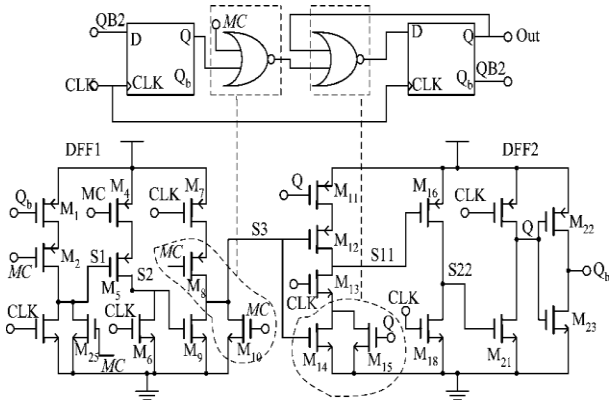

Figure.5. Wideband single phase clock 2/3 prescaler.

two NOR gates embedded in the flip-flops as in Fig. 5. The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2. Here, the transistors M2, M25, M4, M8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

$$C_{L\_Design} = I \; C_{dbM19} \; C_{dbM20} \; 2(C_{gdM19} \; C_{gdM20}) \; C_{gM15} \; C_{gM11} \quad (4)$$

When MC='1', transistor M10 turns-on and node S3 switches to logic '0' irrespective of the data at node S2. The second NOR gate output is always equal to the inverted output of DFF2 as shown in Fig, which is equivalent to simple DFF with its complimentary output connected to the input as shown in Fig.. Thus the prescaler act as divide-by-2 when MC='1'. Here, even though the output of DFF2 is connected in feedback to the input of DFF1, the switching data at node S1 and S2 is blocked by the transistor M10 to reach to the node S3. Thus the switching power at the node S3 is always zero and S2 due to the feedback action of the DFF2 output which switches continuously. The total power of the prescaler in divide-by-2 mode of operation is equal to the sum of switching power of DFF2 and the switching power of first two stages of DFF1 which is less than the conventional 2/3prescaler.

$$P_{wideband\text{-}divide\text{-}by\text{-}2} = \sum_{n=1}^{4} F_{clk} C_{li} V_{dd}^2 + P_{sc1} + P_{sc2} \quad (5)$$

When MC='0', transistor M10 turns-off and the inverted data at node S2 is passed to the node S3. The second NOR gate output is always equal to the inverted output of DFF2. Fig, shows the equivalent circuit of the proposed 2/3 prescaler unit in divide-by-3 mode of operation which is equivalent to the schematic shown in Fig5.

The combination of inverter and NOR gate is equivalent to logic AND gate with the other input inverted. Thus the prescaler act as divide-by-3 when MC='0' There is continuous switching activity at each node and the switching power is given by the sum of switching power of both the DFF1 and DFF2 respectively

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MULTIMODULUS 32/33/47/48 PRESCALAR

The proposed wideband multimodulus prescaler is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed prescaler can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 6. It performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multimodulus prescaler consists of the wideband 2/3 (N1 / (N1 + 1)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD) = 16) and combinational logic circuits to achieve multiple division ratios. Besides the usual MOD signal for controlling N / (N + 1) divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

Case 1: Sel = 0

When Sel = 0, the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC = 1, the 2/3 prescaler operates in the divide-by-2 mode and when MC = 0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD = 1, the NAND2 gate output switches to logic "1" (MC = 1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD * N1) + (0 * (N1 + 1)) = 32 \quad (6)$$

Where N1 = 2 and AD = 16 is fixed for the entire design. If MOD = 0, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N + 1 performed by the multimodulus prescaler is

$$N + 1 = ((AD - 1) * N1) + (1 * (N1 + 1)) = 33 \quad (7)$$

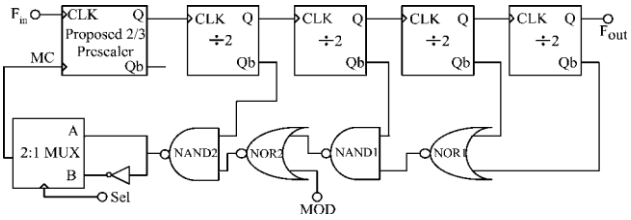

Figure6. Multimodulus 32/33/47/48 Prescaler.

Case 2: Sel = 1

When Sel = 1, the inverted output of the NAND2 gate is directly transfered to the input of 2/3 prescaler and the multi- modulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal . If MC = 1, the 2/3 prescaler operates individe-by-3 mode and when MC = 0, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when Sel = 0, If MOD = 1, the division ratio N + 1 performed by the multimodulus prescalar is same as (4) except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = (AD * (N1 + 1)) + (0 * N1) = 48 \quad (8)$$

If MOD = 1, the division ratio N performed by the multi- modulus prescaler is

$$N = ((AD - 1) * (N1 + 1)) + (1 * N1) = 47 \quad (9)$$

MULTIBAND FLEXIBLE DIVIDER USING SLEEP TRANSISTORS

The single phase clock multiband flexible divider using sleep transistor which is shown in Fig. 1 consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable -counter and a 6-bit swallow counter.

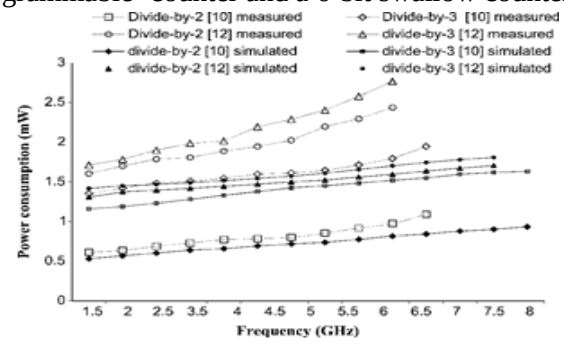

Figure.7.Postlayoutand measured power consumption results of 2/3 prescaler

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The multi- modulus 32/33/47/48 prescaler is briefly discussed in Section IV. The control signal decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5–5.825 GHz).

Swallow S-counter

The 6-bit -counter shown in Fig. 5 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit-cell used in this design shown in Fig. 6 is similar to the bit-cell reported in [6], except it uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S1 and S2 switch to logic“0” and the bit-cell doesn’t perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high the input bit PI transferred to the output.

In the initial state, MOD=0, the multimodulus prescaler selects the divide-by-(N+1) mode (divide-by-33 or divide-by-48) and P,S counters start down counting the input clock cycles. When the S counter finishes counting, MOD switches to logic “1” and the prescaler changes to the divide-by-N mode (divide-by-32 or divide-47) for the remaining (P-S) clock cycles. During this mode, since S counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S1 and S2 at logic “0,” thus saving the switching power in S counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

Programmable P-counter

The programmable P-counter used in the design of the fully programmable divider is a 7-bit asynchronous down counter. The P-counter is designed with 7 reloadable TSPC D flip-flops (DFF) and an end-of-count (EOC) detector which has reload circuit in it. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF’s are loaded by the programmable pins P1-P7. As the counter is triggered by the output of the prescaler, the P-counter starts down counting till the state “0000000” is reached. Once this state is detected by the EOC logic circuit, the load (LD) signal goes high to reset all loadable FF’s to the initial state. The 32/33 prescaler scales the input 2.4 GHz signal by a value of 32 or 33 such that the P and S counters will be working in the frequency range of 72 - 78 MHz in order to obtain the 1 MHz frequency output.

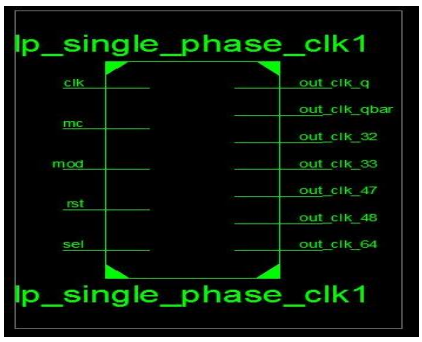

Fig 8: multimodulus 64 divider circuit

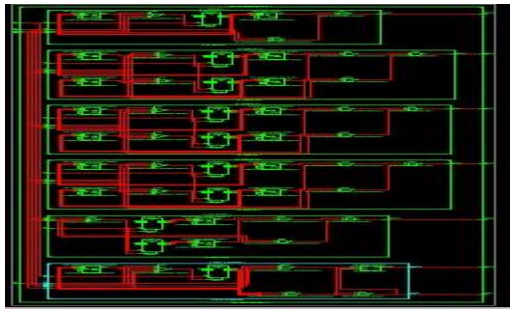
Fig 9: frequency divider rtl symentric

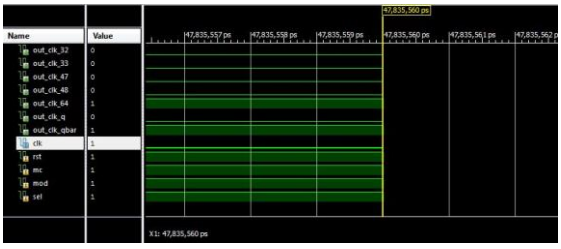
Fig 10: multimodulus 64 divider output

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Comparison between previous work and present work we can reduce the power consumption and reduce the 7 number of stages.

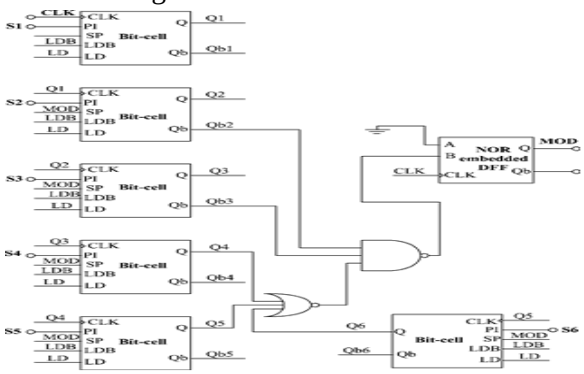

Figure.8. Asynchronous 6-bit S counters

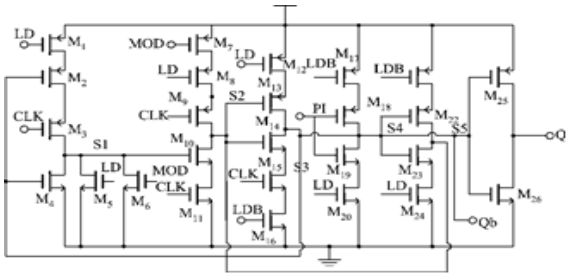

Figure.11. Asynchronous loadable bit-cell for S counters

Sel=0 (2.4–2.484 GHz): the multimodulus prescaler acts as 32/33 prescaler, the Pcounter is programmable from 64 to 127 bit P7 always logic ''1'' of the counter always remains at logic "1") and the S counter is programmable from 0 to 31 to accommodate division ratios from 2048 to 4095 with finest resolution of 1 MHz However, since we are interested in the 2.4-GHz band, bit P6 of the counter always remains at logic "0," since it is tied to the logic signal **Sel**, allowing it to be programmable from 75 to 78. Bit S6 of the Scounter is kept at logic '0' allowing a programmable division from 0 to 31 for the low-frequency band of operation to accommodate division ratios from 2400 to 2484 with resolution of 1 MHz different channel spacing can be achieved by programming Scounter. The frequency division FD ratio of the multiband divider in this mode is given by

$$\mathbf{FD = (N + 1) * S + N * (P – S) = NP + S} \quad (10)$$

Sel=1 (5–5.825 GHz): the multimodulus prescaler acts as 47/48 prescaler, the Pcounter is programmable from 64 to 127 bit P7 always logic ''1'' of the counter always remains at logic "1" and the S counter is programmable from 0 to 48 to accommodate division ratios from 3024 to 6095 with finest resolution of 1 MHz However, since we are interested in the 5-GHz band, bit P6 of the counter always remains at logic "1," since it is tied to the logic signal **Sel**, allowing it to be programmable from 105 to 122. Bit S6 of the Scounter allowing a programmable division from 0 to 48 for the high-frequency band of operation to accommodate division ratios from 5000 to 5824 with resolution of 5 MHz The frequency division **FD** ratio of the multiband divider in this mode is given by

$$\mathbf{FD = (N * S) + (N + 1) * (P – S) = (N + 1) P – S} \quad (11)$$

SIMULATION RESULTS

The simulation of the design is performed using HSPICE. The proposed multiband flexible divider consume the power consumption, gate count and area of the previous programmable dividers and the proposed programmable divider at the supply voltage shown in Table

Comparison between previous and present work and power delay product was calculated.

CONCLUSION

In this paper a lower-power single-phase clock multiband flexible divider, the circuit simplicity leads to reduced power consumption, reduced number of gates required and hence a reduced area requirement we have implemented fully programmable multi-band flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g frequency synthesizers. However, implementing frequency synthesizer which covers 2.4 GHz ISM band and 5-6 GHz WLAN using multi-band divider is very challenging as it requires low power, low phase noise dual-band VCO. When compared to previous power consumption 56.74% has been reduced. In future, more work has to be done in exploring better ways of implementing the low power techniques.

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