

## Optimization of Power and Area Efficient Shift Register Using Pulsed Latch

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### Abstract

*This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 128-bit shift register using pulsed latches was fabricated using a 65nm CMOS process with  $V_{DD} = 1.0V$ . The proposed shift register saves area and power compared to the conventional shift register with flip-flops.*

**Index Terms**—area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.

### I. INTRODUCTION

A SHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [1], communication receivers [2], and image processing ICs [3]–[5]. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register [3]. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [4]. A 16-megapixel CMOS image sensor uses a 45K-bit shift register [5]. As the word length of the

shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flops in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

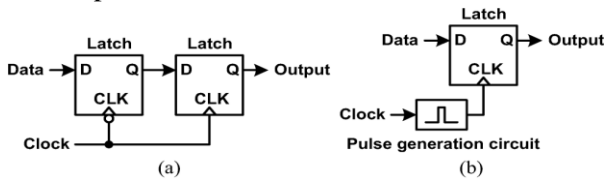
This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The rest of the paper is organized as follows: Section II describes the architecture of the proposed shift register. Section III presents the measurement results of the fabricated chip. Finally, conclusions are drawn in Section IV.

### II. ARCHITECTURE

#### A. Proposed Shift Register

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch

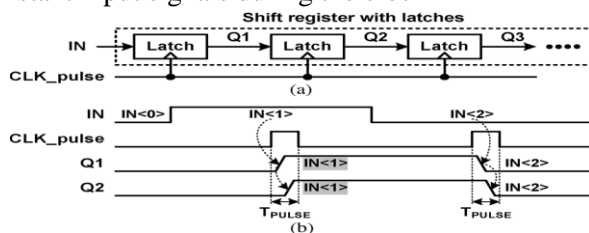
and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.



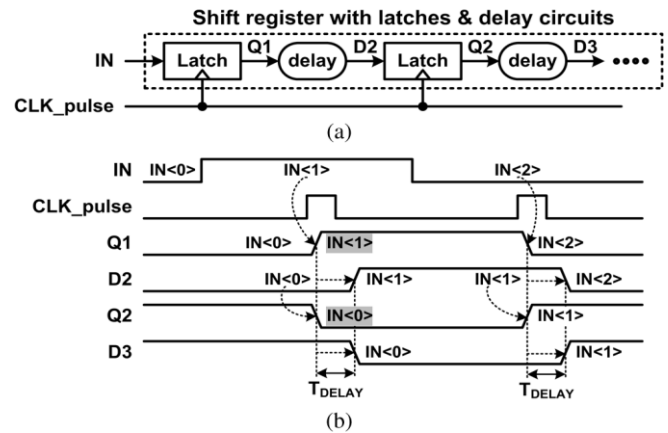
**Fig.1. (a) Master-slave flip-flop.(b) Pulsed latch.**

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK\_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width ( $T_{PULSE}$ ). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed ( $T_{DELAY}$ ) and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width ( $T_{PULSE}$ ), but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock

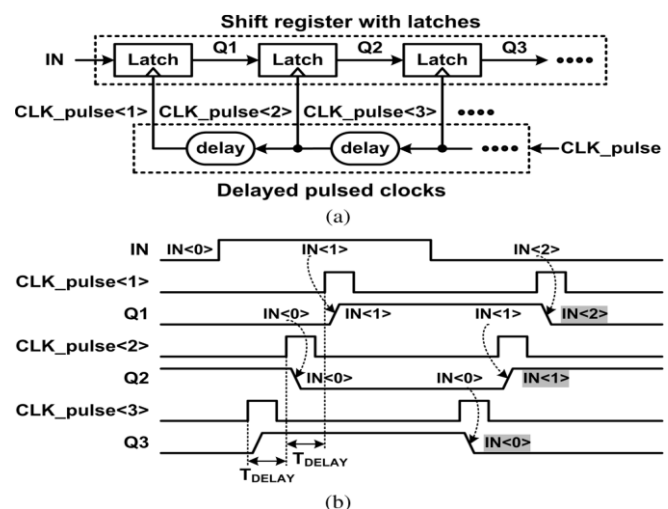


**Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.**



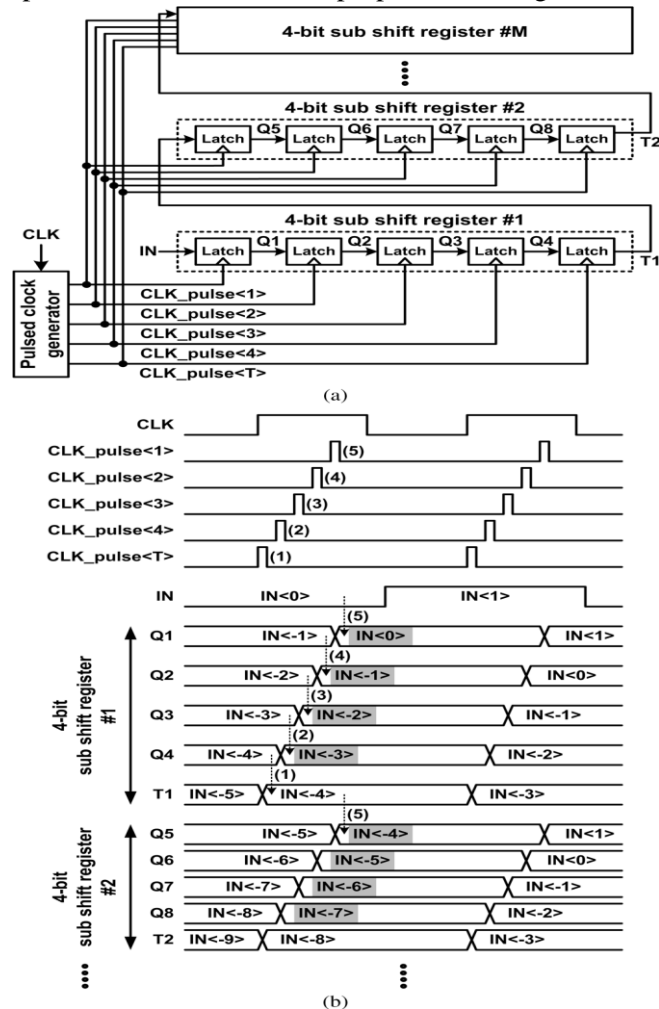
**Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.**

Pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.



**Fig. 4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.**

Fig. 5(a) shows an example the proposed shift register. The proposed shift register is divided into  $M$  sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five nonoverlap delayed pulsed clock signals ( $\text{CLK\_pulse}<1:4>$  and  $\text{CLK\_pulse}<T>$ ). In the 4-bit sub shift register #1, four latches store 4-bit data ( $Q1-Q4$ ) and the last latch stores 1-bit temporary data ( $T1$ ) which will be stored in the first latch ( $Q5$ ) of the 4-bit sub shift register #2.. Fig. 5(b) shows the operation waveforms in the proposed shift register.



**Fig. 5. Proposed shift register. (a) Schematic. (b) Waveforms.**

Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the

opposite order of the five latches. Initially, the pulsed clock signal  $\text{CLK\_pulse}<T>$  updates the latch data  $T1$  from  $Q4$ . And then, the pulsed clock signals  $\text{CLK\_pulse}<1:4>$  update the four latch data from  $Q4$  to  $Q1$  sequentially. The latches  $Q2-Q4$  receive data from their previous latches  $Q1-Q3$  but the first latch  $Q1$  receives data from the input of the shift register ( $IN$ ). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an  $N$ -bit shift register is divided into  $K$ -bit sub shift registers, the number of clock-pulse circuits is  $K+1$  and the number of latches is  $N+N/K$ . A sub shift register consisting of  $K+1$  latches requires  $K+1$  pulsed clock signals. The number of sub shift registers ( $M$ ) becomes  $N/K$ , each sub shift register has a temporary storage latch. Therefore,  $N/K$  latches are added for the temporary storage latches.

The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuit to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register ( $K$ ).  $K$  is selected by considering the area,

power consumption, speed. The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latch and a clock-pulse circuit are 1 and  $\alpha_A$ , respectively. The total area becomes  $\alpha_A \times (K+1) + N(1+K)$ . The optimal  $K = \sqrt{N/\alpha_A}$  for the minimum area is obtained from the first-order differential equation of the total area. An integer  $K$  for the minimum area is selected as a divisor of  $N$ , which is nearest to  $K = \sqrt{N/\alpha_A}$ .

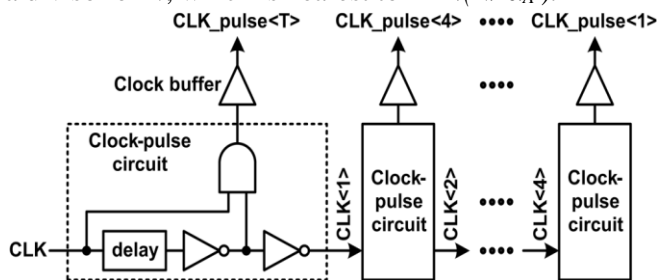


Fig. 6. Delayed pulsed clock generator

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and  $\alpha_P$ , respectively. The total power consumption is also  $\alpha_P \times (K+1) + N(1+1/K)$  the increment ratio of the clock buffers is small. The number of clock buffers is  $K$ . As  $K$  increases, the size of a clock buffer decreases in proportion to  $1/K$  because the number of latches connected to a clock buffer ( $M=N/K$ ) is proportional to  $1/K$ . Therefore, the total size of the clock buffers increases slightly with increasing  $K$  and the effect of the clock buffers can be neglected for choosing  $K$ .

The maximum number of  $K$  is limited to the target clock frequency. As shown in Fig. 7 the minimum clock cycle time ( $T_{CLK\_MIN}$ ) is  $T_{CP} + K * T_{DELAY} + T_{CQ}$ , where  $T_{CP}$  is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK\_pulse<T>),  $T_{DELAY}$  is the delay of two neighbor pulsed clock signals,  $T_{CQ}$  is the delay from the rising edge of the last pulsed clock signal (CLK\_pulse<1>) to the output signal of the latch Q1.  $T_{CLK\_MIN}$  is proportional to  $K$ . As  $K$  increases,

the maximum clock frequency ( $f_{CLK\_MAX} = 1/T_{CLK\_MIN}$ ) decreases in proportion to  $1/K$ . Therefore,  $K$  must be selected under the maximum number which is determined by the maximum clock frequency of the target applications.

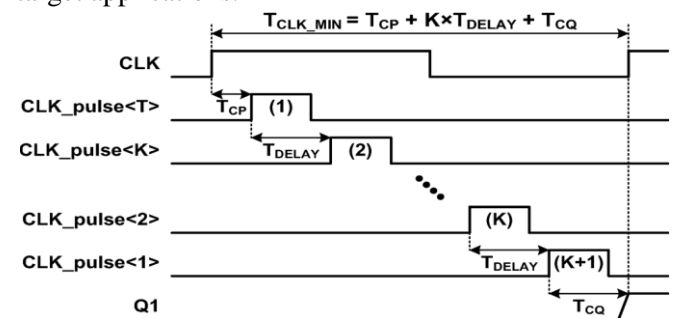


Fig. 7. Minimum clock cycle time of the proposed shift register.

The  $(K+1)$  pulsed clock signals in Fig. 7 are supplied to all sub shift registers. Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK\_pulse<T> and CLK\_pulse<1>) which have a long clock pulse interval.

### III. FLIP FLOP S AND LATCHES FOR SHIFT REGISTER

In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the



maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flops. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 8, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig. 8 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors ( $M_1 - M_3$ ) in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors ( $M_1 - M_3$ ) must be larger than the pull-up current of the PMOS transistors in the inverters.

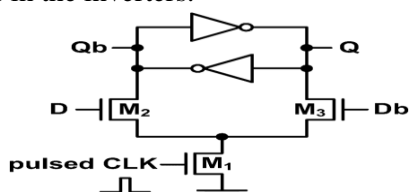


Fig. 8. Schematic of the SSASPL [6].

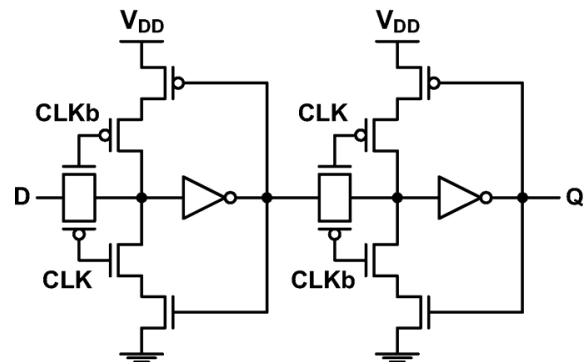


Fig. 9. Schematic of the PPCFF [10].

TABLE I  
TRANSISTOR COMPARISON OF PULSED LATCHES AND FLIP-FLOPS

|              |            | Total number of transistors | Number of transistors connected to clock |
|--------------|------------|-----------------------------|--|
| Pulsed latch | SSASPL [6] | 7                           | 1  |
|              | TGPL [7]   | 10                          | 4  |
|              | HLFF [8]   | 14                          | 2  |
|              | CP3L [9]   | 26                          | 6  |
| Flip-flop    | PPCFF [10] | 16                          | 8  |
|              | SAFF [11]  | 18                          | 3  |
|              | DMFF [12]  | 22                          | 5  |
|              | CPSA [13]  | 28                          | 5  |
|              | CCFF [14]  | 28                          | 5  |
|              | ACFF [15]  | 22                          | 4  |

Table I shows the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch (TGPL) [7], hybrid latch flip-flop (HLFF) [8], conditional push-pull pulsed latch (CP3L) [9], Power-PC-style flip-flop (PPCFF) [10], Strong-ARM flip-flop (SAFF) [11], data mapping flip-flop (DMFF) [12], conditional precharge sense amplifier flip-flop (CPSAFF) [13], conditional capture flip-flop (CCFF) [14], adaptive-coupling flip-flop (ACFF) [15] are compared with the SSASPL [6] used in the proposed shift-register. When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops. The SSASPL uses 7 transistors, which is the smallest number of transistors among the pulsed latches [6]–[9]. The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops [10]–[15]. Fig.9 shows the schematic of the PPCFF, which is a

typical master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. The conventional shift register using flip-flops was implemented with the PPCFFs. Two types of the proposed shift register using pulsed latches were implemented with the SSASPLs. The proposed shift register achieves a small area and low power consumption compared to the conventional shift register

#### IV. SIMULATION RESULTS

All the simulations are performed on Microwind3.5 and DSCH3.5. The main focus of this work is to meet all challenges faces in designing of shift register circuit with pulsed latch. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. The simulation results are shown in below figures.

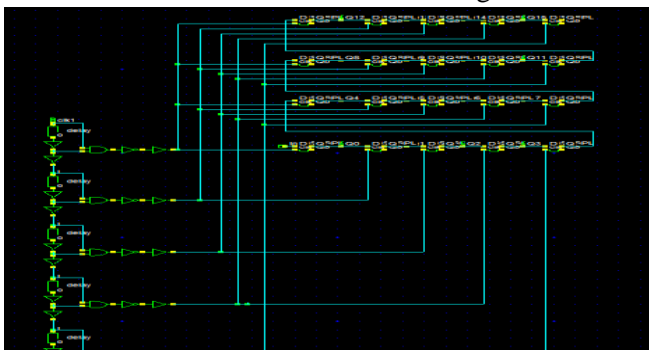


Fig10: Schematic of 16 bit shift register using SSASPL

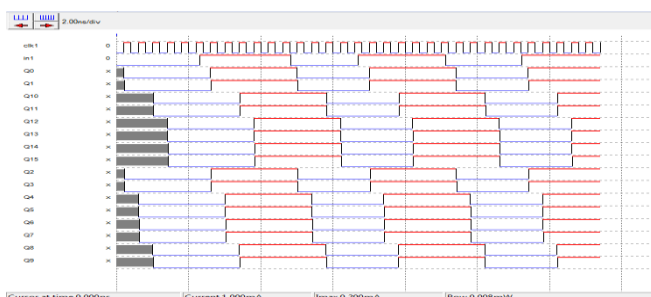


Fig 11: Timing Diagram of 16bit shift register using SSASPL

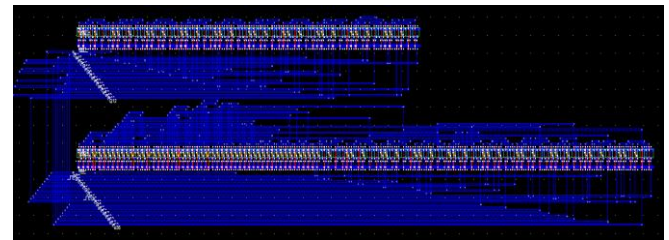


Fig 12: Layout of 16 bit shift register using SSASPL

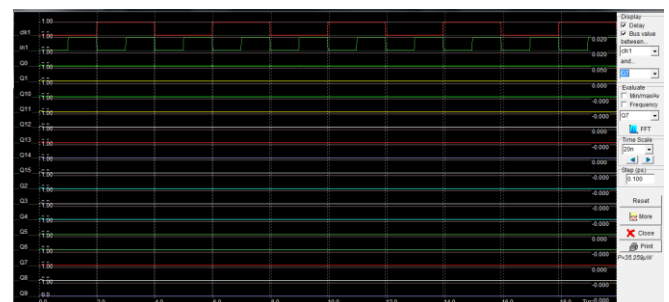


Fig 13: Simulation of Layout of 128 bit shift register using SSASPL

#### V. CONCLUSIONS

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 128-bit shift register was fabricated using a 65nm  $\mu\text{m}$  CMOS process with  $V_{DD} = 1.0\text{V}$ . The proposed shift register saves area and power compared to the conventional shift register with flip-flops.

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