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Efficient Shift Register Design Using Non Overlapped Delayed Clock Pulses for Encoding and Decoding

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ABSRACT

The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption.

This project proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

INTRODUCTION

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixelCMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

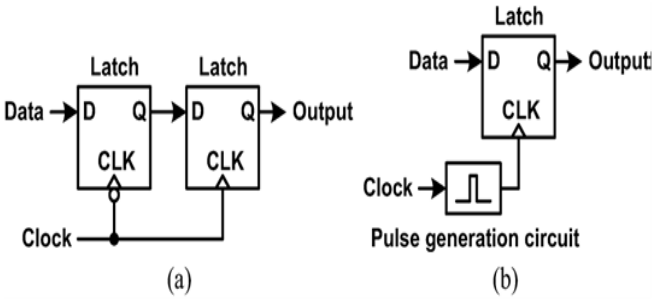

Fig.1 (a) Master-slave flip-flop. (b) Pulsed latch.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register

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solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals bygrouping the latches to several sub shifter registers and usingadditional temporary storage latches.

EXISTING SYSTEM

The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

A master-slave flip-flop using two latches can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem.

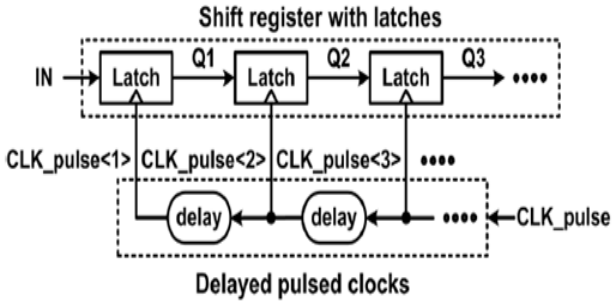

Fig. 2. Schematic of Shift register with latches and delayed pulsed clock signals

Shift Register

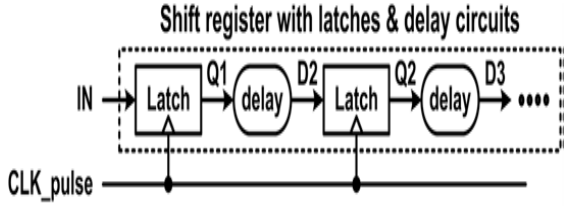

Fig. 3. Schematic of Shift register with latches, delay circuits, and a pulsed clock signal.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3. The output signal of the latch is delayed and reaches the next latch after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4.

The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

PROPOSED SYSTEM

In the proposed system we are implementing the application of the shift registers in the design and implementation of the encoder and decoder.

The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches.

Master Slave Clocking

Gigabit Ethernet transceivers operate in a "loop timed "fashion (Fig. 10). This means that the transceivers at the two ends of a link assume two different roles as far as synchronization is concerned. One of them, called the master, transmits data using an independent clock GTX-CLK provided through the GMII interface (in actuality the transmit clock used by the master may be a filtered version of GTX-CLK, obtained using a phase locked loop with a very narrow bandwidth, to reduce jitter). The other side, called the slave, synchronizes its receive and transmit clocks to the signal received from the master, using its timing recovery system. The slave

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transmit clock maintains a fixed phase relationship with the slave receive clock at all times. Then, the receive clock at the master synchronizes with the signal received from the slave. Thus, after an initial acquisition period, the master receive clock will follow the master transmit clock with a phase difference determined by the round trip delay of the loop. This phase relationship may vary dynamically as a result of the need of the master receive clock to track jitter present in the signal received from the slave.

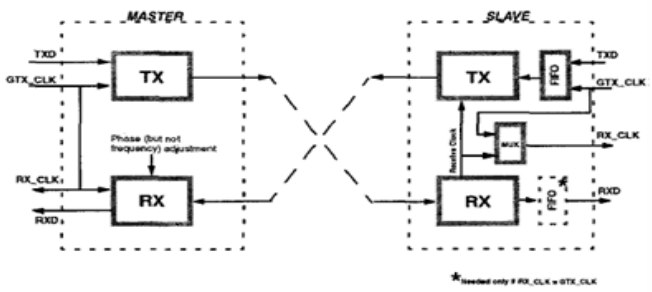

Fig. 1000Base-T master-slave clocking.

DIFFERENCE BETWEEN LATCHES AND FLIP FLOPS:

Latches and flip flops are the basic elements and these are used to store information. One flip flop and latch can store one bit of data. The main difference between the latches and flip flops is that, a latch checks input continuously and changes the output whenever there is a change in input. But, flip flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock. In this article, we are going to look at the operations of the numerous latches and flip-flops.

Latches and Flip Flops

Both Latches and flip flops are circuit elements wherein the output not only depends on the current inputs, but also depends on the previous input and outputs. The main difference between the latch and flip flop is that a flip flop has a clock signal, whereas a latch does not. Basically, there are four types of latches and flip flops: SR, D, JK and T. The major differences between these types of flip flops and latches are the number of i/ps they have and how they change the states. There are different variations for each type of latches and flip-flops which can enhance their operations.

EXPERIMENTAL STUDY

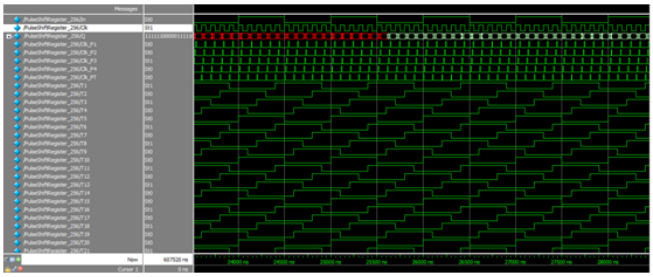

Fig1: The pulsated latches shift register result

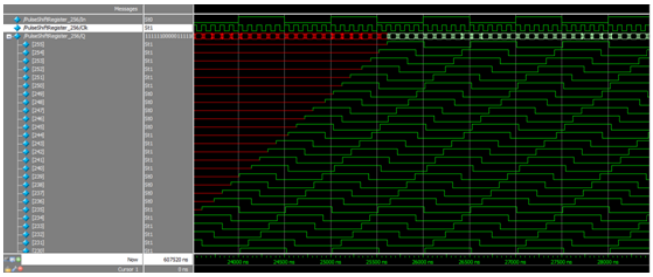

Fig2: the pulsed latches shift register result

The result was achieved by combining 4-bit shift registers in parallel manner. We are using total 64 stages of 4- bit shift registers. Each 4-bit shift registers using 5 latches in total. We are showing the non-overlapped multiple pulsed clock pulses using the delayed clock pulse generator unit. We are showing the shift registers output in the final output.

CONCLUSION

This project proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

FUTURE SCOPE:

In future, we can use this shift registers using pulsed latches to design the encoders and decoders. Those encoders are very much useful in encryption and decryption techniques, which are useful in security applications. Besides that we can also increase the bit size of the shift register for faster operations and for more robust secure applications.

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