ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

An Optimized R-TCAM Array Design Based on Reversible Elements

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Abstract:

Ternary CAM is an improved version of CAM memory which could be used for broader searching operations. It searches input data among stored data and gives the output as the matched data. Now a day Ternary CAM became very popular for its deterministic and quick searching ability as it operates in parallel to compare the data stored with the search data. Reversible method has also gained its name in the industry because of its feature of ultra-low power-characteristics. Hence the reversible-logic has been used as an alternate option for limiting the power consumption in the current design scheme of TCAM cell. The proposed method includes the design of a 4×5 R-TCAM array using individual TCAM cells which are completely built by reversible elements to overcome with the power problem. The optimized limits of a reversible TCAM memory cell are estimated as worst case delay, garbage outputs number and quantum-cost of the design. This proposed model provides us the greater matching and searching ability for fast running applications such as in routers and some networking equipment.

Keywords: TCAM, Garbage output, Quantum cost, Reversible logic, Content addressable memory, Power consumption

I. INTRODUCTION

In many high-performance network applications the need of a special kind of memory called as Content-Addressable-memory which is different than a Random-Access-Memory. Here these type memories are mentioned as CAM and RAM in short forms throughout the chapters. Normally in RAM an operating system must uses the memory address to obtain the data stored at this address location. But in CAM an operating system operates in opposite manner, here the operating system must uses the data stored and meanwhile CAM work is to produce the address location in the memory where the data is located. In a regular type memory like RAM the memory can access only one location at a time. Where as in CAM can access the entire memory locations in a single operation, hence we can conclude that CAM is comparatively fast memory than RAM. But the designing a CAM will leads to complex design and also expensive in building it. It also consumes much power and generates heat into the system during high speed manipulations.

Thus it concludes that CAM has a disadvantage of high power dissipation during the matching and searching contents. The proposed method includes the design of 5 bit wide 4×5-TCAM array using reversible type gates and also presents the 4×3-TCAM array along with a basic TCAM cell. A SRAM cell is also designed with reversible objects for storing data bit in the TCAM cell. The match-line and the search-line are also realized with reversible gates. This proposed scheme incorporates several reversible-logic gates into the design which are named as Feynman Gate, Fred kin Gate and Peres Gate. The entire design modules are verified and simulated with the help of Xilinx-ISE simulator.

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II. LITERATURE REVIEW

Content addressable memory is of two types based on the types of bits stored in it. Each and every CAM cells will have their own comparison and search circuitry in order to search and gives the address of the matched data. Binary CAM can store logic '0' and logic '1' whereas ternary CAM can store logic '0', logic '1' and don't care. Thus in TCAM, the stored key 11x can match any one of the search keys of 110 or 111. TCAM cells are arranged in the 2D array format. The row cells will have common match line which is used to enable or disable the whole row based on matching condition or mismatching condition. The column cells will have common search line which is used to search the whole column. Figure 1 shows the usage of TCAM in routing table. The search data are given through the search registers. The address look up matches both entry 2 and entry 3. By using longest prefix matching method entry 2 will be selected and its address is passed to the priority encoder. This will be decoded and the corresponding address will be matched by the RAM. One approach that is well defined in the literature for practical implementation of reversible circuits is to never turn a switch ON or OFF when there is either voltage across it or current going through it. Reversible energy recovery logic uses this approach in order to avoid the non-adiabatic losses, which is essential for an ultra low power energy system. As a proof of concept for low power energy consumption using reversible logic, an ultra low power 16-bit carry look ahead adder was proposed in [7] using reversible energy recovery logic.

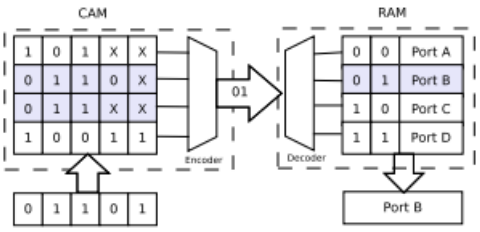

Fig. 1: Application of TCAM in Routing Table

III. REVERSIBLE ELEMENTS

This section discusses about the basics of reversible elements. According to the definition of the reversible circuit, there should not be any loss in the information. The design constraints in the reversible circuit is that the input and output vectors must map uniquely. There should be equal number of inputs and outputs and fan outs are not allowed in the design. Feedback from the output to the input of the same gate is not allowed. The design parameters in the reversible element design are quantum cost, worst case delay and the garbage output. Quantum cost is defined as the number of 1×1 reversible gate or 2 × 2 reversible gates. Worst case delay is defined as the number of delay units to produce the output for the given input. The worst case delay of the 1×1 reversible gate is defined as 1 unit of delay. Garbage output is the number of unused output to ensure the reversibility property of the circuits designed. Feynman [4] has proposed the 2 × 2 Feynman gate which performs the operation of the ex or gate. Figure 4 shows the 2 × 2 Feynman gate with inputs and outputs. Figure 5 shows the 3 × 3 Fredkin gate with inputs and outputs. As per the definition of quantum cost, the quantum cost of 2 × 2 Feynman gate is 1 and 3 × 3 Fredkin gate is 5. Feynman gate can be used as the fanout gate with one input as 0. Feynman gate can also act as not gate with the B input as 1 which will invert the value of A.Fredkin gate can act as multiplexer with the input A as the selection line. Peres [8] has introduced 3 × 3 Peres gate. Figure 6 shows the Peres gate. Peres gate can be used as logical NAND or AND gate based on the values of input C.

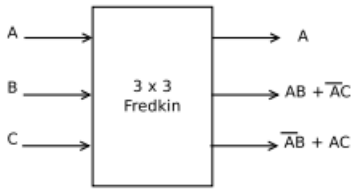

Fig. 5: Fredkin Gate

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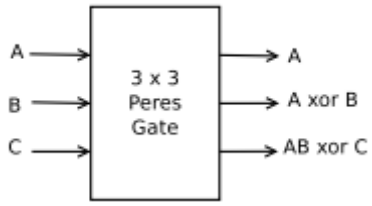

Fig. 6: Peres Gate

The quantum cost of the Peres gate is 4 and the worst case delay is 4. Reversible element based SRAM cell was designed in [9]. The main disadvantage in the design [9] is that quantum cost of the proposed SRAM cell can be further reduced and the reversible decoder proposed does not contain enable signal which is essential for chip select.

IV. SRAM CELL BASED ON REVERSIBLE ELEMENTS

This section discusses about the novel SRAM cell design based on reversible elements. Figure 7 shows the proposed SRAM cell using reversible gates. In this design, 3×3 Fredkin gate and the 2 × 2 Feynman gate is used to form the SRAM cell which is used to store the single bit of information. Each and every SRAM cell will have word line (W L) in order to make the SRAM cell to function in one of the modes that is either in read/write or hold state. If the value of the W L = 0 then the previous value has to be hold by the SRAM cell. If the value of W L = 1, then the SRAM will be in any one of the read/write state based on the external write/sense circuits.The WL output in the SRAM cell is used to enable the row cells which emulate the functionality of the conventional SRAM cell. Quantum cost for the proposed SRAM cell is 6. Figure 8 shows the SRAM cell with read/write enable with the row decoder. The quantum cost of this design is 16 which is still less as compared to the SRAM cell proposed in [9]. This design is used to store the bit in the TCAM memory cells. The design proposed in Figure 8 emulates the functionality of SRAM array with the reversible read circuits, reversible write circuits. The row decoder in [10] is used in the designing of SRAM array.

The quantum cost of the decoder proposed in [9] is 10 whereas the quantum cost of the decoder proposed in [10] is 15. But the decoder proposed in [10] is with the enable bit which is very essential in the design of memories for the chip select.

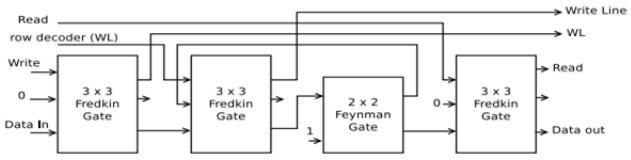

Fig. 7: SRAM Cell using Reversible Gates

TABLE I: Truth Table for Proposed Reversible TCAM Cell

Data Stored	Search Bit	Match Bit	Match-line State
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 8: Reversible SRAM Cell with Read and Write Signals

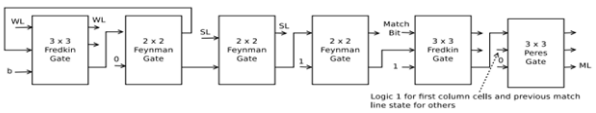

Fig. 9: Reversible TCAM Cell

V.OVERVIEW OF PROPOSED 4×5-TCAM-ARRAY

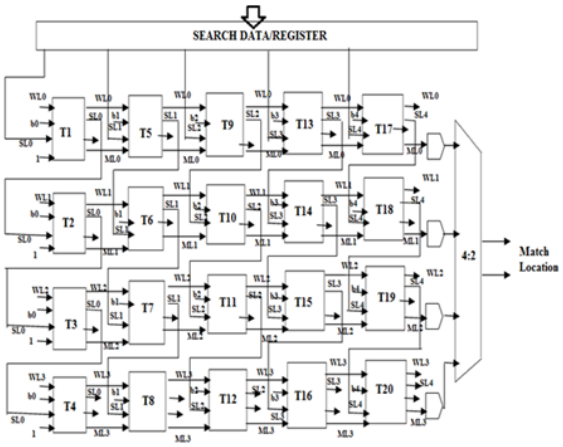

Figure 5.1.1: Proposed 4×5-TCAM array

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The 4×5-TCAM array is as shown in figure 5.1.1, which is having the array of 20 TCAM cells and one 4:2 encoder. This design looks almost like the design of 4×3-TCAM array, only the difference in width of the search bits. This scheme helps us in searching and matching of 5 bits wide data. Again this final design is having 4 rows and 5 columns. Each of the four rows has a common-match-line and each of the five columns has a common-search-line. The TCAM cells arranged along the common matching line are stored with data bits with the help of SRAM cells. And the search bits are passed to column TCAM cells through common searching lines from the search-data registers.

If any one of the same row cells having the match line status low then the status of the common-match-line of entire row becomes low. And if all the cells in the same row having the match-line status high then the status of the common-match-line of that entire row becomes high. The functioning of this proposed scheme is similar to the farmer method with broader searching capability.

The match line status also depends upon the match-bit 'Mb' applied that is considered as don't care bit. It helps in broader searching of data. Whenever the match-bit is high then the match line status becomes always high regardless of the applied inputs. At the end of the each row we get the match line status. It means four match line status at each row end and these status signals are fed to a 4:2 encoder which selects among the four status lines of addresses and gives exact match line address at its output.

VI. OPERATION OF 4 ×5-TCAM-ARRAY

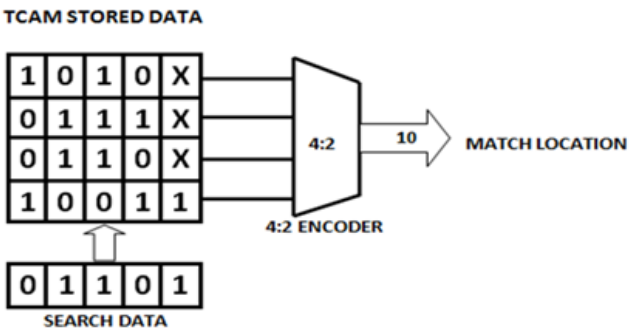

Figure 5.2.1: Operation of 4×5-TCAM array

The operation of the proposed 4×5-TCAM-array can be easily understood through the figure 5.2.1. The TCAM cells in the four different rows contain stored bits. Each row stored with a predefined content value like 1010X, 0111X, 0110X and 10011 respectively. The search bits are sent from search data registers through the five column TCAM cells. Assume the search data here is 01101 which is compared with all row contents. The stored data also contains don't care bits at the end bit. Each bit of the search data is compared with each bit of column data. If both of the stored data bit and search bit matches then the particular TCAM cell shows its match line status as high. If mismatching happens then that particular TCAM cell shows match line status as low. If and only if all the bits of stored data and search data are matched then only the corresponding row line status becomes high. If a single TCAM cell in the same row shows low status then the entire row will be at low status. The below mentioned four conditions show the operation of the TCAM cell. It makes us to find out the match line address where the search data is available and found by comparing and matching operations by TCAM cell.

- If first row gives match line status high then encoder output is '00'.
- If second row gives match line status high then encoder output is '01'.
- If third row gives match line status high then encoder output is '10'.

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- If fourth row gives match line status high then encoder output is '11'.

VII. SIMULATION RESULTS

All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

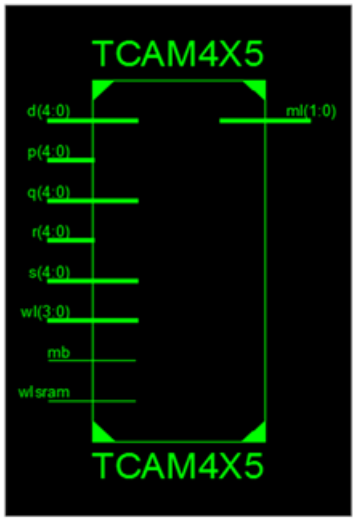

Figure 5.3.1: Block Digram of Proposed 4×5-TCAM-array

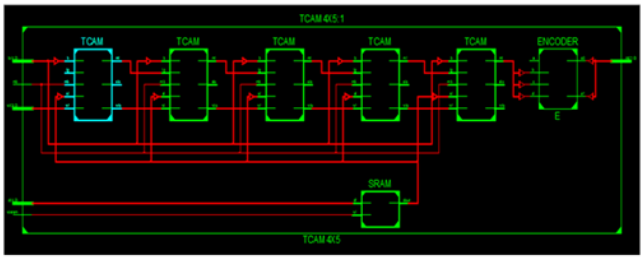

Figure 5.3.2: Internal Architecture of Proposed 4×5-TCAM-array

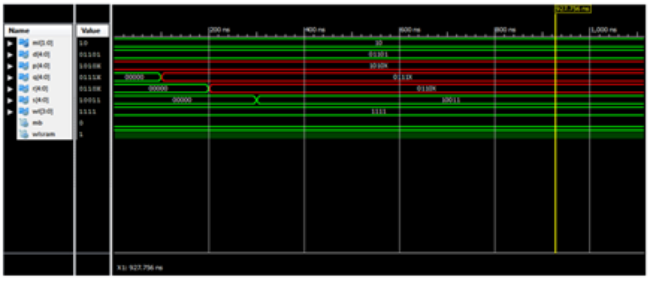

Figure 6.2.9: Simulation Waveforms of Proposed 4×5-TCAM-array

VIII. CONCLUSION AND FUTURE WORK

The proposed work is a design of 4×5-TCAM array using reversible-logic-entities. This array can be helpful in matching and searching up to 5 bit wide length of data. The design comprises of four matching lines along row wise and five search lines along column wise. It allows us to search a 5 bit wide data among four 5 bit stored data. The functioning of this design is similar to the functionality of farmer TCAM array. And hence this design could be used in routing table for looking-up addresses, in high-speed networking instruments and switches. This project work also included with the designs of a SRAM cell, TCAM cell and the farmer design of 4×3-TCAM array by using the reversible gate entities such as 2×2-Feynman gate, 3×3-Fredkin gate and 3×3-PERES GATE. The design also used one 4:2 Encoder for the selection of four match lines status as inputs and gives the single match line status as output. The entire designs are synthesized, verified and simulated by using the XLINX provided XST tool.The future invention about the TCAM designs is to optimize the design using nanotechnology which may definitely optimize the design and increases the efficiency of the networking related equipments.

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