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A New Approach for Designing of 3 to 8 Decoder and It's Applications Using Verilog HDL

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ABSTRACT

In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Decoding is necessary in applications such as data multiplexing, 7-segment display and memory address decoding. Reversible logic has received great importance in the recent years because of its feature of reduction in power dissipation. It finds applications in low power digital designs, quantum computing, nano technology, DNA computing etc.Large number of researches are currently going on sequential and combinational circuits using reversible logic.

Decoders are one of the most important circuits used in combinational logic. Different approaches have been proposed for their design. In this article, we have proposed a novel design of 2:4 decoder and have used it to build a 3:8 decoder. The quantum cost for 3:8 decoder using the proposed design has been compared with a previously existing designand the design has been generalised to decoder with n inputs. A mathematical estimation of the quantum cost for n inputs decoder has been provided. The proposed design is synthesized and simulated on xilinx14.4 ISE and the simulation result verifies the correctness of the proposed design.

*Index Terms—**Reversible computing; Combinational logic; 2:4 Decoder; n:2^n Decoder; Reversible gates.***

I.INTRODUCTION

Landauer showed that the heat generated during computation is not due to the processing of bits, but due to the loss of information. Wiping of each bit of information causes a kTln2 amount of heat dissipation where k is the Boltzmann constant = 1.3805 × 10−23 J/K and T is the temperature in absolute scale. While this heat may be negligible for a single wipe of information, in modern VLSI design, where many chips are arranged in small region and millions of instructions are processed per second, the information loss and consequently the heat generation is formidable.

Bennett later showed that this heat dissipation can be avoided by using reversible computation.This proof by Bennett has led to an extensive research on reversible logic. Most prominent applications of reversible logic are seen in quantum computation, low power CMOS design, nanotechnology and DNA computing.Quantum networks are composed of quantum logic gates- each gate performing an elementary unitary operation on

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one, two or more than two state quantum systems called aubits.Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1.Any unitaryoperation is reversible and hence quantum arithmetic must bebuilt from reversible logic components.

Quantum cost, delay, number of constant inputs and garbageoutputs are the most important cost metrics of reversiblecomputing. Garbage outputs are the outputs which are presentonly to maintain reversibility and do not perform any useful operations. Number of gates is not a good measure of cost, since more than one gates can be taken together to form a new gate, thus reducing the gate count.Quantum gates involving many qubits are extremely difficult to build. Hence quantum cost is an important metric to build quantum gates. Quantum cost is the number of elementary quantum gates required to build the gate. 1*1 reversible gates viz. NOT gate have quantum cost 0 while 2*2 gates viz. Controlled-V, Controlled-V† , CNOT gate etc. have quantum cost 1.

Design of combinational sequential circuits has been ongoing for some time.Various proposals are given for the design of adders, subtractors, multiplexers, decoders etc. Recently a new reversible SG gate has been proposed.Though the provided design is of a 4 qubit gate, the encoding logic enables the gate to be extended to n qubits gate for any n > 4 and the authors have shown this gate to be universal.In this paper, we have proposed a novel design of 2:4 decoder whose quantum cost is less than the previous design. A design has also been proposed to extend the 2:4 decoder to higher dimension and a mathematical estimation of the quantum cost for n:2 n decoder has been provided.

II. BASIC REVERSIBLE GATES

Reversible gates are n*n logic gates where the input vectors I = I(i1; i2; : : : ; in) are mapped to the output vectors O = O(o1; o2; : : : ; on). The mapping is bijective, i.e., every input is mapped to an output and every output has a unique input mapped to it. Thus the outputs of reversible gates are permutations of the inputs. Fan-outs are not allowed in reversible circuit since they violate one-to-one mapping. Some basic reversible gates are introduced in this section.

A. NOT Gate

The simplest reversible gate is NOT gate. It is a 1*1 gate with quantum cost 0. NOT gate simply flips the input as shown in Fig. 1.

Fig.1. NOT gate

B. Controlled -V and Controlled -V+ Gate

Controlled -V and Controlled -V y gates are 2*2 reversible gates with quantum cost 1. In Controlled-V gate, if the control signal A = 0, then the second input B passes unchanged. However, if A = 1, then the unitary operation

$$\frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$$

is applied to the input B. Controlled-V y gate is simply the conjugate transpose of Controlled-V gate.

Controlled-V and Controlled-V y have the following properties:

$$V \times V = NOT$$
$$V \times V^{\dagger} = V^{\dagger} \times V = I$$
$$V^{\dagger} \times V^{\dagger} = NOT$$

Hence Controlled-V is also called the square root of NOT gate. Quantum implementation of V and V^{+} are shown in Fig.2.

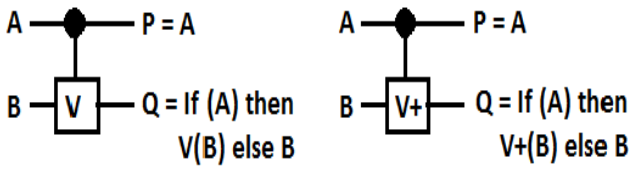

Fig.2. Quantum Implementation of Controlled-V and Controlled-V+ Gate

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C. Feynman Gate

Fig. 3 shows the block diagram and the quantum implementation of Feynman Gate [8], also called Controlled-Not (CNOT) gate. It is a 2*2 gate and its quantum cost is 1. The inputs are A and B and the outputs P = A and Q = A xor B.

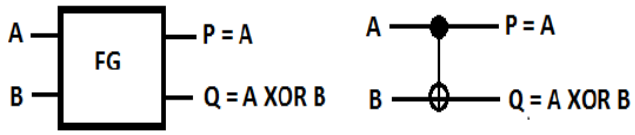


Fig.3. Block diagram and Quantum representation of Feynman Gate

D. Peres Gate

Fig. 4 shows the block diagram and quantum realization of Peres Gate [9]. It is a 3*3 gate with inputs A, B and C and the outputs P = A, Q = AxorB and R = ABxorC. Its quantum cost is 4 since four 2*2 gates are required for its realization.

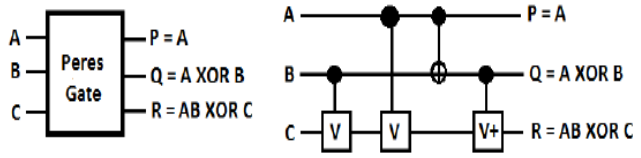
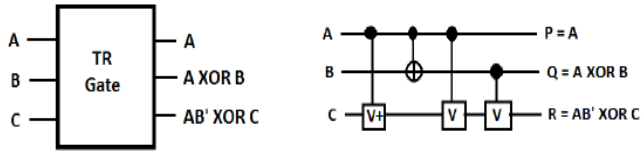


Fig.4. Block diagram and Quantum representation of Peres Gate

E. TR Gate

Fig. 5 shows the block diagram and quantum realization of TR Gate [10]. It is a 3*3 gate with inputs A, B and C and outputs P = A, Q = AxorB and R = AB'C. Its quantum cost is 4 since four 2*2 gates are required for its realization



.Fig.5. Block diagram and quantum implementation of TR Gate

F. Fredkin Gate

Fig. 6 shows the block diagram and quantum realisation of Fredkin Gate [11]. It is a 3*3 gate with inputs A, B and C and outputs P = A, Q = AB + A'C and R = A'B + AC. Its quantum cost is 5 since five 2*2 gates are required for its realisation.

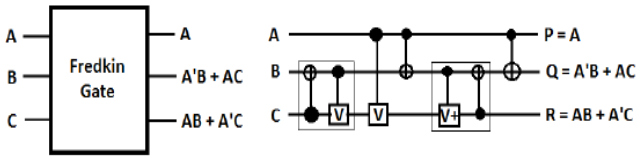


Fig.6. Block diagram and quantum implementation of Fredkin Gate

III.PROPOSED DESIGN OF 2:4 DECODER

A single Fredkin gate is capable of working like a 1:2 decoder if the first input is IN1, while the second and third inputs are 0 and 1 respectively.

Fig.7. Single Fredkin Gate as 1:2 Decoder

A design of 2:4 decoder using 3 Fredkin gates has been proposed, as shown in Fig. 8. The quantum cost ofthis design is 15. A proposal has been given for 4:16 decoder usingthis 2:4 decoder. The 4:16 decoder requires 15 Fredkingates.Hence the quantum cost of the design is 75. In the nextsubsection, we propose our architecture of 2:4 decoder anduse it to design a 4:16 decoder having lower quantum cost.

A. Design and operation of proposed 2:4 decoder

If x and y are the inputs to the decoder, then the four outputswill be xy, x'y, xy' and x'y'. The proposed design uses PeresGate, TR Gate and CNOT Gate as shown in Fig. 9.

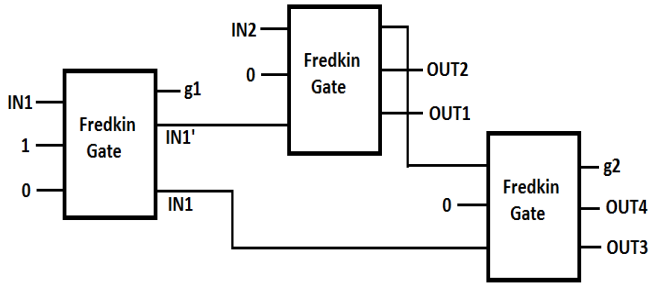


Fig.8. Previously proposed 2:4 decoder

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The Peres gate gives outputs $x \oplus y$ and xy. It is notable that $(x \oplus y)' \oplus xy = x'y'$. A NOT gate is used to flip the output $x \oplus y$ which does not increase the quantum cost. Similarly the TR gate gives outputs $x \oplus y$ and xy' and the XOR of these two gives x'y. So simply by using three more CNOT gates, all four outputs are available. The total quantum cost of this design is 11, since Peres Gate and TR gate both have quantum cost 4 and CNOT gate costs 1.

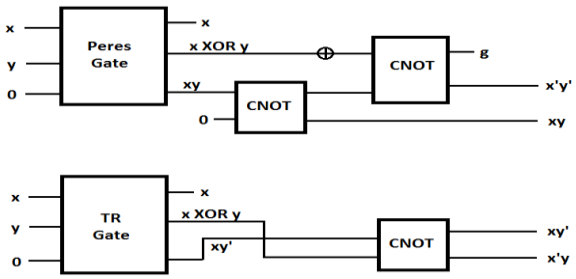

Fig.9. Proposed 2:4 decoder using Peres, TR and CNOT gates

The number of garbage output in this architecture is 1 (not counting the output x in both Peres and TR gates since they will be required to build larger circuits using this decoder).

B. Design of 3:8 decoder

Hence, we shall call the 2:4 decoder as decoder block having two inputs and four outputs. A 3:8 decoder has the outputs x'y'z', x'y'z, xy'z', xy'z, x'yz', x'yz, xyz', xyz. So every output of the 2:4 decoder needs to be multiplied twice, once with z'and then with z . To achieve this using Peres or TR gate, there will be need of a single gate for each multiplication,resulting in 8 gates with a quantum cost of 32 and 16 garbageoutputs (2 for each gate).A better model will be to use Fredkin gate for higher dimension. Each Fredkin gate is capable of performing two multiplications thus reducing the number of gates to 4 and garbage outputs to 1. The architecture is shown in Fig. 10. So to build 4:16 decoder, 8 extra Fredkin gates will be required. So total number of Fredkin gates is 12. Hence the quantum cost is 60 and the 2:4 decoder block costs 11. So the ultimate quantum cost of 4:16 decoder will be 71.

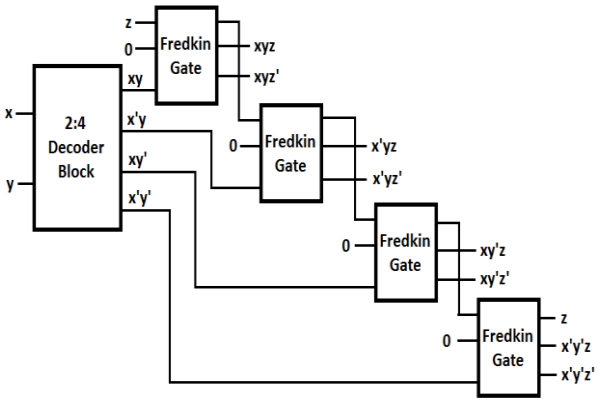

Fig.10. 3:8 decoder using 2:4 decoder block and Fredkin Gates

C. Generalisation to n: 2n decoder

The design of decoder can be generalised to n: 2n for any n > 2 in similar manner. If we have a (n − 1): 2(n−1) decoder, then to build a n: 2n decoder, 2 (n−1) Fredkin gates are necessary. Hence the quantum cost of the design increases by 5 ∗ 2 (n−1). In this manner, 2:4 decoder can also be built [12], but the proposed design has lower quantum cost.

IV.SIMULATION RESULTS

A.RTL Schematic

All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

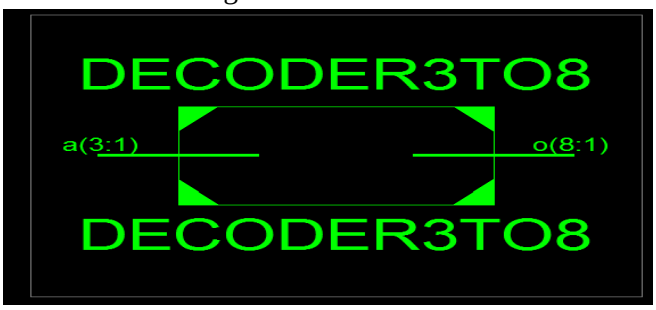

Fig.11. RTL schematic of proposed reversible 3to8 Decoder

B.RTL Sub Schematic

The sub schematic of proposed 3 to 8 decoder is shown in below figure.

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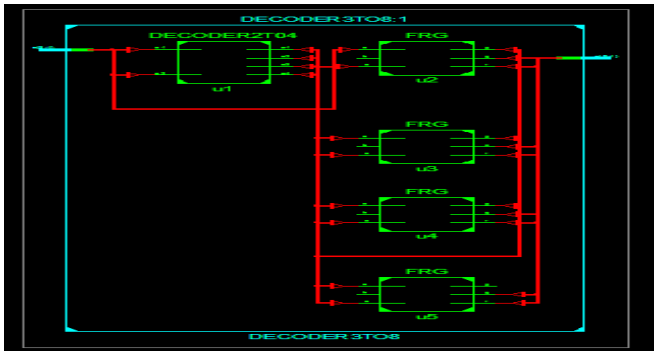

Fig.12. RTL sub schematic of proposed reversible 3to8 Decoder

C.Technology schematic

The Technology schematic of proposed reversible 3 to 8 decoder is shown below.

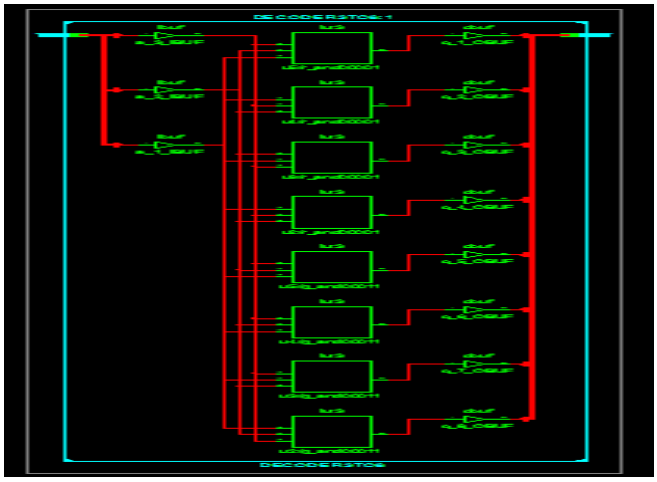

Fig.13. Technology schematic of proposed reversible 3to8 Decoder

D.Simulation

The simulation of proposed reversible 3 to 8 decoder is shown below.

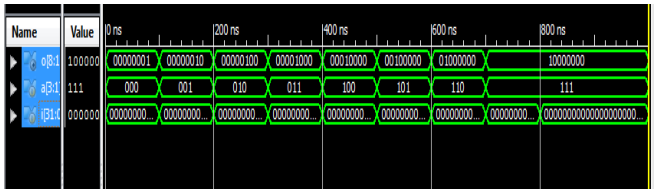

Fig.14: Simulation of proposed reversible 3to8 Decoder

V. Future Scope

A large number of researches are going on sequential and combinational circuits using reversible logic gates.Decoders are one of the most important circuits in combinatonal logic.The design of 2to4 decoder with two fredkin gates is previously proposed and design of 3to8 decoder using 2to4 decoder with four fredkin gates is proposed now.In future we can design 4to16 decoder with twelve fredkin gates.Hence the quantum cost of 4to16 decoder is lower.We can give ‘n’ number of inputs according to our requirement and then we get ‘2^n’outputs.

VI. CONCLUSION

Hence we have proposed a novel design of 2:4decoder and have used it to build a 3:8 decoder. We haveshown that the quantum cost of a n : 2n decoder will be lessby 4 if we use our proposed 2:4 decoder block.The increase in the number of Fredkin gates is exponentiallyhigher for increase in a single input. Though for n inputs, thenumber of outputs is 2n. Hence, from the point of view of thenumber of outputs, the increase in gates is linear. However,by using any other gates like Toffoli, Peres or TR gate, thenumber of gates will be twice as high and hence the quantumcost will be nearly twice. The number of garbage outputs alsoincreases in the same manner since each Fredkin gate has onegarbage output for this architecture.Thegeneralised design cannot be optimised any furtherby using the basic gates like Peres, TR or Toffli. However,further research interest may be to propose new gates thatcan be used to replace Fredkin gates in higher dimensionaldecoders, resulting in decrease of quantum cost.

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