ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of Low power and Area Efficient 8-bit ALU using GDI Full Adder and Multiplexer

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Abstract:
The low power techniques are becoming more important due to rapid development of portable digital applications, demand for high-speed and low power consumption. GDI (Gate Diffusion Input) is one of the low power and area efficient technique. GDI requires less number of transistors compared to CMOS technology. Arithmetic logic unit (ALU) is an important part of microprocessor. In digital processor logical and arithmetic operation executes using ALU. In this paper we describes 8-bit ALU using low power 11-transistor full adder (FA) and Gate diffusion input (GDI) based multiplexer. By using FA and multiplexer, we have reduced power and delay of 8-bit ALU as compare to existing design. All design were simulated using DSCH and Microwind 3.5 in 65 nm BSIM4 technology. Performance analyses were done with respect to power, delay and power delay product.

Keywords:
Gate diffusion input (GDI), 8-bit ALU, Full Adder.

I. INTRODUCTION

ALU is the section of the computer processor that executes arithmetic and logical operation. ALU is an exclusively combinational logic circuit which means output changes with changing of input response. The ALU is a utile device in microprocessor, performing various logical and arithmetic operations [1]. Exploitation of very large scale integration (VLSI) technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal oxide semiconductor (CMOS) has been the backbone in mixed signal because it reducing power and providing good mix component for analog and digital design.

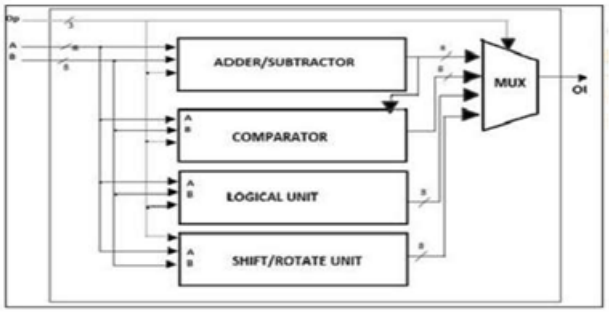

Fig. 1. Internal Architecture of ALU.

The mainstays of power consumption in CMOS circuits are static power (P_s), dynamic power (P_d) and short circuit power (P_{sc}). Thus, the total power consumption (P_t) is

$$P_t = P_s + P_d + P_{sc} \quad (1)$$

P_s is caused by leakage current between the diffusion region and the substrate. P_d consumes due to capacitive load and clock frequency and P_{sc} is caused by short circuit current. Increasing number of transistors per chip area and scale down technologies have consumed more power thus the main objective is to reduce the power consumption by using different techniques for improving performance of VLSI circuits.

II. PREVIOUSWORK

Power can be reduced either architecture level or module level or circuit level. In analog switch technique select input logic as a control logic and passes another input signal from gate terminal [4]. FA is a basic building block for designing ALU, different types of FA designing for minimizing power such as hybrid FA, low power 10 transistors FA and 11 transistor FA.

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FA operating in ultra-low mode by using sub-threshold current and consumes low power [2]-[3]. FA build using low power XOR gates and 2 is to 1 multiplexer [7]. ALU design using Fin FET technology has two gates which are electrically independent, minimize the complexity of the circuit and also reduce the power consumption due to reducing the leakage current. In Fin FET technology "Fin" is a thin silicon which mould the body of the device [5]. ALU design using the reconfigurable logic of multi input floating gate metal oxide semiconductor (MIFG-MOS) transistor have multiple inputs, increased the functionality of the circuit. MIFG-MOS transistor gives ON and OFF states of the transistor by observing weighted sum of all inputs. MIFG-MOS transistor reducing the number of transistor and complexity of the circuit, improve the performance of the circuit minimize the delay and reduced the power dissipation [6]. When channel length is scale down for designing circuits, metal gate and high-k dielectric is to be introduced. Metal gate and high-k dielectric gives extra channel length without put down the leakage current [8].

III. CIRCUIT DESIGN OF ALU

ALU is a core part of computer or digital processor that executes arithmetic and logical operation, such as increment, decrement, addition and subtraction as an arithmetic operation and AND, OR, XOR, XNOR as a logical operations as shown in table 1. The symbol of ALU is in fig1. ALU is build by using FA and multiplexer.

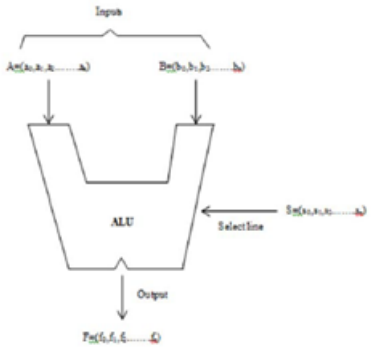

Fig. 2. Symbol of ALU

TABLE I. TRUTH TABLE OF ALU

S_2	S_1	S_0	OPERATION
0	0	0	OR
0	0	1	XNOR
0	1	0	XOR
0	1	1	AND
1	0	0	INCREMENT
1	0	1	ADDITION
1	1	0	DECREMENT
1	1	1	SUBTRACTION

A. 11 Transistor Full Adder (11TFA)

FA is basic functional module for designing ALU. 11T used for design of FA, this modern design of FA is minimize the power and reduced the delay. FA depicts in Fig. 2, circuit is operating at power supply (V_{DD}) 0.9V. Input A apply to the gate terminal of PMOS_1 and NMOS_1, drain terminal of PMOS_2. Input B apply to the gate terminal of PMOS_2 and PMOS_2, drain terminal of NMOS_1. When source voltage (V_S) is greater than threshold voltage (V_{TH}) transistor is ON and pass the signal from gate terminal to drain terminal means pass the gate voltage (V_G) to drain terminal.

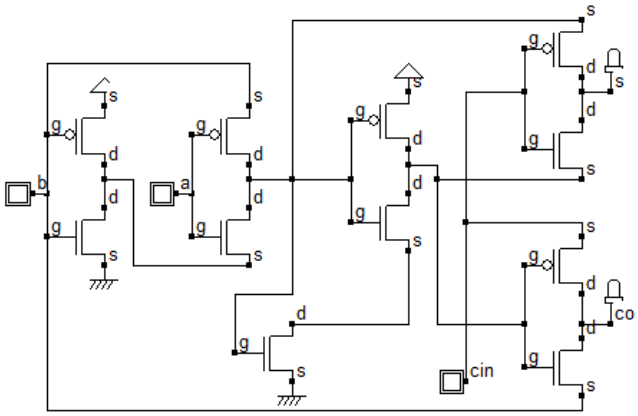

Fig. 3. Schematic of 11T FA

Thus, when input A is high, pass the input B vice versa. FA is build using low power XOR gates and 2 is to 1 multiplexer. XOR gates gives the sum output and multiplexer responsible for carry out (C_{out}). An extra transistor NMOS_6 operates in ultra-low mode using sub-threshold current and consumes low power.

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At strong inversion region gate to source voltage (VGS) is higher than threshold voltage (VTH), majority carriers removed from the area of gate and minority carriers is produced, at weak inversion region VGS is below than VTH less minority carrier is produced, but their presence produce leakage current this current is called subthreshold current. This current can be used when VDD is below then VTH and run the circuit at ultra-low mode and consumes less power. 11T FA is operating at sub-threshold mode by adding an extra transistor NMOS_6.

B. GDI based Multiplexers

GDI technique is area efficient technique which consumes less power with reducing the number of transistor. GDI technique need twin well process or silicon on insulator for chip composition. Twin well process gives separate optimization of n-type and p-type transistor and also optimizes gain and VTH of n-type and p-type device. Silicon on insulator combined both MOS and bipolar technologies into a single process.

GDI technique providing an extra input for the cell and maintain the circuit complexity. GDI technique solves the problem of poor ON to OFF transition characteristic of PMOS and providing the full swing at internal node of circuit. Fig. 3 depicts the 2 is to 1 multiplexer, select line S is common input for gate terminal of PMOS_1 and NMOS_1. Input A and Input B is connected to the source terminal of PMOS_1 and NMOS_1 respectively. When S is low then PMOS_1 is ON and pass the input A from source terminal to drain terminal, when S is high NMOS_1 is ON and PMOS_1 is OFF. Output is common for drain terminal for PMOS_1 andNMOS_1.

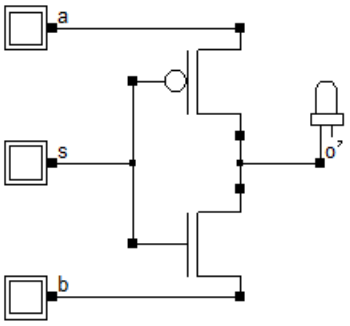

Fig. 4. GDI based MUX 2

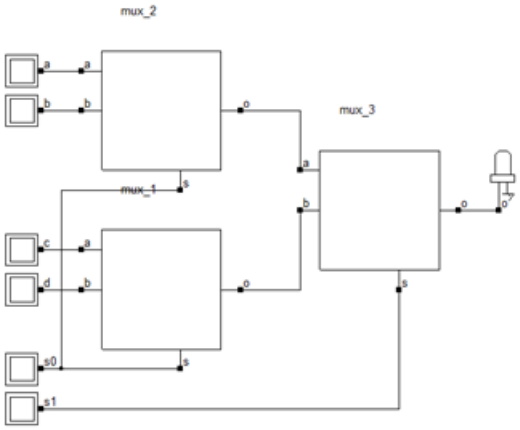

Fig. 5. GDI based MUX 4

Fig. 4 depicts the 4 is to 1 multiplexer, 4 is to 1 multiplexer design using three 2 is to 1 multiplexer. Select lines S0 and S1 is worked as a switching input which is responsible for the high and low states of the transistor, S0 is common input for gate terminal of PMOS_1, PMOS_2, NMOS_1 and NMOS_2, S1 is common input for gate terminal of PMOS_3 and NMOS_3. Inputs are connected to the source terminal of transistor.

C. Design of 8-bit ALU

FA is mainstays of ALU, 8-bit ALU is design using 8-bit ripple carry adder (RCA). RCA is responsible for arithmetic operation of ALU. Other modules needed for designing ALU are 2 is to 1 multiplexer and 4 is to 1 multiplexer. Logical operation executes by using multiplexer.

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Fig.5 depicts the 1-bit ALU, 1-bit ALU design using two 4 is to 1 multiplexer and one 2 is to 1 multiplexer and FA.

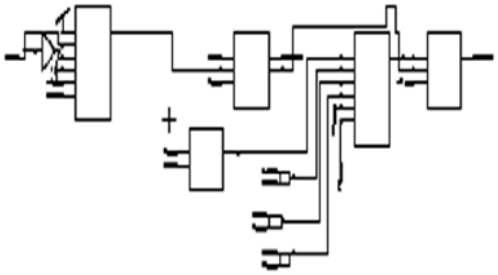

Fig. 6. 1-bit ALU

Fig. 6 depicts 8-bit ALU, RCA is basic building block of 8-bit ALU which is perform arithmetic operation. Input A ($a_0,a_1,\ldots a_8$) is apply in first input of RCA, Input B ($b_0,b_1,\ldots b_8$) is apply in first input of 4 is to 1 multiplexer and pass to the second input of RCA from output of 4 is to 1 multiplexer, and executes arithmetic operation. Logical operation executes through the cascading combination of 4 is to 1 multiplexer and 2 is to 1 multiplexer.

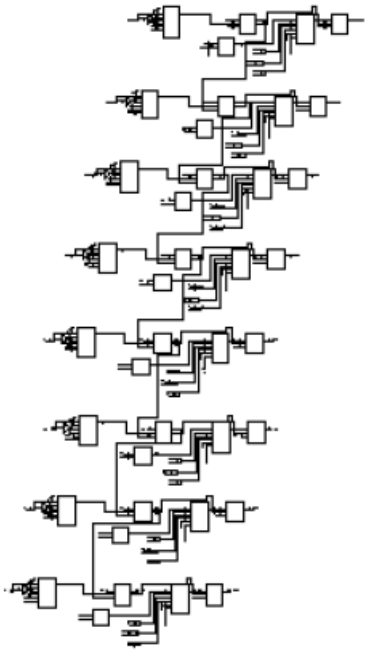

Fig. 7. 8-bit ALU

IV. SIMULATION AND RESULT

All design is to be simulated using tanner eda tool W-edit at transition time 80ns. Fig. 7 shows the waveform of 11T FA, at input combination "000" to "111". At "000", "010" and "110" problem is occur, this problem is solved by adding an extra transistor NMOS_6.

Fig. 8. Waveform of 11-T FA

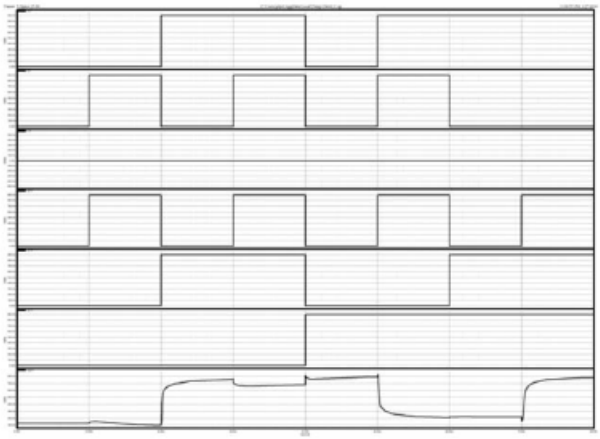

Fig. 9. Waveform of 1-bit ALU

Fig. 8 shows the waveform of 1-bit ALU. Simulation is done with select line combination "000" to "111". When select line S_2 is high ALU performs logical operation and S_2 is low ALU performs arithmetic operation. When select line combination is "000" then ALU performs OR logical operation and at "001", "010" and "011" combination ALU performs XNOR, XOR and AND logical operations respectively. From "100" to "111" combinations ALU performs arithmetic operation.

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At "010", "011" and "111" combination output gives 0.75V which is higher than the V_{TH}, so we consider these outputs as a logic1. Table II and Table III shows the comparison between CMOS logic based design and proposed design with respect to power, delay and power delay product at 32nm technology. Using proposed logic, 8-bit ALU consumes 31% less power as compare to CMOS logic based 8-bit ALU and also minimizes the delay.

TABLE II. CMOS LOGIC BASED DESIGN AT 32NMTECHNOLOGY

Design	Power	Delay	PDP
14T FA	444.2nW	40.15ns	17834nW*ns
MUX2	270nW	40.68ns	10983nW*ns
MUX4	795nW	21ns	16695nW*ns
1-bit ALU	4.91µW	32.47ns	159.42 µW*ns
8-bit ALU	47.64 µW	31.8ns	1514.9 µW*ns

TABLE III. PROPOSED LOGIC BASED DESIGN AT 32NM TECHNOLOGY

Design	Power	Delay	PDP
11T FA	33nW	89.62ps	2957nW*ps
GDI based MUX2	68.8nW	15.83ps	1089nW*ps
GDI based MUX4	289nW	20ns	5780nW*ns
1-bit ALU	4.47µW	20.33ns	90.87 µW*ns
8-bit ALU	32.9 µW	6.95ns	228.65 µW*ns

V. CONCLUSION

In this paper, 8-bit ALU design using 11-T FA and GDI based multiplexer at 32nm technology. At 32nm technology high-k dielectric and metal gate is to be introduced.

There are three main sources responsible for occurring leakage current are the gate direct tunneling current, the sub-threshold leakage current and reverse biased junction leakage. High-k dielectric is permitted to increase the gate capacitance and reduced the leakage power due to gate direct tunneling current. Metal gate make better strain capacity. Sub-threshold leakage current is to be used at sub-threshold mode and consumes low power. Finally, 8-bit ALU performs better as compare to existing design and consumes low power.

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