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Design of Conditional-Boosting Flip-Flop for Ultra Low Power Applications

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Abstract:
Power consumption is considered as one of the important challenge in modern VLSI design along with area and speed consideration. Flip flop plays very important role in digital systems. In this paper comparative study of four different flip flops which includes pulse triggered as well as conditional technique flip flop such as IP-DCO, MHLFF, CPSFF, and CPFF topologies in sub threshold operation are examined. In recent years the ultra-low power application can be possible using sub threshold technology. Using the advantage of this technology the power consumption of these flip flops is minimized. Sub threshold circuit consume less power than strong inversion circuit at the same frequency. Design is done using HSPICE in TSMC 18nm technology. The flip flops are analysed in all corners and parameters such as delay, power delay product, Energy delay product, and average power is measured at power supply voltage 300mV, and applied clock frequency is 1 MHz at temperature of 270C.

Keywords:
Sub threshold technology, flip flop, low power.

INTRODUCTION:

As stated by International Technology Roadmap for Semiconductor power consumption is considered as one of the important challenge in VLSI along with speed and area consideration. Different ways for reducing the power consumption have been proposed [1].

In all these challenging methods minimizing power supply voltage gives direct and effect on reducing power consumption. Flip flops are major building blocks in digital VLSI system. The applications areas where flip flops are majorly used are in registers, pipelines, state machines for sequencing data. Flip flop have direct impact on power consumption and speed of VLSI system. Flip flop and latches consume more power because of redundant transitions & clocking system which is included in it. Thus our aim is to design high performance and also power efficient flip flop [2]. One of the challenging methods to design low power flip flop is to use sub threshold technology. Power consumption of circuit depends on several factors such as data activity, frequency, supply voltage, capacitance leakage and short circuit current. The total power dissipation is given by the sum of static and dynamic power dissipation. Amongst them dynamic power is one of the important and it is given by, $P_{Dynamic} = 0.5.\alpha\ CL.VDD^2.f$ ..... (1)
Where α is the probability of signal transition within clock period, CL is the load capacitance, VDD is the power supply voltage, f is clock frequency. Hence by reducing the power supply voltage there is tremendous reduction in power consumption of circuit. When supply voltage VDD reduces below the transistor threshold voltage V_T, it is said to operate in sub threshold region [3].

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This is one of the efficient methods for low power application in which the performance is of secondary importance. As power supply voltage is reduced below the transistors supply voltage V_T, the sub threshold current slowly charges and discharges nodes for circuits logic function. This weak driving current limits the performance but low energy operation can be achieved with reduced dynamic &leakage power, resulting in improving battery life. In sub threshold region due to absence of conducting inversion channels, transistors behave differently than in strong inversion region. Thus resulting circuit characteristics change accordingly [4]. Sub threshold technology can be used in various applications such as wearable medical equipment's such as hearing aids & pace makers, wrist watch acomputers, self-powered devices & wireless sensor networks. One more application of sub threshold circuits is in burst mode application, which is ideal for a long period of time. In sub threshold circuit it satisfies the ultra-power requirement. The reason behind this is that it uses leakage current for its operating switching current. This small leakage current however affects the performance at which the circuit is operated.

Existing System:

Capacitive boosting can be a solution to overcome the problems caused by aggressive voltage scaling. It allows the gate source voltage of some MOS transistors to be boosted above the supply voltage or below the ground. The enhanced driving capability of transistors thus obtained can reduce the latency and its sensitivity to process variations. The bootstrapped CMOS driver presented in relies on this technique to drive heavy capacitive loads with substantially reduced latency [5]. However, since it is a static driver, every input transition causes the bootstrapping operation. So, if some of the transitions are redundant, a large amount of redundant power consumption may occur. The conditional-bootstrapping latched CMOS driver proposes the concept of conditional bootstrapping to eliminate the redundant power consumption. As it is a latched driver, it can allow boosting only when the input and output logic values are different, resulting in no redundant boosting and improved energy efficiency, especially at low switching activity. Recently, differential CMOS logic family adapting the boosting technique has also been proposed for fast operation at the near-threshold voltage region [6].

PROPOSED FLIP FLOP DESIGNS

For incorporating the conditional boosting into a pre charged differential flip-flop, four different scenarios regarding input data capture should be considered, which are determined by the logic states of the input and output. These scenarios are as follows:

1) For a low output data, a high input data should trigger boosting for a fast capture of incoming data;
2) For a low output data, a low input data should trigger no boosting since the input need not be captured;
3) For a high output data, a low input data should trigger boosting for a fast capture of incoming data;
4) For a high output data, a high input data should trigger no boosting.

These scenarios can be embodied into a circuit topology using a single boosting capacitor by a combination of two operation principles. One is that the voltage presetting for the terminals of the boosting capacitor must be determined by the data stored at the output (so-called output dependent presetting). The other principle is that boosting operations must be conditional to the input data givento the flip-flop (so called input-dependent boosting) [7]. The conceptual circuit diagrams for supporting these principles are shown in Fig. 1.To support the output-dependent presetting, the preset voltages of capacitor terminals N and N Bare made to be determined by outputs Q and QB as shown in Fig. 1(a). If Q and QB are low and high N and NB are preset to be low and high [left diagram in Fig. 1(a)],and if Q and QB are high and low, N and NB are preset to be high and low [right diagram in Fig. 1(a)], respectively. To support the input dependent boosting, the non-inverting input (D) is coupled to NB through an nMOS transistor and the

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inverting input (DB) is coupled to N through another nMOS transistor, as shown in Fig. 1(b). Then, as one case in which a low data is stored in the flip-flop, resulting in the capacitor presetting given in the left diagram in Fig. 1(a),a high input allows NBto be pulled down to the ground, lettingNbeing boosted toward–V_{DD}due to capacitive coupling [upper left diagram in Fig. 1(b)] [8]. Meanwhile, a low input allows Ntobe connected to the ground, but since the node is already presetto V_{SS}, there is no voltage change at NB, resulting in no boosting [lower left diagram in Fig. 1(b)].

As the other case in which a high data is stored in the flip-flop, resulting in the capacitor presetting given in right diagram in Fig. 1(a), a low input allows Nto bepulled down to the ground, letting NBbeing boosted toward –V_{DD}due to capacitive coupling [lower right diagram in Fig. 1(b)].

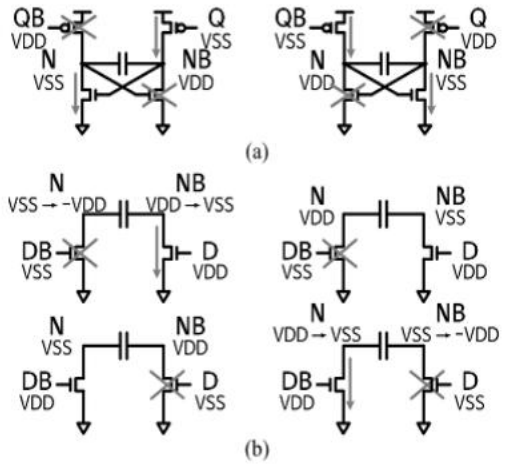

Figure 1: Conceptual circuit diagrams for (a) output data-dependent presetting

Meanwhile, a high input allows NBto be connected to the ground, but since the node is already preset to VSS, there is no voltage change at N, resulting in no boosting [upper right diagram in Fig. 1(b)].

Table I summarizes these operations for easier understanding. Withthese operations, any redundant boosting can be eliminated, resulting in a significant power reduction, especially at low switching activity.

Table 1: DATA-DEPENDENTPRESETTING ANDBOOSTING

	input (D)	output (Q)	boosting node (N)	boosting node (NB)
output-dependent presetting	-	VSS	VSS	VDD
		VDD	VDD	VSS
input-dependent boosting	D=VDD	VSS	VSS → –VDD	VDD → VSS
		VDD	VSS	VDD
	D=VSS	VSS	VDD	VSS
		VDD	VDD → VSS	VSS → –VDD

Circuit Implementation

The structure of the proposed conditional-boosting flip-flop (CBFF)based on the concepts described in the previous section is shown inFig. 2. It consists of a conditional-boosting differential stage, a symmetric latch, and an explicit brief pulse generator. In the conditionalboosting differential stage shown in Fig. 2(a), MP5/MP6/MP7and MN8/MN9 are used to perform the output-dependent presetting, whereas MN5/MN6/MN7 with boosting capacitor CBOOTareused to perform the input-dependent boosting. MP8–MP13 andMN10–MN15 constitute the symmetric latch, asshown in Fig. 2(b) [9].

Some transistors in the differential stage are driven by a brief pulsedsignal PSgenerated by a novel explicit pulse generator shown inFig. 2(c). Unlike conventional pulse generators, the proposed pulse generator has no pMOS keeper, resulting in higher speed and lowerpower due to no signal fighting during the pull-down ofPSB.Theroleof the keeper to maintain a high logic value ofPSBis done by MP1added in parallel with MN1, which also helps a fast pull-down ofPSB.At the rising edge ofCLK, PSBis rapidly discharged by MN1, MP1, and I1, lettingPShigh [10].

After the latency of I2 and I3, PSBis chargedby MP2, and soPSreturns to low, resulting in a brief positive pulseatPSwhose width is determined by the latency of I2 and I3. WhenCLKis low, PSBis maintained high by MP1, although MP2 is OFF. According to our evaluation, the energy reduction is up to 9% for the same slew rate and pulse width [11].

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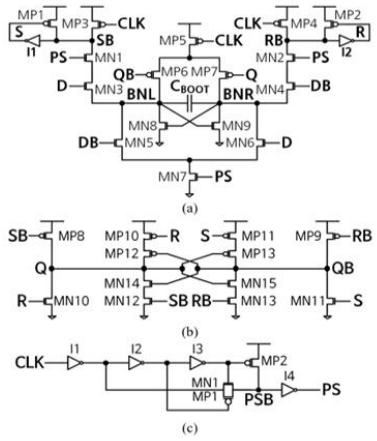

Figure 2: Proposed CBFF. (a) Conditional-boosting differential stage. (b) Symmetric latch. (c) Explicit brief pulse generator.

SIMULATION

A comparative study of above flip flop cells are performed with respect to parameters such as delay, power consumption, power delay product, energy delay product. The simulation results for above types of flip flop were obtained using HSPICE simulator. The operating conditions for design of the flip flop are V_{DD}=300mV, clock and input data frequency applied is 1MHz, temperature is 270C. The technology used for the flip flop design is TSMC 18nm. The parasitic capacitances were extracted from layouts to simulate circuit accurately.

By eliminating parasitic capacitances we can avoid delay which depends on these capacitances and more over power consumption also. Fig. shows the delay time variation of flip flops. It is seen fro the graph that MHLFF is having less delay as compared to other flip flops. Fig. shows the average power consumption of flip flop. The average power consumption is very less in CPSFF and MHLFF is having higher power consumption in our all four flip flop designs. Is having comparison of power delay product. The variations in average power for flip flop types. The value of CPSFF is lower than other flip flops. It shows that CPSFF gives the best performance amongst these four flip flops.

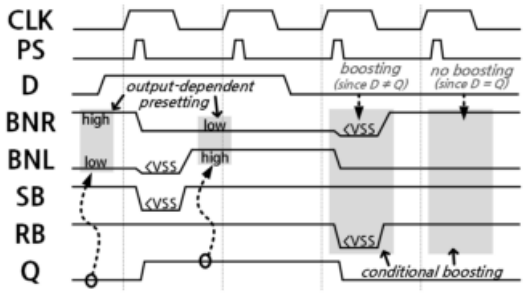

Fig. 3. Timing diagram of the proposed flip-flop.

TABLE II
FLIP-FLOP PERFORMANCE COMPARISON AT 0.5 V

	SCFF [5]	ACFF [6]	TCFF [7]	SAFF [3]	STFF-D [4]	CBFF	CBFF-SP
Structure	Single-end	Single-end	Single-end	Differential	Differential	Differential	Differential
Device count (EA)	24	22	21	26	32	43	34.75
Layout area (um²)	20	26	24	23	27	42	37
Setup time (ns)	2.86	5.92	8.4	-0.16	-2.59	-2.46	-3.45
Hold time (ns)	-0.2	2.87	2.94	1.85	3.51	3.16	4.17
Pulse width (ns)	-	-	-	-	-	4.09	5.98
CQ latency (ns, TT/27°)	3.6	3.27	8.59	3.8	5.4	3.49	4.43
DQ latency (ns, TT/27°)	6.32	9.6	16.9	3.7	2.8	1.03	1.05
σ of DQ latency (ns, TT/27°)	0.73	0.68	3.87	0.32	0.56	0.082	0.083
Energy (D, α = 25%, TT/27°)	1.98	1.83	1.43	3.63	4.3	6.21	4.25
EDP (yJs, α = 25%, TT/27°)	12.5	17.6	24.2	13.4	12.1	6.36	4.44

RESULTS

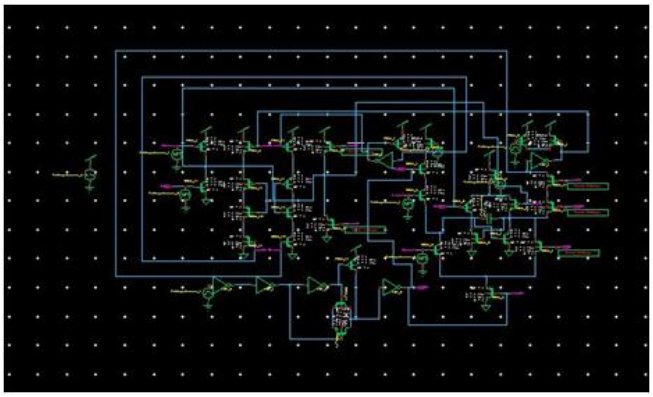

Fig :4 Schmatic digram of Proposed CBFF.

Power

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Power Results

VVoltageSource_7 from time 0 to 100
Average power consumed -> 9.373288e-015 watts
Max power 6.271342e-004 at time 1.60632e-007
Min power 0.000000e+000 at time 0
```

Delay

```
Parsing                    0.01 seconds
Setup                      0.02 seconds
DC operating point         0.28 seconds
Transient Analysis         0.19 seconds
Overhead                   0.42 seconds
-----------------------------------------
Total                      0.92 seconds
```

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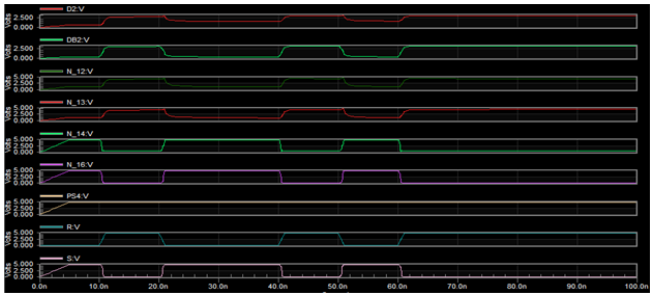
Area

```
Device and node counts:
              MOSFETs -       32
    MOSFET geometries -        3
           Capacitors -        1
      Voltage sources -        7
          Subcircuits -        2
    Model Definitions -       21
      Computed Models -        2
    Independent nodes -       18
       Boundary nodes -        8
          Total nodes -       26
** 12 WARNING MESSAGES GENERATED DURING SETUP
```

SIMULATION RESULTS



CONCLUSION

For aggressive voltage scaling down to the near-threshold voltage region without severe performance degradation, a novel CBFF hasbeen proposed. The evaluation in a 18-nm CMOS process indicates that the proposed flip-flop has smaller DQ latency, lower EDP, and less sensitivity to process variation.

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