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Design of Digital Fir Filter Design on FPGA

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Abstract

The digital finite impulse response (FIR) is widely used in many digital signal processing (DSP) systems, ranging from wireless communication to image and video processing. Digital FIR filter is primarily composed of multipliers, adders and delay elements. Several techniques have been reported in the open literature to implement digital FIR filters using Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). This paper presents various approaches of designing the FIR filter using Xilinx ISE tool.

Key Words: ***FIR filter, DSP systems, FPGA, ASIC, Xilinx.***

INTRODUCTION

Filtering is one of the fundamental steps in many digital signal processing (DSP) applications such as video processing, image processing and wireless communication. Basically there are two types of filters Analog and Digital. Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communications channel, signal detection and analysis in radar application. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. The architectures possess different attributes in the form of speed, complexity, and power dissipation [1]. A filter is frequency selective network, which is used to modify an input signal in order to facilitate further processing. Digital filters have the potential to attain much better signal to noise ratio than analog filters. The basic operation of digital filter is to take a sequence of input numbers and compute a different sequence of output numbers. There exists a range of different digital filters. FIR and IIR are two common filters forms. A drawback of IIR filters is that the closed-form IIR designs are preliminary limited to low pass, band pass, and high pass filters etc. Secondly FIR filters can have precise linear phase. Also, in case of FIR filters, closed-form design equations do not exist and the design problem for FIR filters is much more under control than the IIR design problem.

Adders, multipliers and Delay element are the key block used in the in the implementation of digital FIR filter. Basically, FIR filter performs a linear convolution on a window of N data samples which can be mathematically expressed as follows:

$$y(k)=\sum w(n).x(k-n) \quad \text{for } 0\le n\le N-1$$

The direct form of implementation of an FIR filters can be readily developed from the convolution sum as shown in fig1. Direct form FIR filters are also known as tapped delay line or traversal filters. N-tap filters consist of N delay elements, N multipliers and N-1 adders or accumulators. The impulse response of the FIR filters can be directly inferred from the tap coefficient h.

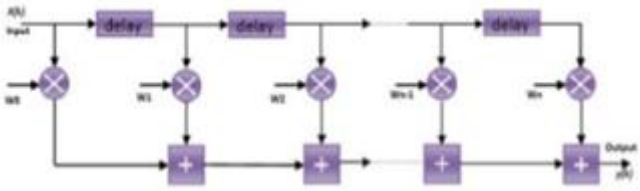

Fig 1: Block diagram of digital FIR filter

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This paper describes the review work on design of digital FIR filters using different designing approaches and its implementation results obtained through Xilinx.

LITERATURE REVIEW

The research paper on the design of FIR filters are published in various journals and presented in many conferences. Here the paper selected describes the design of FIR filters using VHDL or Verilog language. Some of the paper represents the modular design approach of the FIR filters and which is implemented in spartan-3E FPGA/Xilinx Virtex-5 FPGA.The evaluation result shows good area/power efficiency and flexibility by using different architectures for application. .Most papers have used micro programmed FIR filters design approach.

Abdullah A.Aljuffri, Aiman S. Badawai , Mohammad S.Bensaleh, AbdulfattahM.Odeid and SayedManzoorQasim [1] in paper entitled "FPGA implementation of scalable micro programmed FIR filter architectures using Wallace tree and Vedic multipliers". In this paper used Wallace Tree and Vedic multipliers for implementation of 8-tap and 16-tap sequential and parallel micro programmed FIR filters architectures which shows in fig. 2 and fig. 3 respectively.

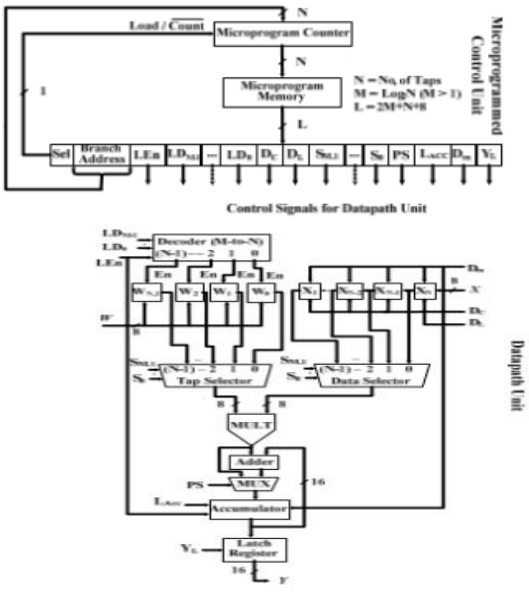

Fig-2: Architecture of sequential micro programmed FIR filter

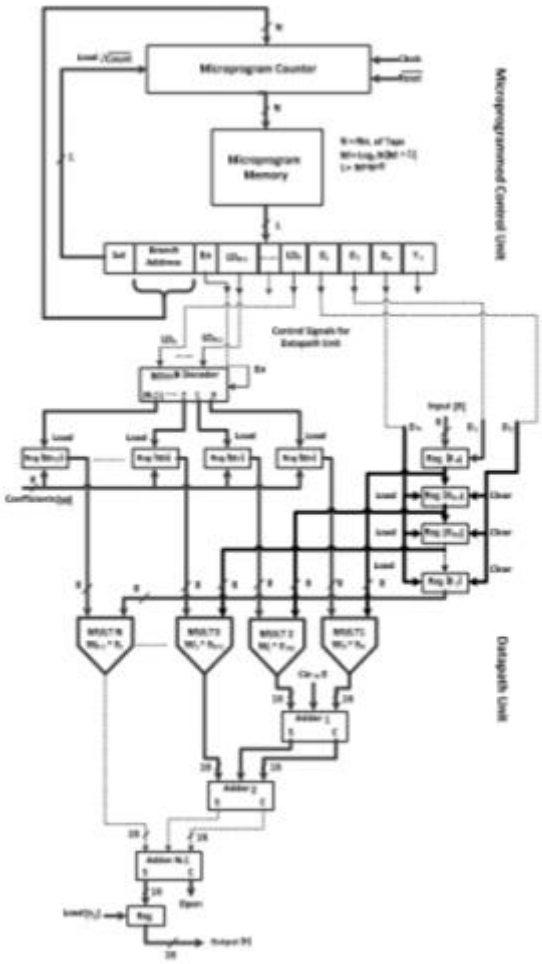

Fig-3: Architecture of parallel micro programmed FIR filter

The designs are realized using Xilinx virtex-5 FPGA. Synplify pro tool used for synthesis, translation, mapping and place and route process and Reports are generated by CAD tool. Performance analyze base on parameter such as minimum period, slice LUTs and maximum operating frequency. The sequential FIR filters architecture designed using Wallace Tree multiplier seems to be more efficient as compared to Vedic multipliers. For 8-tap FIR filter using Wallace Tree have minimum period 11.448 ns and maximum operating frequency 87.4 MHz And for 16-tap FIR filter using WallaceTree have minimum period 10.491 ns and maximum operating frequency 85.3 MHz . A. Aljuffri. M. M. AlNahdi, A.A.Hemaid , O. A. Alshaalan, M. S. BenSaleh, A.M. Obeid and S. M. Qasim [2], in paper entitled, "ASIC realization and performance evaluation

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of scalable micro-programmed FIR filter architectures using Wallace tree and Vedic multiplier". In this paper, Wallace tree and Vedic multiplier are used for efficient realization of 8-tap and 16-tap sequential and parallel scalable micro-programmed FIR filter architectures. The designs of FIR filter are coded in VHDL. Lfoundary 150nm standard-cell based technology is used for the hardware realization of the proposed designs in ASIC. Synopsys Design Compiler is used for the gate-level synthesis. Analyze the performance based on area, Slice LUTs and critical path delays. Wallace tree multiplier using CSA (Carry Skip Adder) has minimum area and delay while Vedic using KSA (Kogge-Stone Adder) has maximum area and delay. For 8-tap FIR filter have period 6.62 ns for 8-tap filter have period 6.62 ns and area 29496 μm^2. For 16-tap FIR filter have period 6.63 ns and area 47463 μm^2 .

Sushma .S and Shobha .S [3] in paper entitled, "Design and implementation of sequential micro programmed FIR filter using efficient multipliers on FPGA". In this paper 8-tap sequential FIR architecture is implemented. Implementation of 8-tap sequential digital FIR filter is presented Using Wallace Tree and Vedic multiplier which is Coded in VHDL. The designs are realized using Xilinx Virtex-5 FPGA. FPGA Resource utilization of Wallace Tree and Vedic multiplier has improved. Analyzed the performance based on the parameter minimum period, slice LUTs and maximum frequency. Implementation result have maximum operating frequency 217.68 MHz, minimum period 4.595 ns and slice LUTs 99 [3].

Pramod Kumar Meher and Abbes Amira [4], in paper entitled, " FPGA realization of FIR filters by efficient and flexible systolization using Distributed Arithmetic". This paper present the realization of 8-tap and 16-tap Digital FIR filters by systolic decomposition of distributed arithmetic (DA). Implemented on Xilinx Virtex-E XCV2000E FPGA using hybrid combination of Handel-C and parameterizable VHDL cores. Analyze the performance on the basis of maximum operating frequency. Implementation is found less areadelay complexity. Implementing 8-tap FIR filter give maximum operating frequency 74.025 MHz and for 16-tap FIR filter 67.222 MHz.

S. C. Prasanna and S. P. Joy Vasantha Rani [5], in paper entitled, "Area and Speed efficient implementation of symmetric FIR Digital filter through reduced parallel LUT Decomposed DA approach .In this paper, implement 16-tap symmetric FIR filter using Reduced parallel LUT decomposed DA (Distributed Arithmetic) approach which is implemented over Xilinx virtex-5 FPGA device-XC5VSX95FT1FF1136. The proposed design reduces the no. of LUTs. This design Support upto the maximum operating frequency of 607MHz and requires lesser clock period than high throughput DA based design. It offers 60.5% less delay than systolic DA based design.

Rakhi Thakur and kavitakhare [6], in paper entitled, "High Speed FPGA implementation of FIR filter for DSP Applications". This paper presented on high speed FPGA implementation of FIR filter. FPGA offers higher sampling rate and lower cost than ASIC. This paper describes an approach to the implementation of digital filter based on FPGA which is coded in VHDL. Analyze the performance base on the parameter such as minimum period is 4.255 ns and maximum frequency 235.026 MHz The result presented requires low area and total memory usage is 147920 kilobytes .

Mahesh Golconda and MarutiZalte [7], in paper entitled, "Comparative analysis of Multiplier and Multiplier-less method used to implement FIR filter on FPGA". In this paper, 8-tap FIR filter is implemented using multiplier and multiplier-less method. In multiplier method, Modified Booth and a Modified Booth with Wallace tree multiplier is designed, While in multiplier-less method, distributed arithmetic and distributed arithmetic with partition is used. Designs are coded in verilog. The code is simulated in Model Sim and synthesized in Xilinx 14.7. Modified Booth with Wallace Tree method has the least delay 8.957 ns among all the other methods. Distributed arithmetic with partition which is a

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multiplier less method had a greater delay than multiplier methods but covers the least area i.e. 165 slice LUTs. As the area is less, power dissipation is also less than others.

FIR FILTER ADD/SHIFT IMPLEMENTATION

In binary arithmetic, multiplication by a power-of-two is simply a shift operation. Implementation of systems with multiplications may be simplified by using only a limited number of power-of-two terms, so that only a small number of shift and add operations are required [4]. An FIR filter tap as shown in Fig.4 can be implemented in two array columns of Xilinx series FPGAs. Because of the high degree of spatial and temporal locality, most signal routing delays are not critical, as they are with typical high performance FPGA designs. Each of the bit slices for the tap requires two combinational logic blocks (CLBs) in the array for implementation. The extensive local routing capability of typical FPGAs can be used for the majority of signals within and between taps. The implementation is based on a Xilinx board . This board has the following features, relevant to the presented implementation [5]:

1) Spartan3 FPGA with 500000 equivalent gates (XC3S5500E), 2) 50MHz crystal oscillator, 3) Asynchronous serial port, with RS232 drivers, 4) Expansion connector with 100 I/O pins, 5) Flash memory for bit stream storage, 6) USB port for FPGA configuration and memory programming. The scheme for the implementation of FIR filter to FPGAs is shown in Fig. 4. The main components of the implemented circuit are as follows [1]:

A. Memory Prepared for storage of past position data of bunches. z-1 in Fig. 1means 1-turn delay

B. Adder: Adder is made to reduce the number of stages and is a key for stable operation of the FPGA used in the board. This reduction of the stage is effective to avoid errors by clock skew in the FPGA and to reduce the power consumption and a circuit area (or number of gates) on FPGA.

C. Multiplier Build-in multipliers are used to fulfill the requirements of high-speed operation; therefore this number of build-in multipliers is one of the constraints to the number of taps of FIR filter.

D. Shift-Register it is used for additional delay for adjust latency to one or two revolution period.

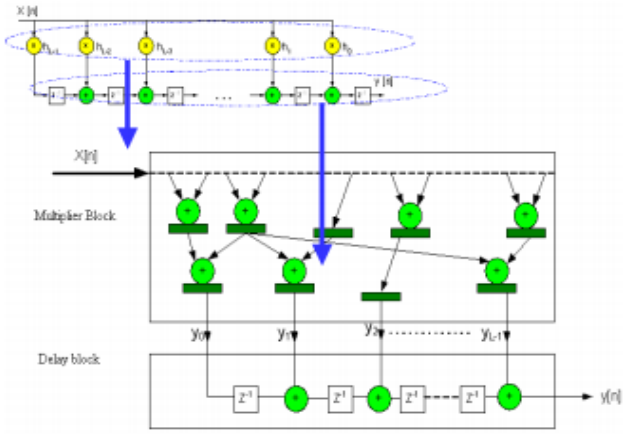

Fig. 4. Implementation of FIR Filter.

FPGA IMPLEMENTATION

Advances in field programmable gate array technology have enabled FPGAs to be applied to a variety of problems. In particular, FPGAs prove particularly useful in data path designs, where the regular structure of the array can be utilized effectively. The programmability of FPGAs adds flexibility not available in custom approaches, while retaining relatively high system clock rates. The disadvantages of FPGAs are primarily related to the limited number of logic operations that can be implemented on a particular device, and the limited signal routing options that are available for connecting logical operators on the array. The hardware description language VHDL is very popular among designers. One reason is good support of integrated circuit design by offering many integrated circuit related function and Data types. There is also large number of libraries available. It supports the behavioral modeling of hardware necessary when implementing a Fir filter generation program. Reducing flip-flop count through minimizing multiplier logic depth has instead been shown to yield the lowest area solutions. The results presented establish a clear low area. Total memory usage is 147920 kilobytes and Minimum period is 4.255ns (Maximum Frequency: 235.026MHz).

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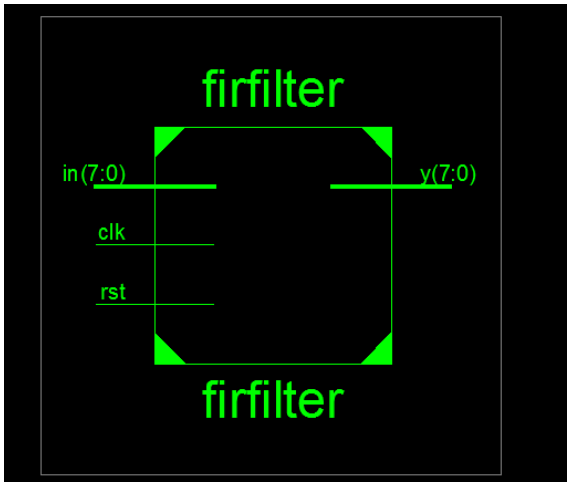

Fig. 5. RTL view of FIR Filter

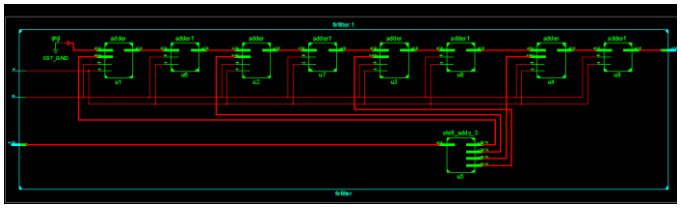
Fig 6: Internal block diagram

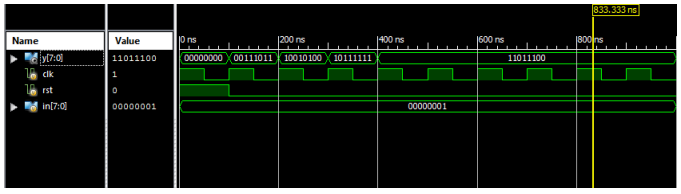

Fig 7: simulation results

TABLE I: FPGA RESOURCE UTILIZATION OF MULTIPLIER BLOCK

Resource	*Used*	*Available*	*Utilization*
Slice	144	9312	1%
LUTs	92	9312	1%
Occupied Slices	84	4656	1%
Related Logic	84	84	100%
I OBs	46	92	50%
BUFGMUXs	1	24	4%

CONCLUSION

There is a constant requirement for efficient use of FPGA resources where occupying less hardware for a given system. In this paper we presented a multiplier less technique, based on the add and shift method. It can perform at sample rates greatly exceeding those of a state-of-the-art programmable DSP. The FPGA solution offers completeflexibility in the design. By reducing chip count, it improves the overall reliability of the system, provides low area, low power and high-speed implementation of FIR filters. It also reduces filter latency.

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