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Design of High Speed UART Using Verilog HDL

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Abstract :

A UART is usually anindividual (or part of an) used for over a computer or peripheral device. UARTs are now commonly icluded included in microcontrollers.

A UART (Universal Asynchronous Receiver/Transmitter) is the microchip with programming that controls a computer's interface to its attached serial devices. Specifically, it provides the computer with the RS-232C Data Terminal Equipment (DTE) interface so that it can "talk" to and exchange data with modems and other serial devices.

Serial transmission is commonly used with modems and for non-networked communication between computers, terminals and other devices.The Universal Asynchronous Receiver/Transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion.

At the destination, a second UART re-assembles the bits into complete bytes. Each UART contains which is the fundamental method of conversion between serial and parallel forms. Serial transmission of digital information (bits) through a single wire or other medium is much more cost effective than parallel transmission through multiple wires.

1. Introduction:

Asynchronous serial communication has advantages of less transmission line, high reliability, and long transmission distance, therefore is widely used in data exchange between computer and peripherals. Asynchronous serial communication is usually implemented by Universal Asynchronous Receiver Transmitter (UART) [1].

UART allows full-duplex communication in serial link, thus has been widely used in the data communications and control system. In actual applications, usually only a few key features of UART are needed. Specific interface chip will cause waste of resources and increased cost.

Particularly in the field of electronic design,SOC technology is recently becoming increasingly mature. This situation results in the requirement of realizing the whole system function in a single or a very few chips. Designers must integrate the similar function module into FPGA.

uses VERILOGHDL to implement the UART core functions and integrate them into a FPGA chip to achieve compact, stable and reliable data transmission, which effectively solves the above problem [2] [3].One of the most important applications of UART is Multi-channel UART Controller designed by Shouqian Yu, Lili Yi, Weihai Chen and Zhaojin Wen.[2].

The proposed method paper presents a multi-channel UART controller based on FIFO technique and FPGA. This controller is designed with FIFO circuit block and UART circuit block to implementcommunication in modern complex control systems quickly and effectively.

In this, the flow charts of data processing as well as the implementation state machine are also presented in detail. This controller can be used to implement communication when master equipment and slaver equipment are set at different Baud Rate. It also can be used to reduce synchronization error between sub-systems in a system with several sub-systems. The controller is reconfigurable and scalable.

Basic building block:

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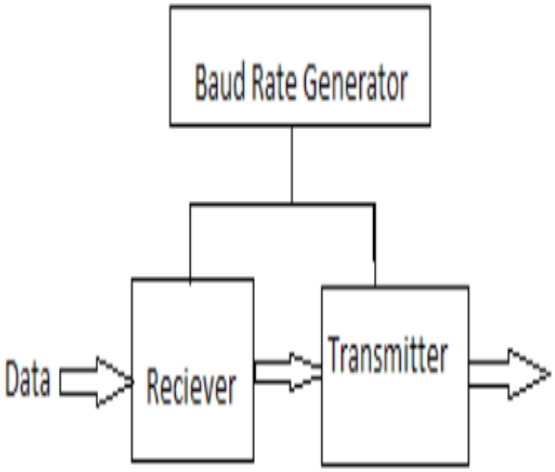
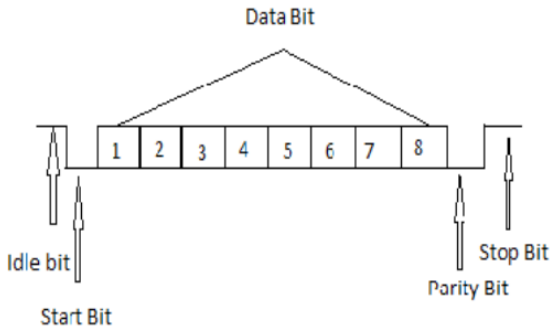


Figure1



2.UART DATA FORMAT:

From review of related work and published literature, it is observed that many researchers have designed UART by applying different techniques like algorithms, logical relations. Researchers have undertaken different phenomena with regards to design UART and attempted to find better result.

Today in real world the actual applications, usually needed only a few key features of UART. Specific interface chip will cause waste of resources and increased cost. Particularly in the field of electronic design, SOC technology is recently becoming increasingly mature.

This situation results in the requirement of realizing the whole system function in a single or a very few chips. From the careful studyof reported work it is observed that very few researchers have taken a work for integrating the required feature of UART. Variable-sized adder.

2.EXPERIMENTAL DETAILS:

The three main components of the UART such as transmitter, receiver and the baud rate generator are described below:

A.Transmitter Module:

The function of the transmitter module is to convert the 8 bit serial data into the single bit data. In this module, when our load signal is high the data_in is stored into the holding register. The data in the holding register is shifted to the intermediate register with the start bit of zero and thisintermediate register is of 8 bits. Once the shift signal is high the least significant bit of the intermediate register i.e.

the start bit comes at the output of the transmitter and served as the input to the receiver. When the entire data has been sent, the transmitter provides a parity bit which is served as the input to the receiver. To check the CRC error, we have to provide the divisor as the user input and once the entire data has been sent, the transmitter generates the remainder which is given as the input to the receiver.

B.BaudRateGenerator:

The Baud rate generator is nothing but the frequency divider. In this UART we will apply the synchronized clock signal to both transmitter and the receiver. The clock signal applied to the receiver is 16 times to that of the transmitter.

C.ReceiverModule:

The function of the receiver module is that it will store the tx out i.e. the output of the transmitter which is of single bit into the intermediate register with the start bit as the least significant bit and collectively provides the serial data of 8bit. When the load signal is high it will get the start bit from the transmitter which assures that the original data is now being send by the transmitter.Once the shift signal is becomes high with no load signal, the data coming from the transmitter gets shifted into the intermediate register of the receiver and provides the 8 bit serial data which we have given as an input to the transmitter.

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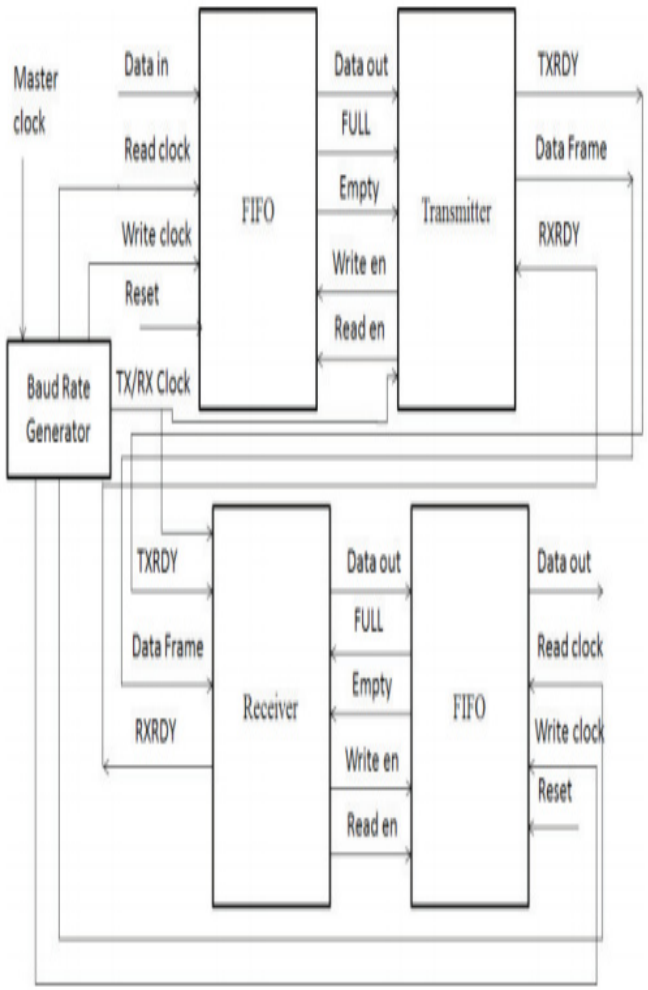
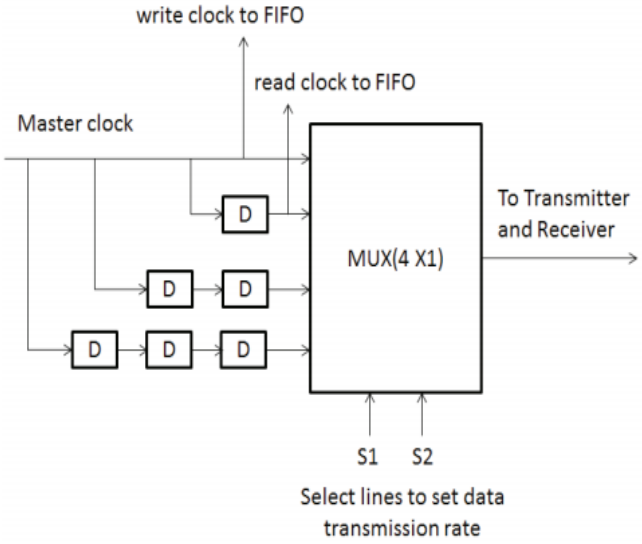
Once the entire data has been sent the parity error and the CRC errors has been checked out and are served as the input to the transmitter. If parity error and CRC errors occur or are at logic 1, it means that our transmission is having some errors.

III.PROPOSED ARCHITECTURE:

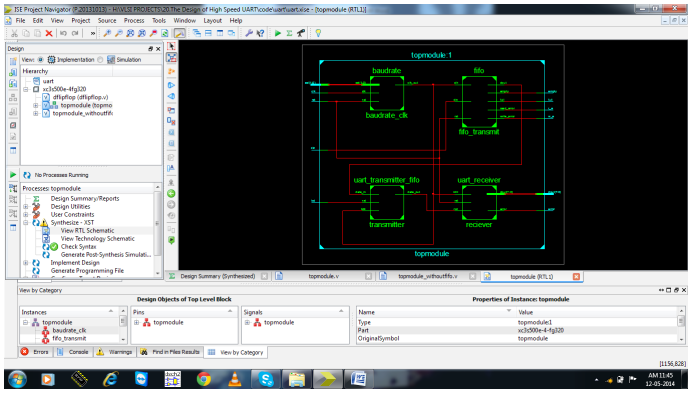
The proposed architecture of UART is shown in fig.3. Baudrate generator provides read clock and write clock to both FIFO and a common clock signal to both transmitter and receiver. FIFO depth is calculated as: FIFO size (depth) = Data frame size – (read frequency/write frequency) * Data frame size.



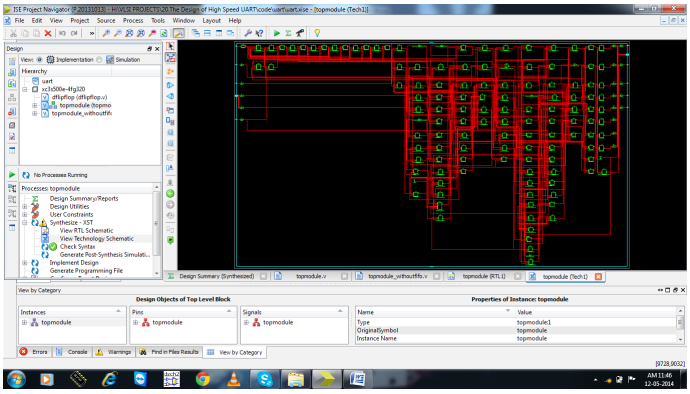
3. PROPOSE ARCHITECTURE:



WAVE FORMS:



RTL SCHAMATIC:



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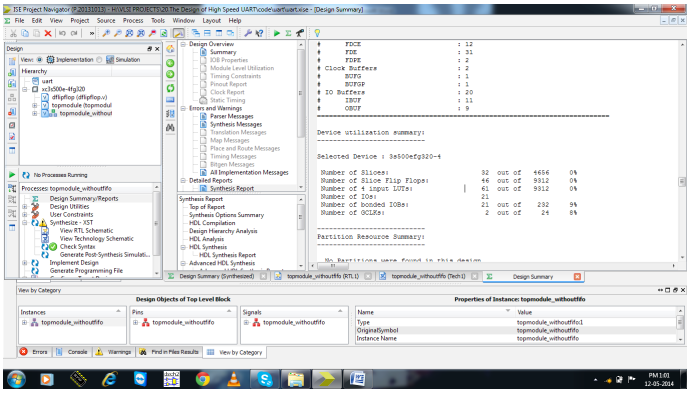
TECHNOLOGY SCHAMATIC:



SYNTHESIS REPORT:

IV.CONCLUSIONS:

This uses Verilog description language to get the modules of UART. After studying the comparative analysis we conclude that there is a difference in between the number of slices, LUTs, GCLKs and the maximum frequency. The results are quiet stable and reliable and has great flexibility with high integration. If we use FIFO in making the UART our design becomesmore flexible, stable and reliable which provides the high bps rate.

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