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Low Power Analysis of Double Tail Comparator for ADC by Using Hspice

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Abstract:

The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived.

From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages.

Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-μm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 μW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

Index Terms:

Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.

I.INTRODUCTION:

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1].

Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges.

Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that body-driven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantiser for sub-1V ΣΔ modulators is proposed.

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Despite the advantages, the body-driven transistor suffers from smaller trans conductance (equal to gmb of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In [7]–[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of [7] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 µW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range [10].

In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each structure is discussed.

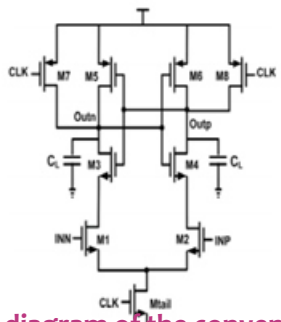

Fig. 1. Schematic diagram of the conventional dynamic comparator.

Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section III. Section IV discusses the design issues. Simulation results are addressed in Section V, followed by conclusions in Section VI.

II. Clocked Regenerative Comparators:

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common struc-tures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator:

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Out n and Out p to VDD to define a start condition and to have a valid logical level during reset.

In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Out p, Out n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input volt-age (INN/INP). Assuming the case where VINP > VINN, Out p discharges faster than Outn, hence when Out p (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Out p discharges to ground. If VINP < VINN, the circuits works vice versa.

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The delay of this comparator is comprised of two time delays, to and tlatch. The delay to represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on.In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Out p node compared to the Outn node, which is driven by M1 with smaller current. Consequently, the discharge delay (to) is given by

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \cong 2\frac{C_L |V_{thp}|}{I_{tail}}. \quad (1)$$

In (1), since I2 =Itail/2+ΔIin =Itail/2+gm1,2ΔVin , small differential input (ΔVin), I2 can be approximated to be constant and equal to the half of the tail current.

The second term, tlatch, is the latching delay of two cross-coupled inverters. It is assumed that a voltage swing of ΔVout = VDD/2 has to be obtained from an initial output voltage difference ΔVo at the falling output (e.g., Out p). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [17]. Hence, the latch delay time is given by, [18].

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (2)$$

where gm,eff is the effective trans conductance of the back-to-back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the begin-ning of the regeneration (i.e., at t = to). Based on (1), ΔVo can be calculated from (3).

$$\Delta V_0 = \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right| = |V_{thp}| - \frac{I_2 t_0}{C_L} = |V_{thp}|\left(1 - \frac{I_2}{I_1}\right). \quad (3)$$

The current difference, Δ Iin = | I1 – I2|, between the branches is much smaller than I1 and I2. Thus, I1 can be approximated by Itail/2 and (3) can be rewritten as

$$\begin{aligned}\Delta V_0 &= |V_{thp}| \frac{\Delta I_{in}}{I_1} \\ &\approx 2|V_{thp}| \frac{\Delta I_{in}}{I_{tail}} \\ &= 2|V_{thp}| \frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}} \Delta V_{in} \\ &= 2|V_{thp}| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in}. \end{aligned} \quad (4)$$

In this equation, β1,2 is the input transistors' current factor and Itail is a function of input common-mode voltage (Vcm) and VDD. Now, substituting ΔVo in latch delay expression and considering to, the expression for the delay of the conventional dynamic comparator is obtained as tdelay = to +tlatch.

$$= 2\frac{C_L |V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}| \Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right). \quad (5)$$

Equation (5) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input dif-ference voltage (ΔVin). Besides, the delay depends indirectly to the input common-mode voltage (Vcm). By reducing Vcm, the delay to of the first sensing phase increases because lower Vcm causes smaller bias current (Itail).

On the other hand, (4) shows that a delayed discharge with smaller Itail results in an increased initial voltage difference (ΔVo), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing of to and reducing of tlatch will finally lead to an increase in the total delay. In [17], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consump-tion, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset.

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The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate-source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower trans conductances.

Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

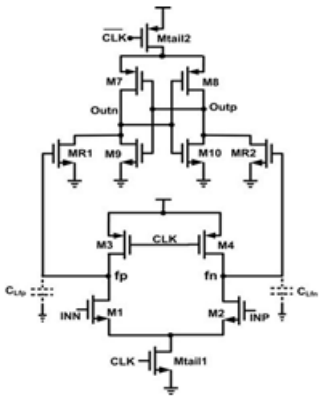

Fig. 3. Schematic diagram of the conventional double-tail dynamic com-parator.

B. Conventional Double-Tail Dynamic Comparator:

A conventional double-tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10].

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and volt-ages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn (p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes _Vfn(p) to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, to and tlatch. The delay to represents the capacitive charging of the load capacitance C Lout(at the latch stage output nodes, Out n and Out p) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus to is obtained. From eq-6.

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn} C_{Lout}}{I_{tail2}}$$

Where IB1is the drain current of the M9 (assuming VINP >VINN, see Fig. 3) and is approximately equal to the half of the tail current (Itail2).

After the first n-channel transistor of the latch turns on (for instance, M9), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD). The regeneration time (tlatch) is achieved according to (2). For the initial output voltage difference at time to, ΔVo we have

$$\Delta V_0 = \left|V_{outp}(t=t_0) - V_{outn}(t=t_0)\right| = V_{Thn} - \frac{I_{B2} t_0}{C_{Lout}}$$

$$= V_{Thn}\left(1 - \frac{I_{B2}}{I_{B1}}\right) \qquad (7)$$

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Where IB1andIB2are the currents of the latch left- and rightside branches of the second stage, respectively. Considering ΔIlatch =|IB1−IB2|=gmR1,2ΔVfn/fp, (7) can be rewritten as

$$\Delta V_0 = V_{\text{Thn}} \frac{\Delta I_{\text{latch}}}{I_{\text{B1}}} \approx 2V_{\text{Thn}} \frac{\Delta I_{\text{latch}}}{I_{\text{tail2}}} = 2V_{\text{Thn}} \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \Delta V_{\text{fn/fp}} \tag{8}$$

where gmR1,2 is the transconductance of the intermediate stage transistors (MR1 and MR2) and ΔVfn/fp is the voltage difference at the first stage outputs (fn and fp) at time to. T

hus, it can be concluded that two main parameters which influence the initial output differential voltage (ΔVo) and thereby the latch regeneration time are the transcon-ductance of the intermediate stage transistors (gmR1,2) and the voltage difference at the first stage outputs (fn and fp) at time to. In fact, intermediate stage transistors amplify the voltage difference of ΔVfn/fp causing the latch to be imbalanced.
The differential voltage at nodes fn/fp (ΔVfn/fp) at time to can be achieved from

$$\begin{aligned} \Delta V_{\text{fn/fp}} &= \left| V_{\text{fn}}(t = t_0) - V_{\text{fp}}(t = t_0) \right| \\ &= t_0 \cdot \frac{I_{\text{N1}} - I_{\text{N2}}}{C_{L,\text{fn(p)}}} \\ &= t_0 \cdot \frac{g_{\text{m1,2}} \Delta V_{\text{in}}}{C_{L,\text{fn(p)}}}. \end{aligned} \tag{9}$$

In this equation, IN1 and IN2 refer to the discharging currents of input transistors (M1andM2), which are dependent on the input differential voltage (i.e., ΔIN =gm1,2ΔVin). Substituting (9) in (8), ΔVo will be

$$\begin{aligned} \Delta V_0 &= 2V_{\text{Thn}} \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \Delta V_{\text{fn/fp}} \\ &= \left(\frac{2V_{\text{Thn}}}{I_{\text{tail2}}} \right)^2 \cdot \frac{C_{\text{Lout}}}{C_{L,\text{fn(p)}}} \cdot g_{\text{mR1,2}} g_{\text{m1,2}} \Delta V_{\text{in}}. \end{aligned} \tag{10}$$

This equation shows thatΔVo depends strongly on the transconductance of input and intermediate stage transistors,input voltage difference (ΔVin), latch tail current, and the capacitive ratio ofCLoutto CL,fn(p). Substituting ΔVoin latch regeneration time (2), the total delay of this comparator is achieved as follows

$$\begin{aligned} t_{\text{delay}} &= t_0 + t_{\text{latch}} = 2\frac{V_{\text{Thn}} C_{\text{Lout}}}{I_{\text{tail2}}} + \frac{C_{\text{Lout}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0} \right) \\ &= 2\frac{V_{\text{Thn}} C_{\text{Lout}}}{I_{\text{tail2}}} + \frac{C_{\text{Lout}}}{g_{m,\text{eff}}} \\ &\quad \cdot \ln\left(\frac{V_{\text{DD}} \cdot I_{\text{tail2}}^2 \cdot C_{L,\text{fn(p)}}}{8V_{\text{Thn}}^2 \cdot C_{\text{Lout}} g_{\text{mR1,2}} g_{\text{m1,2}} \Delta V_{\text{in}}} \right). \end{aligned} \tag{11}$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.1) The voltage difference at the first stage outputs (ΔVfn/fp) at timetohas a profound effect on latch initial differential output voltage (ΔVo) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground toVDD, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. Proposed Double-Tail Dynamic Comparator:

Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner [see Fig. 5(a)].

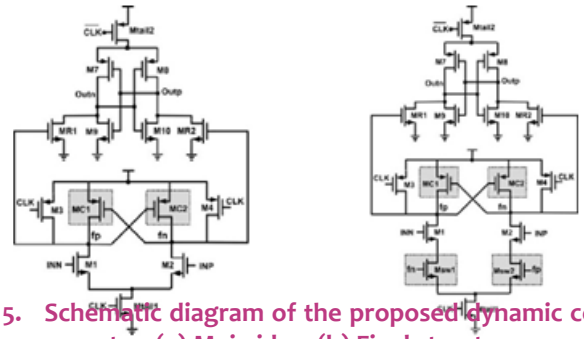

Fig. 5. Schematic diagram of the proposed dynamic comparator. (a) Main idea. (b) Final structure

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A. Operation of the Proposed Comparator:

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD).

Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference (9),

in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/ fp) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B).

Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M 1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig. 5(b)].

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been precharged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates.

As soon as the comparator detects that one of the fn/ fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn fromVDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. This will be more discussed in the following section.

B. Delay Analysis:

In order to theoretically demonstrate how the delay is reduced, delay equations are derived for this structure as previously done for the conventional dynamic comparator and the conventional double-tail dynamic comparator. The analysis is similar to the conventional double-tail dynamic comparator ,however;the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (ΔV0) at the beginning of the regeneration (t =t0); and second, it enhances the effective transconductace (gmeff)of the latch. Each of these factors will be discussed in detail.

1) Effect of EnhancingΔV0: As discussed before, we define:t0, as a time after which latch regeneration starts. In other words,tois considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence.According to (2), the latch output voltage difference at time to,(ΔV0) has a considerable impact on the latch regeneration time, such that biggerΔV0 results in less regeneration time.Similar to the equation derived for theΔV0of the double-tail structure, in this comparator we have

$$\Delta V_0 = V_{\mathrm{Thn}} \frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{B1}}} \approx 2V_{\mathrm{Thn}} \frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{tail2}}} = 2V_{\mathrm{Thn}} \frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}} \Delta V_{\mathrm{fn/fp}}. \quad (12)$$

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In order to find ΔVfn/fp at t =t0, we shall notice that the combination of the control transistors (Mc1 andMc2) with two serial switches (Msw1, Msw2) emulates the operation of a back to-back inverter pair; thus using small-signal model presented in [18], ΔVfn/fp is calculated by

$$\Delta V_{fn/fp} = \Delta V_{fn(p)0} \exp((A_v - 1)t/\tau). \quad (13)$$

In this equation,τ/Av−1=(CL,fn(p)/Gm,eff1)andΔVfn(p)o is the initial fn/fp node difference voltage at the time when the corresponding pMOS control transistor is started to be turned on. Hence,it can be shown that ΔVfn(p)o is obtained from

$$\Delta V_{fn(p)0} = 2|V_{Thp}| \frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}. \quad (14)$$

Substituting (13) in (12), ΔV_0 will be

$$\Delta V_0 = 2V_{Thn}\frac{g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp} = 4V_{Thn}|V_{Thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right). \quad (15)$$

Comparing (15) with (10), it is evident that ΔV0 has been increased remarkably (in an exponential manner) in compare with the conventional dynamic comparator.

2) Effect of Enhancing Latch Effective Transconductance: As mentioned before, in conventional double-tail comparator,both fn and fp nodes will be finally discharged completely.

In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the VDDat the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words,positive feedback is strengthened. Hence,tlatch will be

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\cdot\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\cdot\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right). \quad (16)$$

Finally, by including both effects, the total delay of the proposed comparator is achieved from

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\cdot\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}} \times \ln\left(\frac{V_{DD}/2}{4V_{Thn}|V_{Thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right)}\right). \quad (17)$$

By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes advantage of an inner positive feedback in double-tail operation, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of VTh/VDD, the trans conductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator.

3) Reducing the Energy per Comparison:

It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies.

IV. DESIGN CONSIDERATIONS:

In designing the proposed comparator, some design issues must be considered. When deter

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$$t_{on,Mc1(2)} < t_0 \rightarrow \frac{|V_{Thp}| \cdot C_{L,fn(p)}}{I_{n1,2}} < \frac{V_{Thn} C_{Lout}}{I_{B1}}$$
$$\rightarrow \frac{|V_{Thp}| \cdot C_{L,fn(p)}}{\frac{I_{Tail1}}{2}} < \frac{V_{Thn} \cdot C_{Lout}}{\frac{I_{Tail2}}{2}}. \quad (18)$$

This condition can be easily achieved by properly designing the first and second stage tail currents. Even if possible in the fabrication technology, low-threshold pMOS devices can be used as control transistors leading to faster turn on.In designing the nMOS switches, located below the input transistors, the drain-source voltage of these switches must be considered since it might limit the voltage headroom,restricting the advantage of being used in low-voltage applications. In order to diminish this effect, low-on-resistance nMOS switches are required.

In other words, large transistors must be used. Since the parasitic capacitances of these switches do not affect the parasitic capacitances of the fn/fp nodes (delay bottlenecks), it is possible to optimally select the size of the nMOS switch transistors in a way that both low-voltage and low-power operations are maintained. The effect of mismatch between controlling transistors on the total input-referred offset of the comparator is another important issue. When determining the size of controlling transistors (MC1–MC2), two important issues should be considered.

First, the effect of threshold voltage mismatch and current factor mismatch of the controlling transistors on the comparator input-referred offset voltage. Second, the effect of transistor sizing on parasitic capacitances of the fn/fp nodes, i.e., CL,fn(p), and consequently the delay of the comparator. While larger transistors are required for better matching; however, the increased parasitic capacitances are delay bottlenecks. In order to study the effect of threshold and current factor mismatch of control transistors on the total input-referred offset voltage, a brief mismatch analysis is presented here.

A. Mismatch Analysis:

In principle, the effect of threshold voltage mismatch and current factor mismatch of controlling transistors is almost negligible in most cases except for the situation where input differential voltage (ΔVin) is very small where fn and fp have approximately similar discharging rates. This is true because by the time that the controlling transistor (Mc1 orMC2) turns on, the differential input signal is already amplified to large amplitude compared to the mismatches. In other words, offset due to the controlling transistor mismatches is divided by the gain from the input to the output.

However, in case of small ΔVin, when fn and fp follow each other tightly, the mismatch of the controlling transistors might influence the result of the comparison. Hence, the following brief analyzes the effect of threshold and current factor mismatches of controlling transistors on the total input-referred offset voltage.

1) Effect of Threshold Voltage Mismatch of MC1, MC2, i.e., ΔVThC1, 2:

The differential current due to the threshold voltage mismatch can be obtained from

idiff = gmc1,2ΔVThc1,2 (19)

where gmc1,2 is the transconductance of the controlling transistors. So, the input-referred offset voltage due to the Mc1,2 threshold voltage mismatch is obtained as follows:

$$\Delta V_{eq,due\,\Delta V_{Thc1,2}} = \frac{g_{mc1,2}\Delta V_{Thc1,2}}{g_{m1,2}} = \frac{\mu_p W_{C1,2} V_{ODC1,2}}{\mu_n W_{1,2} V_{OD1,2}} \Delta V_{Thc1,2} \quad (20)$$

Where VOD refers to the overdrive voltage of the transistors.

2) Effect of Current-Factor Mismatch MC1, MC2, i.e., ΔβC1, 2:

In order to calculate the input-referred offset due to the current factor mismatch of MC1,2, ΔβC1,2 is modeled as a channel width mismatch ΔW, i.e., Δβ/β=ΔW/W. The differential current that ΔW generates can be obtained as expressed in (21).

$$i_{diff} = \frac{1}{2}\mu_p C_{ox} \frac{\Delta W}{L} (V_{gsc1,2} - V_{thc1,2})^2. \quad (21)$$

Note that the controlling transistors are in saturation since |VGDc1,2|=|Vfn –Vfp| <|Vthp|. So the input-referred offset voltage due to the current factor mismatch is calculated from

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$$\Delta V_{eq,due\Delta\beta_{C1,2}} = \frac{i_{diff}}{g_{m1,2}} = \frac{0.5\mu_p W_{C1,2}(V_{gsc1,2} - V_{thp})^2}{\mu_n W_{1,2}(V_{gs1,2} - V_{thn})} = \frac{0.5\mu_p W_{C1,2} V_{OD_{C1,2}}^2}{\mu_n W_{1,2}(V_{cm} - R_{CLK} K_{nC1,2} V_{OD_{C1,2}}^2 - V_{thn})} \quad (22)$$

Where Vcm is the input common mode voltage and Rclk is the equivalent on resistance of the tail transistor.Assuming both mismatch factors, the total input referred offset due to the mismatch of the controlling transistors can be found from

$$\sigma_{total} = \sqrt{\sigma^2_{\Delta V_{ThC1,2}} + \sigma^2_{\Delta\beta_{C1,2}}}. \quad (23)$$

From (20) and (22), it can be concluded that the ratio of the controlling transistor sizes to the input transistor size, i.e.,(WC1,2/W1,2), is effective in reducing the offset. Due to the fact that the transconductance of the input transistors (gm1,2) is important in amplifying the input differential voltage and due to the dominant role of the size of these transistors on total input-referred offset, usually large input transistors are designed, which results in diminishing the effect of controlling transistors mismatch.

V. SIMULATION RESULTS:

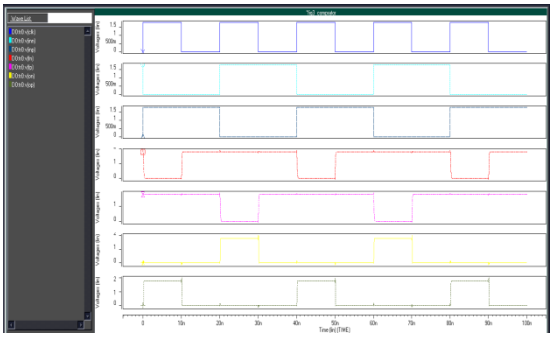

Fig1

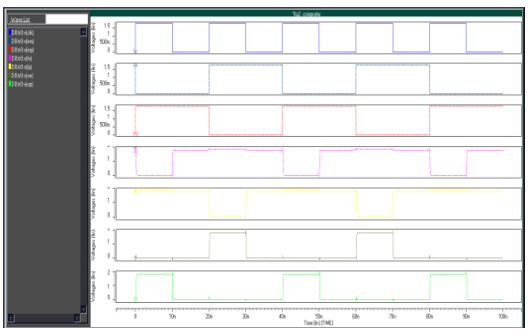

Fig2

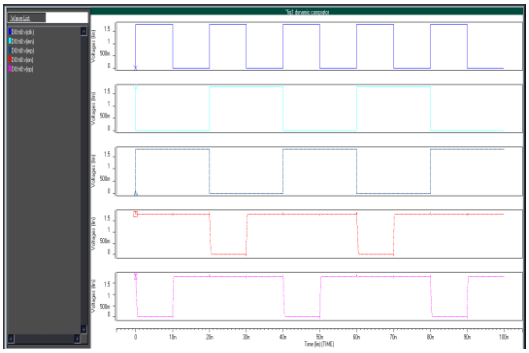

Fig3

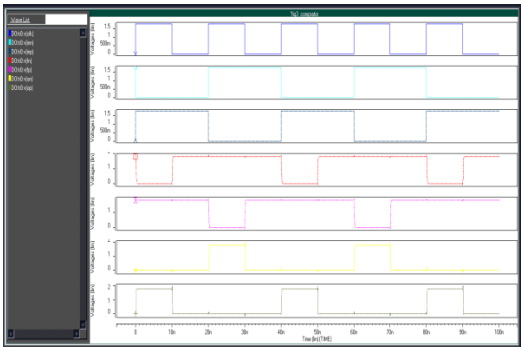

Fig4

The above waveforms show the simulated delay of the comparator versus differential input voltage under different conditions of input common-mode voltage (Vcm) at VDD. For a given value of Vcm, the delay decreases as differential input voltage increases. Furthermore, the delay is also dependent on the variation of common-mode voltage

Performance Comparison:

Sl. No	Comparator structure	Conventional dynamic Comparator	Double-tail dynamic comparator	Proposed dynamic comparator	
				Main Idea	Final structure
1	Technology CMOS	180 nm	180 nm	180 nm	180 nm
2	Supply Voltages (V)	0.8 V	0.8 V	0.8 V	0.8 V
3	Frequency	50 MHz	50 MHz	33.3 MHz	25 MHz
4	Average Power	560.4 n W	510.2 n W	251.2 n W	242.3 n W
5	Delay	211.22 p sec	191.2 p sec	151.3 p sec	146.2 p sec
6	Power delay product	$118.36*10^{-18}$ J	$97.55*10^{-18}$ J	$38.05*10^{-18}$ J	$35.42*10^{-18}$ J
7	Energy	$25*10^{-27}$ J	$18.65*10^{-27}$ J	$5.75*10^{-27}$ J	$5.17*10^{-27}$ J
8	Offset Voltages	0.393 V	0.394 V	0.392 V	0.395 V
9	Leakage Power	1.206 µW	1.24 µW	1.59 µW	2.08 µW

VI. CONCLUSION:

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived.

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Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-µmCMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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