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Symmetrical and asymmetrical faults controlling in distribution system by using series connected device

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Abstract:

This paper describes the problem of voltage sags and swells introduces and evaluates an auxiliary con-trol strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR).
The proposed controller supplements the voltage-sag compensa-tion control of the DVR. It does not require phase- locked loop and independently controls the magnitude and phase angle of the in-jected voltage for each phase.

It first analyzes the power circuit of a DVR system in order to come up with appropriate control limitations and control targets for the compensation voltage control. The proposed control scheme is simple to design. Simulation results carried out by Matlab/Simulink verify the performance of the proposed method.
Here effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters, and this en-ables effective fault current interrupting even under arcing fault conditions.

The proposed control scheme:

1) can limit the fault current to less than the nom-inal load current and restore the point of common coupling voltage within 10 ms; 2) can interrupt the fault current in less than two cy-cles; 3) limits the dc-link voltage rise and, thus, has no restrictions on the duration of fault current interruption; 4) performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions.

INTRODUCTION:

The DYNAMIC voltage restorer (DVR) is a custom power device utilized to counteract voltage sags [1], [2]. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to a voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle.
Fig. 1 shows the main components of a DVR (i.e., a series transformer , a voltage- source converter (VSC), a harmonic filter, a dc-side capacitor, and an energy storage de-vice [7], [8]).

The line -side harmonic filter [5] consists of the leakage inductance of the series transformer and the filter capacitor. The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current [9]–[11].
A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it also to limit or interrupt the downstream fault currents.

A control approach to enable a DVR to serve as a fault current lim-iter is provided in [9]. The main drawback of this approach is that the dc- link voltage of the DVR increases due to real power absorption during fault current-limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault.

The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the methods introduced in [7] and [12].

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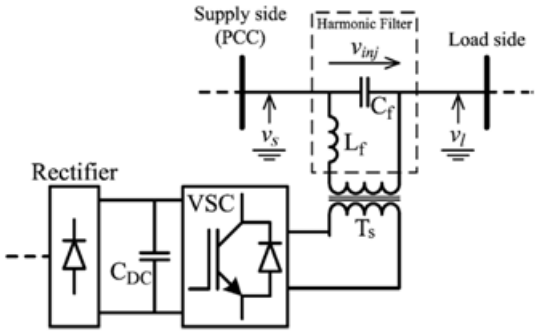

Fig. 1. Schematic diagram of a DVR with a line-side harmonic filter.

To overcome the aforementioned limitations, this paper proposes an augmented control strategy for the DVR that provides: 1) voltage -sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. The former function has been presented in [13] and the latter is de-scribed in this paper.It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the overcurrent relays).

This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the up-stream relay or the circuit breaker (CB).It should be noted that the FCI function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself.

The performance of the proposed control scheme is evaluated through various simulation studies in the SIMULINK platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions.

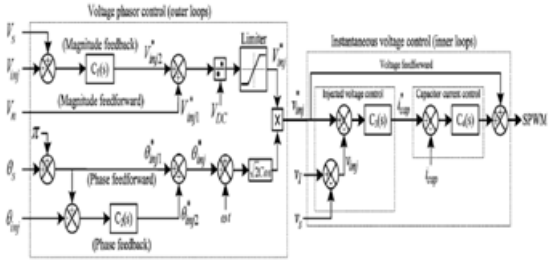

Fig. 2. Per-phase block diagram of the DVR control system in FCI mode.

PROPOSED FCI CONTROL STRATEGY:

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc -link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controllers one for each single-phase VSC of the DVR.

Assume the fundamental frequency components of the supply voltage v_s, load voltage v_l, and the injected Voltage v_{inj}, Fig. 1 are

$$v_s = V_s \times \cos(\omega t + \theta_s), \quad (1)$$

$$v_l = V_l \times \cos(\omega t + \theta_l), \quad (2)$$

$$v_{\text{inj}} = v_l - v_s = V_{\text{inj}} \times \cos(\omega t + \theta_{\text{inj}}). \quad (3)$$

The FCI function requires a phasor parameter estimator (dig-ital filter) which attenuates the harmonic contents of the mea-sured signal. To attenuate all harmonics, the filter must have a full -cycle data window length which leads to one cycle delay in the DVR response. Thus, a compromise between the voltage in-jection speed and disturbance attenuation is made. The designed LES filters utilize a data window length of 50 samples at the sampling rate of 10 kHz and, hence, estimate the voltage phasor parameters in 5 ms.

Fig. 3 depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference [13] demonstrates the effectiveness of this fi lter in attenuating the noise, harmonics, and distortions for the sag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highly distorted.

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Fig. 2 shows a per-phase block diagram of the proposed DVR control system corresponding to the FCI operation mode, where is the nominal rms phase voltage. The control system of Fig. 2 utilizes, the dc-link voltage, and the harmonic filter capacitor current as the input signals. The reported studies in this paper are based on the over current fault detection method of [7] and [12]. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the rated load current.

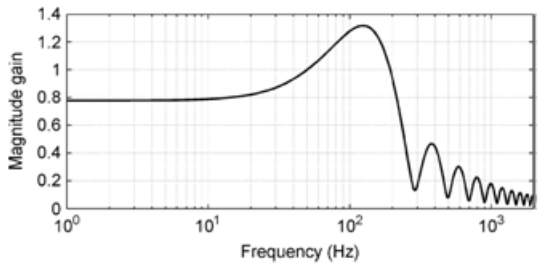

Fig.3. Magnitude of the LES filters frequency response.

The proposed multiloop control system [3], [8], [9], [15]–[20] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter [18] and [21], and improves the dynamic re-sponse and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are described in the following two subsections.

A.Voltage Phasor Control System:

In the FCI operation mode, the required injected voltage Phasor is equal to the source voltage phasor, but in phase opposition [i.e., the injected phasor is controlled to be]. Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback control system [17], [18], [21]–[27].

Fig. 2 shows two proportional-integral (PI) controllers (and) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller are determined to achieve a fast response with zero steady-state error.

B. Instantaneous Voltage-Control System:

Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor based controller is directly fed to the sinusoidal pulse-width modulation (SPWM) unit. However, resonances of the harmonic filter cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances.

The generated reference signal for the injected voltage error is fed to the voltage controller. As shown in Fig. 2, the output of the voltage controller is the reference signal for the filter capacitor current control loop. It is compared with the measured capacitor current, and the error is fed to the current controller.

The steady-state error of the proposed control system is fully eliminated by the PI controllers in the outer control loop (i.e.,and), which track dc signals (magnitude and phase angle). Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. Thus, in Fig. 2, and are pure gains and , respectively.

A large results in amplification of the DVR filter resonance and can adversely impact the system stability [18]. Thus, the transient response of the DVR is enhanced by a feed forward loop, and a small proportional gain is utilized as the voltage controller. A large damps the harmonic filter resonance more effectively, but it is limited by practical considerations (e.g., amplification of capacitor current noise, measurement noise, and dc offset [18]).

Therefore, the lowest value of the proportional gain which can effectively damp the resonances is utilized. The output of the current controller is added to the feed forward voltage to derive the signal for the PWM generator.

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III. STUDY RESULTS:

Fig. 4 depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the SIMULINK software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given in Appendix A. In the reported studies, the base voltage for per-unit values is the nominal phase voltage. Besides, voltage and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively.

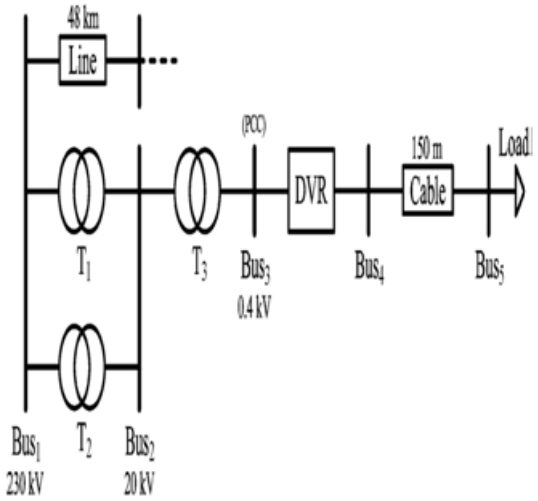

Fig. 4. Single-line diagram of the system used for simulation studies.

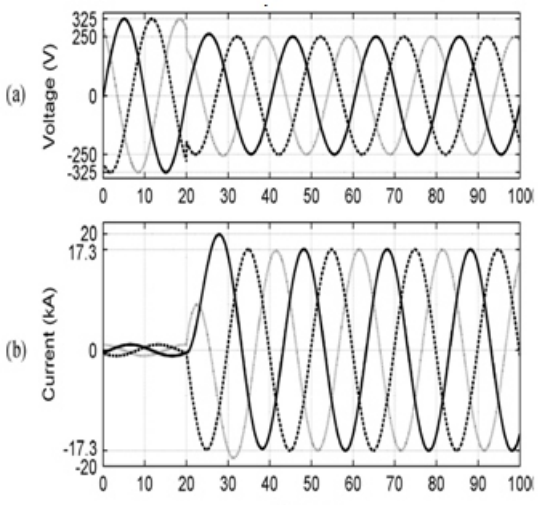

Fig. 5. (a) Voltages at BUS3. (b) Fault currents, during downstream three-phase fault when the DVR is inactive (bypassed).

A.Three-Phase Downstream Fault:

The system is subjected to a three- phase short circuit with a negligible fault resistance at 20 ms at . Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current (Fig. 5) .

Fig. 6 shows FCI performance of the proposed DVR control system during the fault. Fig. 6(a)–(c), respectively, shows the three-phase injected voltages, the restored three-phase supply-side voltages, and the three-phase load -side voltages which are reduced to zero to in-terrupt the fault currents. The slightly injected voltage by the DVR before the fault initiation [Fig. 6(a)] is the voltage drop across the series impedance of the DVR series transformer sec-ondary winding.

Fig. 6(d) shows the line currents (i.e., the currents passing through the DVR). Fig. 6(d) illustrates that the proposed FCI method limits the maximum fault current to about 2.5 times the nominal value of the load current and interrupts the fault cur-rents in less than 2 cycles. Fig. 6(e) depicts variations of the dc-link voltage during the FCI operation, and indicates that the dc-link voltage rise under the worst case (i.e., a severe three-phase fault) is about 15% and occurs during the first 5 ms after fault inception.

B. Phase-to-Phase Downstream Faults:

The system of Fig. 4 is subjected to a phase-A to phase-C fault with the resistance of 0.05 at 10% of the cable length connecting to , at 20 ms. When the DVR is inactive (bypassed) during the fault (Fig. 7), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11 times the rated load current Fig.

8 illustrates that when the DVR is in service, the proposed FCI control successfully interrupts the fault current and restores the PCC voltage of the faulty phases within two cycles. Fig. 8(e) shows that the dc -link voltage rise is less than 7%. Fig. 8 also shows that only the two faulty phases of the DVR react, and the healthy phase is not interrupted.

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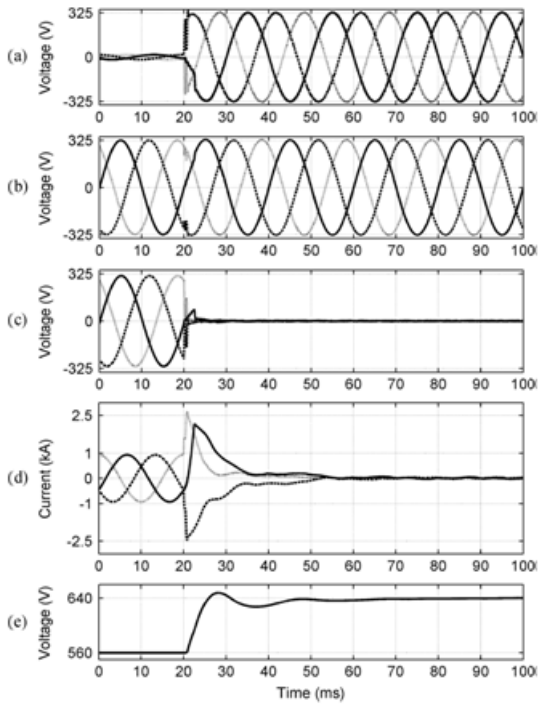

Fig. 6. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the three-phase downstream fault.

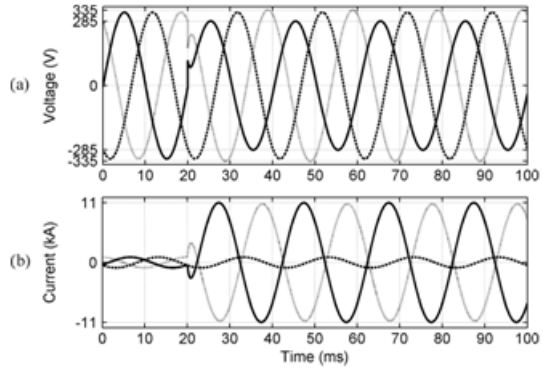

Fig. 7. (a) Voltages at Bus3 , (b) Fault currents, during downstream phase-to phase fault when the DVR is inactive (bypassed).

C.Single-Phase-to-Ground Downstream Fault:

Phase-A of the system of Fig. 4 is subjected to a fault with the resistance of 0.2 at 10% length of the cable connecting to , at 20 ms. If the DVR is inactive (Fig. 9), the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the overcurrent relays is considerable for a fault current of about 2.5 p.u. Fig. 10 illustrates that the proposed DVR control strategy successfully interrupts the fault current in the faulty phase in about two cycles. Fig. 10(e) shows that the dc-link voltage rises less than 1.8%. Fig. 10 also shows that only the faulty phase of the DVR reacts to fault current, and the healthy phases are not interrupted.

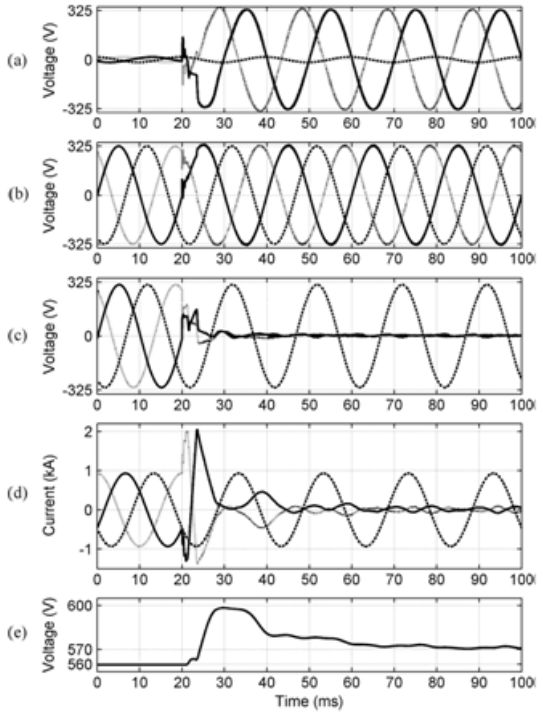

Fig. 8. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the phase-to-phase downstream fault.

Simulation studies conclude that the dc-link voltage rise caused by the proposed FCI mode of operation is proportional to the fault current, and depends on the type of fault. The results also indicate that the maximum dc-link voltage rise occurs under the most severe three-phase fault which is about 15%, and can be tolerated based on DVR appropriate design.

It must be noted that to prevent operation of three -phase in-duction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such condi-tions and disconnect the load when any of the phases is de-en-ergized by the single-phase

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operation of the FCI function. Fur-thermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the op erator can decide either to use or disable this function depending on the type of load.

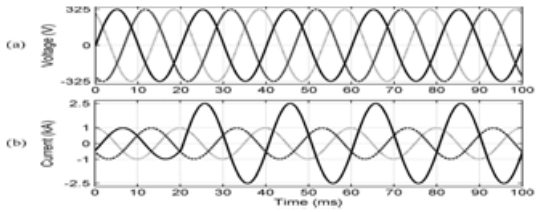

Fig. 9. (a) Voltages at bus3. (b) Fault currents, during the downstream singlephase- to-ground fault when the DVR is inactive (bypassed).

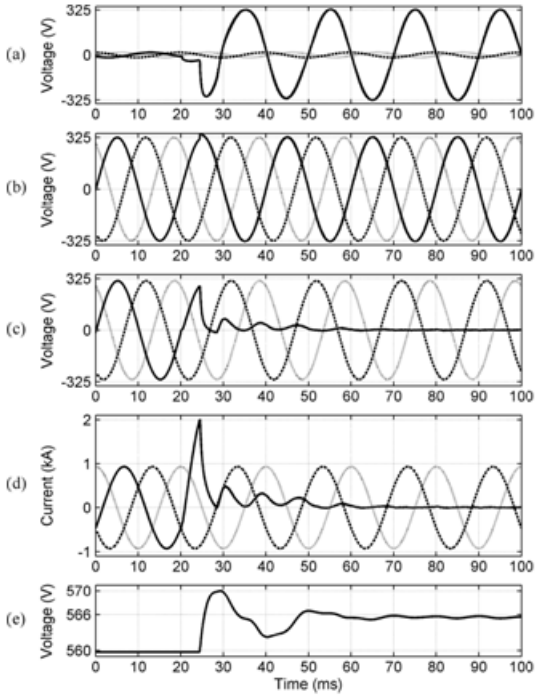

Fig. 10. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground downstream fault.

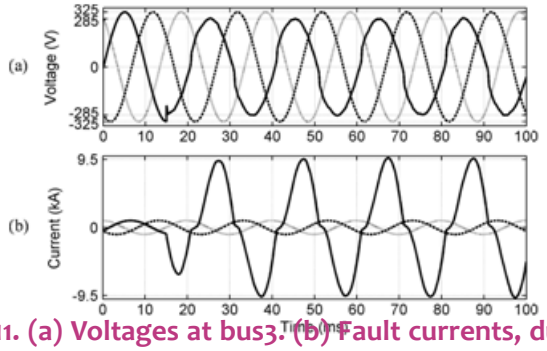

Fig. 11. (a) Voltages at bus3. (b) Fault currents, during the downstream singlephase- to-ground arcing fault when the DVR is inactive (bypassed).

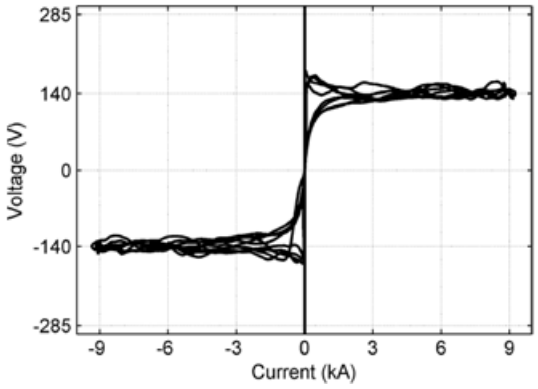

Fig. 12. Nonlinear - characteristic of the arc.

D. Effect of the Fault v-i Characteristic:

Due to the nonlinear v-i characteristic of a free-burning arc, the voltage and current waveforms are highly distorted during an arcing fault. To investigate the effects of such distortions on the performance of the proposed FCI control scheme, a single-phase-to -ground downstream arcing fault at is considered. The arc is modeled based on the modified Cassie–Mayr equations [28]. The effect of variation of the arc length on the arc voltage [29] is also taken into account.The fault is initiated at 15 ms on phase A. When the DVR is inactive (bypassed), Fig. 11, the PCC voltage drops to 0.87 p.u., and the fault current rises to about 9.5 p.u. Fig. 12 shows the time-varying nonlinear - characteristic of the arc during this fault. Fig. 11 shows the PCC voltage, and the fault current waveforms are highly distorted as a result of the fault - characteristic. This is confirmed by the frequency spectrum of the voltage waveform as depicted in Fig. 13. The performance of the proposed FCI control scheme during the arcing fault is illustrated in Fig. 14. Fig. 14 shows that the proposed control strategy successfully interrupts the arcing fault current in the faulty phase in half a cycle (i.e., even faster than that of the bolted fault conditions). The reason is that the re-sistance of the arcing fault provides higher damping for the de-caying dc component of the fault current.

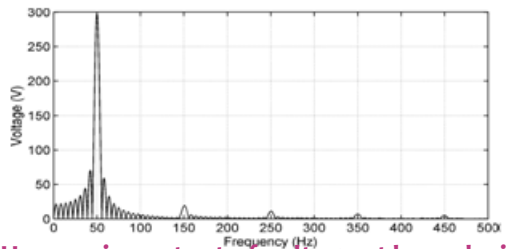

Fig. 13. Harmonic content of voltage at bus3 during the arcing fault.

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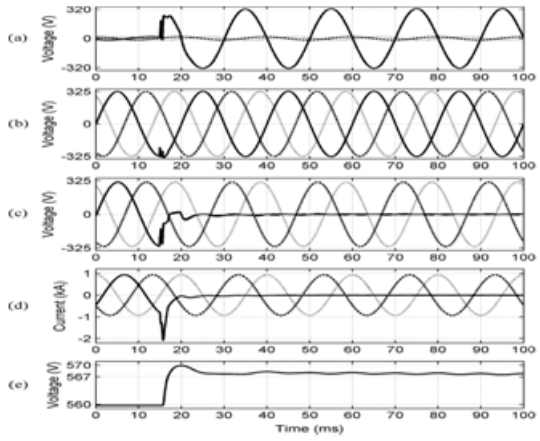

Fig. 14. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground downstream arcing fault.

E. Simultaneous FCI Operation and Sag Compensation:

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At 15 ms, the system of Fig. 4 is subjected to a phase-A to phase-B fault with the resistance of 1 at 90% of the line length from. The fault causes 87% voltage sag at the PCC. At 55 ms, another fault with the resistance of 0.2 on phase-A at 10% length of the cable connecting to occurs. The upstream fault is cleared by relays at 93 t=ms.

Fig. 15 shows the performance of the proposed DVR control system under the aforementioned conditions (i.e., simultaneous FCI operation and sag compensation). Fig. 15 shows that when the downstream fault occurs in phase-A, the operation mode of the DVR in phase-A changes from sag compensation to FCI operation. However, the DVR continues to compensate the sag in phase-B to restore the load voltage in this phase. Consequently, phase-A and phase-B of the DVR operate in sag compensation mode during 15 < t < 55 ms. During 55 < t < 93ms, phase-A is in FCI operation mode, and phase-B continues to compensate the sag. During t > 93 ms, phase-B is in standby mode since the upstream fault is cleared and phase-A continues to interrupt the downstream fault current. During the entire process, phase-C is in standby mode.

Fig. 15(d) depicts variations of the dc-link voltage and indicates that the dc-link voltage drops during sag compensation, but the FCI operation maintains the dc-link voltage when it is lower than a certain value (the dc-link voltage, which is needed to reduce the load voltage to zero). This continues until the capacitor voltage approaches the aforementioned threshold. The reason is that when the capacitor voltage is lower than a certain value, the magnitude of the voltage injected by the DVR, which must be 180 out of phase with respect to the source voltage, is less than the source voltage magnitude. Thus, small current flows through the DVR until the capacitor is charged. This current result in active power absorption by the DVR.

Fig. 16 shows the effect of lower initial dc-link voltage on the FCI operation during a phase-A to ground fault with the resistance of 0.05 at 10% length of the cable connecting to , at 15 ms. If the DVR is inactive (bypassed) during the fault, the fault current increases to about 7 times the rated load current. Fig. 16(a) shows that even under very low dc-link voltage conditions, the FCI control limits the fault current to less than the nominal load current in about one cycle. Fig. 16(b) shows that regardless of the initial dc-link voltage, the dc-link capacitor is charged up to a voltage which is adequate to inject a voltage equal to the supply voltage and fully interrupt the fault current.

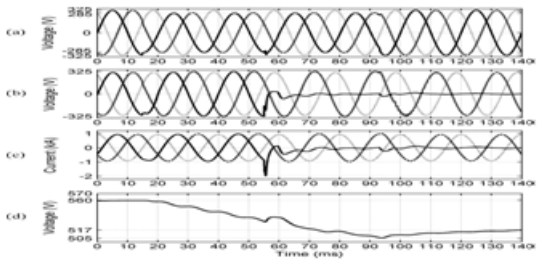

Fig. 15. (a) Source voltages. (b) Load voltages. (c) Line currents. (d) DC-link voltage, during phase-A to ground downstream fault which takes place during sag compensation in phases A and B.

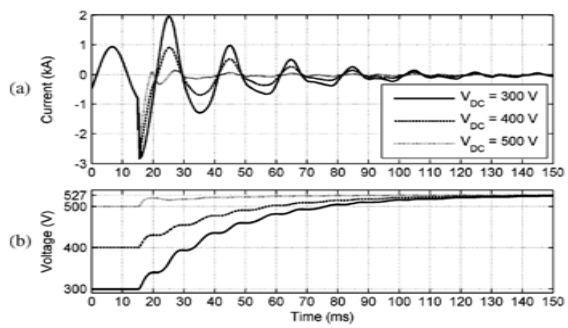

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Fig. 16. (a) Line current of phase-A and (b) dc-link voltage, for different initial values of the dc-link voltage, during downstream phase-A-to-ground fault.

IV. CONCLUSION:

This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. This control function is an addition to the voltage-sag compensation control of the DVR. The performance of the proposed controller, under different fault scenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in the SIMULINK environment. The study results conclude that:

- The proposed multiloop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter;

- the proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz);

- the proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, to less than 15% and enables the DVR to restore the PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltage conditions.

- the proposed control system also performs satisfactorily under downstream arcing fault conditions.

APPENDIX A
DVR MODEL PARAMETERS

Parameters of the studied power system and the DVR are as follows:

Short-circuit current at Bus1 : 31.5 kA, X/R at Bus1:5.67

$\omega = 2\pi \times 50$ rad/s

TABLE I
TRANSFORMER PARAMETERS

Transformer	T_1, T_2	T_3	T_s
Rated Power (MVA)	90	2	0.175
No load losses (p.u.)	0.001	0.00205	0.003
Copper losses (p.u.)	0.0048	0.0097	0.02
Leakage reactance (p.u.)	0.237	0.06	0.05
Primary voltage rating (kV)	230	20	0.4
Secondary voltage rating (kV)	20	0.4	0.245
Winding connection type	YnD	DYn	---

TABLE II
VSC PARAMETERS

Parameter	Value
Switching frequency (unipolar SPWM)	3 kHz
DC-link rated voltage	560 V
DC-link capacitor	100 mF
Harmonic filter capacitor C_f	300 μF
Harmonic filter inductor L_f (leakage inductance of T_s)	56.82 μH

cable (150 m):

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