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Simulation of Low Power Energy Recovery Type Synchronous Circuit Design

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Abstract:

The major portion of total power in highly synchronous systems is dissipated in the clock network. Hence, energy recovery clocking is a much needed low power solution. In this method the clock is a trapezoidal signal that recycles the energy from the clock network capacitances to the supply voltage. Clock gating is another technique for reducing clock power as well as the power dissipated in the data circuits.Energy recovery is a technique developed for low power digital circuits.

Energy recovery clocking is an effective method for reducing the clock power in which the conventional square wave clock signal is replaced by a trapezoidal clock .This modification in the clock signal prevents the application of existing clock gating solutions. In this project, a clock gating solution for energy recovery clocking is proposed by gating the flip-flops. In this paper, we propose a design of negative edge triggered flip-flop with the clock gating feature.Electric Tool is used to design the schematic and layout level diagrams of our project. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of our generated layout and schematic blocks.

Keywords:

Adiabatic switching, energy recovery flip-flops, clock gating, negative edge triggering.

I. INTRODUCTION:

Energy recovery circuits achieve low energy dissipation by recycling the energy stored on capacitors by using an AC type (oscillating) supply voltage [1, 2]. The major portion of total power in highly synchronous systems is dissipated in the clock network. Hence, energy recovery clocking is a much needed low power solution [3]. In this method the clock is a trapezoidal signal that recycles the energy from the clock network capacitances to the supply voltage. Replacing the conventional square wave clock signal with a trapezoidal one requires modifications in the design of the flip-flops. Recently new flip-flops have been developed to operate with energy recovery clock signals [2, 3].

Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the flip-flops themselves due to non-adiabatic switching. Clock gating is another technique for reducing clock power as well as the power dissipated in the data circuits [4].In this paper, we propose a clock gating by modifying the design of the energy recovery DSPFF(dual static edge triggered FF) that eliminates any energy loss on the internal clock and other nodes of the flip- flops. In this paper we also propose a negative edge triggering in energy recovery clocked flip-flop by modifying the DSPFF(dual static pulse edge triggered flip-flop).This paper aims at introducing a negative edge triggered energy recovery flip flop for the first time in the literature and also brings about reduction in power dissipation by adopting a clock gating feature .

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Section I explains about adiabatic switching in detail. Section II discusses on negative edge triggered energy recovery flip-flops and section III is about clock gating. Section IV presents the simulation results.

I. ADIABATIC SWITCHING:

In conventional CMOS logic circuits each switching event causes an energy transfer from the power supply to the output node or from the output node to the ground. During ago-to-VDD transition of the output, the total output charge Q =C load * VDD is drawn from the power supply at a constant voltage. Thus, an energy of E supply = C load* vide is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level V dd means that at the end of the transition, the amount of stored energy in the output node is E stored = C load VDD2/2.

Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node [1].This injected energy is ultimately dissipated to the ground, when the NMOS network is ON. During a VDD-to-O or logic 1to 0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network.

To reduce the dissipation thus occurring , the circuit designer can choose one of the three ways, namely, 1) minimize the switching events or the frequency of switching,2) decrease the nodal capacitance or minimize the size of the devices, by scaling down the technology and 3) reduce the voltage swing or supply voltage, or apply a combination of these methods. Yet in all these cases, the energy drawn from the power supply is used only once before being dissipated to the ground.
To increase the energy efficiency of the logic circuits, other conventional methodologies have been researched upon. One such a method is the possibility of reducing the power dissipation by recycling the energy drawn from the power supply at each node before it reaches the ground. These novel classes of logic circuits are called Adiabatic Logic Circuits or Energy Recovery Logic Circuits. They offer the possibility of reducing the energy dissipated during the switching events, by the process of recycling, or reusing, some of the energy drawn from the power supply [1].

The word adiabatic describes the thermodynamic process that exchanges no energy with the environment. Therefore, no energy loss in the form of dissipated heat is incurred by the process [2]. However, in real-life computing applications, such ideal processing conditions cannot be achieved because of the presence of dissipative elements such as resistances of the circuit.

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed [2]. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems.

II.NEGATIVE EDGE TRIGGERED ENERGY RECOVERY FLIP-FLOP:

Fig.l.a.shows the structure of a modified DSPFF (dual static pulse flip-flop) for negative edge triggering .In synchronous circuits, there is a wide requirement for negative edge triggering, but it has not been discussed in the literature before. This paper introduces a negative edge triggered energy recovery flip-flop along with a clock gating feature.

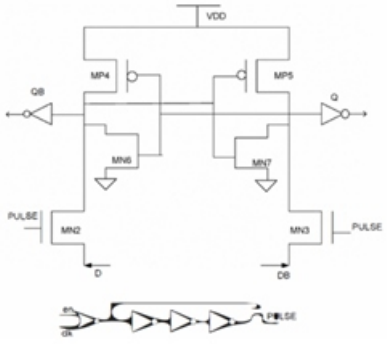

Fig.l.a.Modified DSPFF for negative edge triggering and clock gating

The pulse generator shown consists of 4 inverters to provide the pulse signal of which the first inversion is done by the NOR gate.

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This NOR gate is the clock gating introduced in the design which is explained in section III. The output pulse signal from the pulse generator is given to both the pass transistors MN2 and MN3. These two transistors capture the data during the pulse window. Data inputs have direct access to the static nodes S and SB. Hence this structure has negligible delay. The node that is at zero voltage floats when the pulse is finished. This creates short circuit currents on the next inverter or it may cause a functional failure. The transistors MN6 and MN7 prevent the nodes S and SB from floating at any time. In this design the pulse generated has a little latency relative to the clock edge & hence has negative setup time. The pulse generator can be shared among a group of flip-flops to reduce the area overhead.Waveforms for pulsed clock generation is shown in Fig.2.

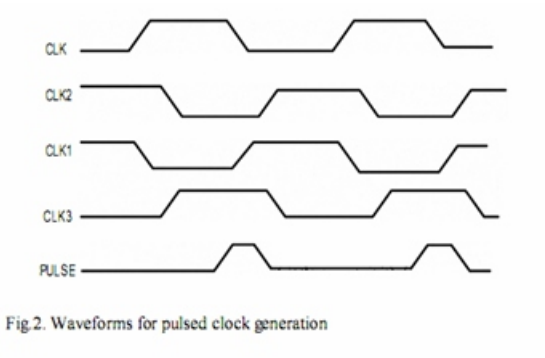

Fig.2. Waveforms for pulsed clock generation

Fig.2. Waveforms for pulsed clock generation

III. CLOCKGATING SCHEME USING NOR GATE:

In synchronous digital systems, clock signals are needed for timing references in computation and communication .The increasing demand for high performance VLSI designs results in increasing clock frequency and integration of more components on a chip .This results in increased power consumption which is a major obstacle .

The cooling costs are higher and the increased power consumption reduces the battery lifetime in portable applications .The major fraction of the power is wasted in the clock network which necessitates the requirement of the low power clocking schemes. The traditional CMOS circuits operated by timing clocks incur more than 65% of the total power dissipation of the chips in the clock network trees.

Hence, design solutions to reduce the power dissipation in the clock tree have been proposed. One of the main approaches has been the clock gating method, in which macro or micro level clock gating solutions are realized through selectively allowing the clock signals to the required part of the circuits.

Focus has been recently made onto the use of such clock gating solutions, in the operation of the adiabatic circuits. As opposed to square wave clocking, the clock gating cannot be implemented by insertion of masking logic gates at any arbitrary node on the clock network [5]. This is due to the reason that insertion of such logic gates on a sinusoidal clock network destroys the shape of the clock and hinders the energy recovery property in the downstream fan-out capacitances of the clock network. Hence, our work strives for proposing a novel approach to clock gating of energy recovery clock by inserting the gating feature inside flip-flops themselves.

That is in the macro level design of circuits. It can be noted that the energy recovery clocked flip flops shown in Figs. I (a) cannot save the power during sleep mode if the clock is still running [I]. There are two components of power dissipation in flip-flops, namely, clock circuit power (power of logic gates connected to the clock) and data circuit power (power of the rest of the flip-flop circuit). We have isolated the clock circuit power from the data circuit power in our power measurements to identify the design advantage of our circuit in a justifiable manner.

The presence of clock enables the operation of the circuit. Disabling the clock circuit (inverter gates connected to the clock input as shown in Fig. 2) in the idle state can therefore eliminate both power dissipation due to the clock circuit and that due to the data circuit [6]. Hence, deactivation of the inverter gate through the use of disabling signal with the use of the NOR gate is realized in the circuit shown in Figs. I (a) This proposed approach implements the clock gating solution inside energy recovery clocked flip-flop .The proposed clock gating results in 14% reduction in power in the clock network (when using negative edge triggered flip-flop) Clock gating is implemented by replacing the inverter with the NOR gate as shown in the figure I.a. The NOR gate has two inputs, namely, the clock signal and the enable signal [3].In the active mode, the enable signal is low so that the NOR gate behaves as an inverter.

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Then, the flip-flop operates just like the original flip-flop. In the idle state, the enable signal is set to high. This disables the internal clock by setting the output of the NOR gate to zero. This turns off the pull down path through transistor MN2 and prevents any evaluation of the data input. Hence, it can be observed that I) the internal clock is stopped, thus saving the power dissipation in the clock network and 2) all the internal switching is prevented where the clock is not supplied and data is not consequently processed. This creates power dissipation reduction in the data circuits.

IV. SIMULATION RESULTS:

A.DSPFF for negative edge triggering and clock gating:

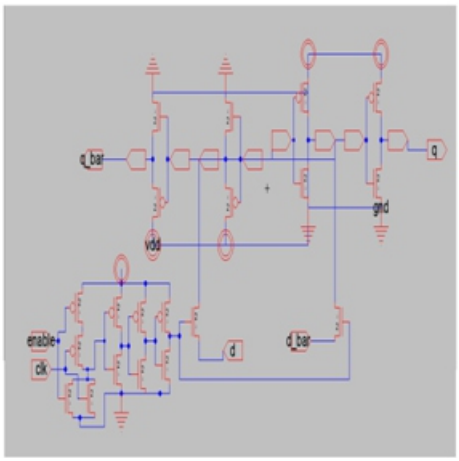

Fig.3. DSPFF for negative edge triggering and clock gating

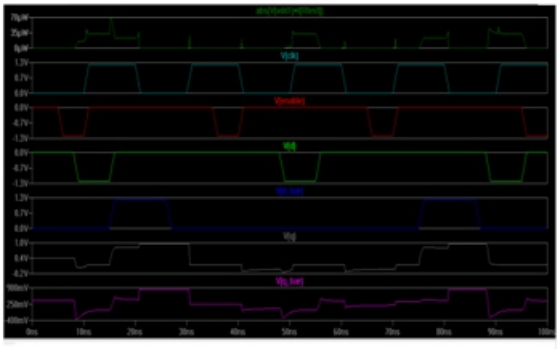

Fig.4.Simulation of DSPFF for negative edge triggering and clock gating

B. Application

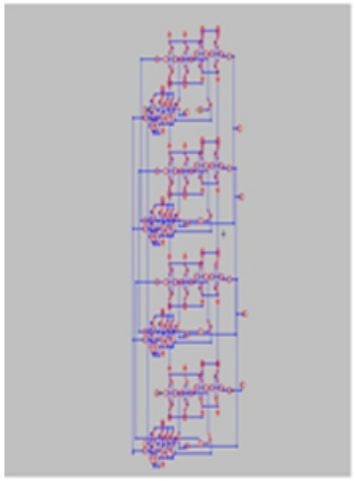

Fig.5.SIPO SCHEMATIC DIAGRAM

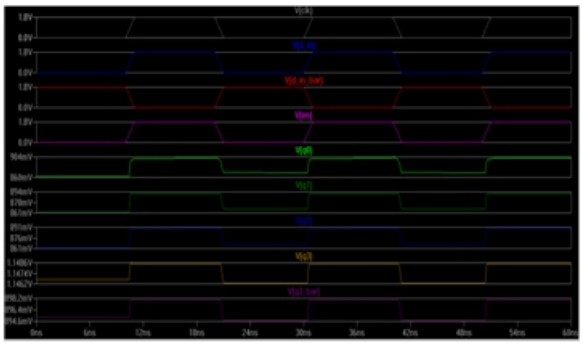

Fig.6.Simulation of Serial in parallel out

Table-I
Power Comparison

Type	Power dissipation In the data Network(in µw)
Flip flop	240
DSPFF	8.9641

V. CONCLUSION :

This paper focuses on the clock network of the adiabatic circuits which is the major dissipating element of any circuit. The clocked flip-flops are always positive edge triggered although there is a need for the negative edge triggered flip-flops in the synchronous circuits.This paper introduces a negative edge triggered energy recovery flip-flop along with a added clock gating feature .The simulation results precisely shows that the proposed design is highly power efficient and is suitable for power efficient applications .In future, the other types of energy recovery flip-flops may be altered for triggering in the falling edge of the clock and may be simulated for power results.

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