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Power optimization of spread spectrum clock generator using glitch free nand based DCDL

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Abstract:

This paper presents power optimisation of SSCG using glitchfree nand based DCDL. The recently proposed NAND-based digitally controlled delay-lines (DCDL) present a glitching problem which may limit their employ in many applications. In this proposed system we presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications.The proposed NAND based DCDL is designed by using two delay controls.Proposed DCDLs have been designed in a 90-nm CMOS technology and compared, in this technology, to the state-of-the-art.

Simulation results show that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with the lowest delay. Simulations also confirm the correctness of developed glitching model and sizing strategy. As example application, proposed DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The employ of proposed DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs.

INTRODUCTION:

In electronics a dealy-locked loop(DLL) is adigital circuit similarto a phase-lockedloop(PLL)but internal voltage controlled oscilater is not present in the DL-Las like PLL.the DLL is also used for clock-recovery.a DLL can be seen as anegative-dealy gate placed in the clock path of a digital circuit.The DLL transmission does not have low clock skew between output clock signals propagation dealy and advanced clock domain control.A DCDL are designed glitch free and it is implemented in the application for the better performance.

A necessary condition to avoid glitching is designing a DCDL which have no-glitch in presence of a dealy control code switching this is a major issue at the DCDL-design level.The project carrier out with the glitch free NAND based dealy elements which have good resolutionso that the better performance can be obtainedin the digital application.The application used in this project was dealy locked loop(DLL).This paper contributed to the glitch free DCDL with the driving circuits for the dealy control bits of the glitch free DCDL implemented in the deealy locked loop.

The dll has dealy line phasecomparator and shift register as the components.The digram ofthe register-conrolled DLL(RDLL).The feedback clock signal is the delayed version of the input clock signal and the shift register controls the amount of the dealy time.The pc compares the phases of the input clock signal and output clock signal.The output of the PC is used to control the shift register.The input clock signal is a common input for every dealy stage.At any time only onebit of the shift register is active to select a point of entry of the dealy line for the input clock signal.the no.of the dealy stages which the input clock signal goes throughdeterminestotal amount of dealy.The loop is locked and will not alter untill the phase error excedds the unit dealy again.The RDLL is determined and the unit delay of the dealy line and the total dealy time of the dealy line.

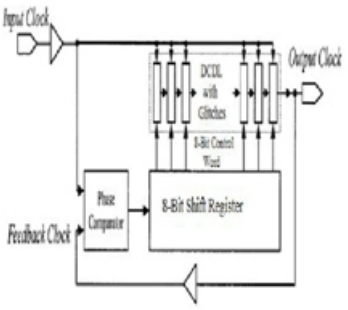

fig:1Dllwith glitching DCDL

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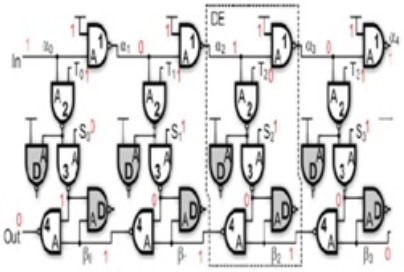
The phase dector orphase comparator is a logic gate that generates a volatage signal which represent the difference in phase between two signals inputs. It is an essential elements of phase-locked loop.Detecting phase difference is very importantin many applications such as Radar and telecomunaction systems servo mechanisms and demodulators.

DLL with glitch free NAND-based DCDL:



The minimum dealy t min of proposed inverting solution is higher than the tmin of the nand based DCDl.In this circuit it is interseting to observe that the first DE is never in past-turn state to always1.The observation allows to construct a non-inverting DCDL by modifing only the first DE.In this circuit the NAND gates 1and 2 of the1st DE have-been detecting together.the signal α1 of the second DE is now equal to in the whole behaviour of the DCDL is non-inverting.This topology maintains the same tr(2.tnand) of the previous solution while it can easily verifed that the minimum dealy tminis nand2.The TNAND the non inverting DCDL maintaince the same performance of the NAND-based DCDL.The simulation confirms that noglitching is obtained at the output and this results in a correct DCO operation.IN fact the simulatio shows that the DCO output switchies correctly from 500to333mhz and back to500mhz without any glitches or any problem .In the glitching DCDl circuit consider only one control bit is used.when there is a sudden switching takes place in the control bit glitches.

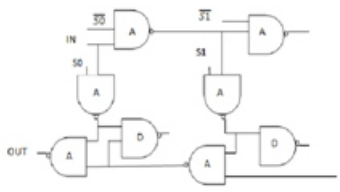
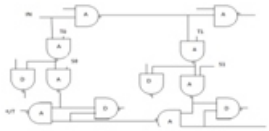


Fig3:Block diagram of the conventional DCDL with one control bit

This conventational DCDL was designed with NAND cell AS lattice structure in the figure2.the cell which is denoated by A is the fast inputof the NAND gate.The gates denoated by D is the dummy cellforthe load blanching. These dealy elementsare controlled by one bit control code 'c'to propagate the dealy.when the dealy control code 'c'increased by1,multiplepropagation path with in the DCDL structure generates leads to moreglitching in the dealy line.The control bit SI=o(pass state)SI=1(turn state).In DCDL applicaation to avoide DCDL output glitching the switching of dealy control bits is synchronized with the switching of the input signal.Glitching is avoided if the control bits arrival time is lower than the arrival time of input signal.

GLITCH FREE NADND BASED DCDL WITH TWO-CONTROL BITS:



The stracture proposed in this control bits to control the dealy elements in that 'A' denoates the fast input of the NAND gate 'D'denoates the dummy cell for the load balacing.Two control bits Ti and Si are used to synchronize the arrival of the input and the arrival of the control bits.It has 3 possible states. The DESi with are in pass-state (Si=0,TI=1),in this state the nand 3 outputs is equal to 1 and nand4 allows the signal propagation in the lower nand gates chain.The DE with I=c is in turn state(Si=Ti=0).In this state the upper input of the DE is passedto the output of nand3 the next DE(i=ct) is in past-turn-state.In this DE the output of the NAND4 is stuck-at 1 by allowing the propagation in this previous DE of the output of NAND3 through NAND4.all remaining DES are again in turn-state .

	IMPLEMENTATION OF CONVENTIONAL DCDL IN ADDLL	IMPLEMENTATION OF PROPOSED DCDL IN ADDLL
POWER(mV)	315	209
AREA(Gate count)	1410	1134
DELAY(ns)	7.107	6.057

The correspoinding Si and Ti values are summarized in table.The simulation results shows that the proposed NAND based DCDL confirms.The glitches free propagation in dealy elements.

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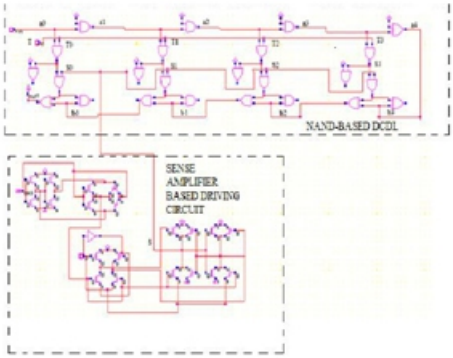
PROPOSED DCDL:

The proposed DCDL uses dual edge triggered sense amplifier Flip-flop as a driving circuit.This shwon in figure by using this proposed driving circuit.The power and dealy time of existing.Glitch free NAND-based DCDL is reduced.The sense amplifier based dual triaggered flip-flop in fig consists of three stages.Those are pulse generating sensing and latching stages.1st stage is used to generate the pulses.2nd stages is used to sense the pulses and 3rd stage is used to produce the output during the rising and falling edges.

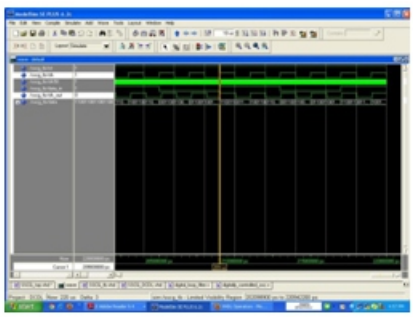


EXISITING NAND BASED DCDL:

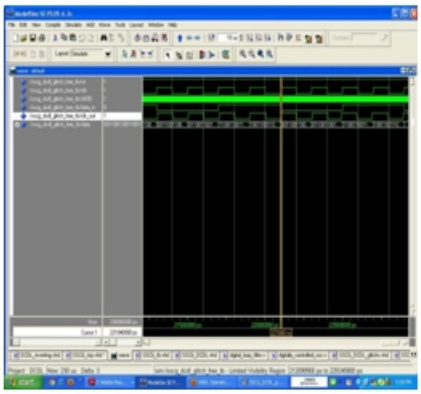
The existing NAND based DCDL.It consists of a NAND based lattice dealy units which is cascaded for largedeallines in application

SIMULATION RESULT:

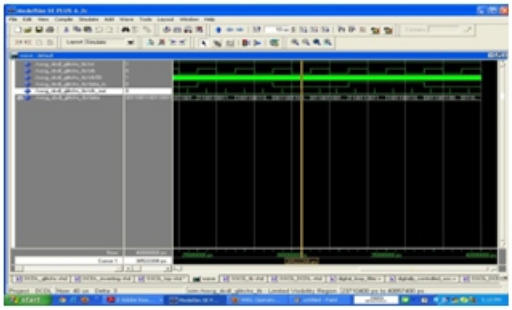
1. . SSCG DCDL GLICTH FREE



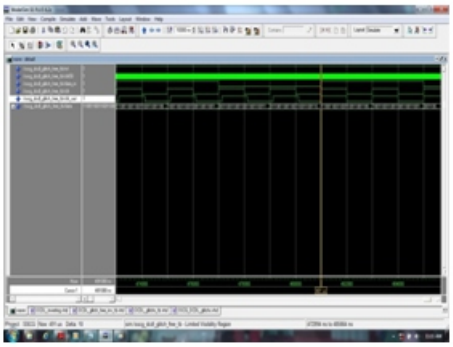
2. SSCG DCDL GLICTH FREE 1



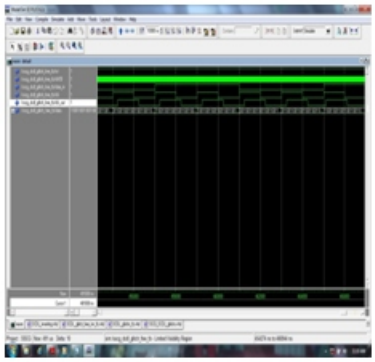
3. SSCG DCDL WITH GLITCH



4. SYCHRONISED WITH INPUT CLOCK



5. UNSYCHRONISED



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CONCULSION:

In the projects the occurrence of glitches and its effect on dealy line has been developed. The glitches free NAND based DCDL is implemented in the DLL.

Iso sutiable timing constraints for the control bits in the DCDL are analyzed.Area power and dealyanalysis for the both conventional and proposed DCDL is also compared.This results shows that the dealy is minimal in the glitch free NAND based DCDL.

Futher modificationcan be doneby ading the finate .Dealy unit(FDL)with the lattice dealy unit for better resolutionand also suitable driving circuits can also be designed.

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