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Area-Delay Efficient Binary Adders in QCA

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Abstract:

As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state-of-theart competitors and achieves the best area-delay tradeoff. The above advantages are obtained by using an overall area similar to the cheaper designs known in literature. The 64-bit version of the novel adder spans over 18.72 μm2 of active area and shows a delay of only nine clock cycles, that is just 36 clock phases.

Keywords:

Adders, nanocomputing, quantum-dot cellular automata (QCA).

I. INTRODUCTION:

Quantum-dot cellular automata (QCA) is an attractive emerging technology suitable for the development of ultradense low-power high-performance digital circuits [1]. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits [2]–[16], with the main interest focused on the binary addition [11]–[16] that is the basic operation of any digital system. Of course, the architectures commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry (RCA), carry look-ahead (CLA), and conditional sum adders were presented in [11]. The carry-flow adder (CFA) shown in [12] was mainly an improved RCA in which detrimental wires effects were mitigated.

Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA in [13] and [14]. Recently, more efficient designs were proposed in [15] for the CLA and the BKA, and in [16] for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA.

Theoretical formulations demonstrated in [15] for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.

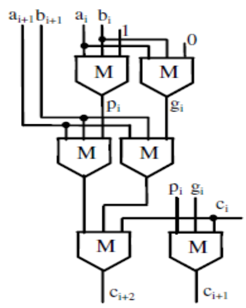

Fig. 1. Novel 2-bit basic module .

An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-of the- art competitors and achieves the lowest area-delay product (ADP).

The rest of this brief is organized as follows: a brief background of the QCA technology and existing adders designed in QCA is given in Section II, the novel adder design is then introduced in Section III, simulation and comparison results are presented in Section IV, and finally, in Section V conclusions are drawn.

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II. BACKGROUND:

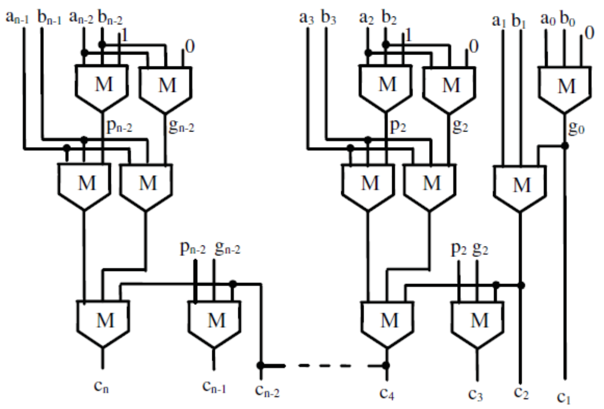
A QCA is a nanostructure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell [1].Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations P) determine two possible stable states that can be associated to the binary states 1 and 0. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality.

To achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock scheme, named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch [8]. QCA cells are used for both logic structures and interconnections that can exploit either the coplanar cross or the bridge technique [1], [2], [5], [17], [18].

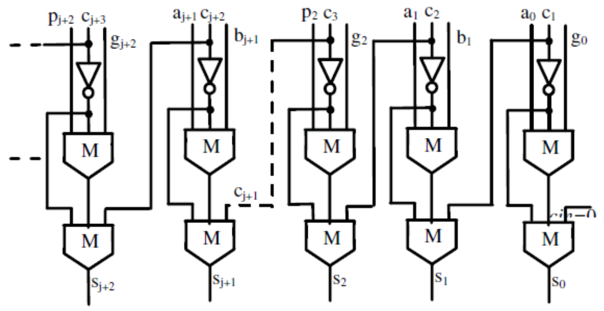
The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs a, b, and c, the MG performs the logic function reported in (1) provided that all input cells are associated to the same clock signal clkx (with x ranging from 0 to 3), whereas the remaining cells of the MG are associated to the clock signal clkx+1

M(abc) = a • b + a • c + b • c……………. (1)

Several designs of adders in QCA exist in literature.The RCA [11], [13] and the CFA [12] process n-bit



(a)



(b)

Fig. 2. Novel n-bit adder (a) carry chain and (b) sum block

operands by cascading n full-adders (FAs). Even though these addition circuits use different topologies of the generic FA, they have a carry-in to carry-out path consisting of one MG, and a carry-in to sum bit path containing two MGs plus one inverter. As a consequence, the worst case computational paths of the n-bit RCA and the n-bit CFA consist of (n+2) MGs and one inverter. A CLA architecture formed by 4-bit slices was also presented in [11]. In particular, the auxiliary propagate and generate signals, namely pi = ai + bi and gi = ai • bi ,are computed for each bit of the operands and then they are grouped four by four. Such a designed n-bit CLA has a computational path composed of 7+4×(log4 n) cascaded MGs and one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which only one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path.

In addition, to compute the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that, to process nbit addends, log4 n levels of CLA logic are required, each contributing to the computational path with four cascaded MGs. Finally, the computation of sum bits introduces two further cascaded MGs and one inverter. The parallel-prefix BKA demonstrated in [13] exploits more efficient basic CLA logic structures. As its main advantage over the previously described adders, the BKAcan achieve lower computational delay. When n-bit operands are processed, its worst case computational path consists of 4×log2 n−3 cascaded MGs and one inverter. Apart from the level required to compute propagate and generate signals, the prefix tree consists of 2 × log2n – 2 stages.

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From the logic equations provided in [13], it can be easily verified that the first stage of the tree introduces in the computational path just one MG; the last stage of the tree contributes with only one MG; whereas, the intermediate stages introduce in the critical path two cascaded MGs each. Finally, for the computation of the sum bits, further two cascaded MGs and one inverter are added.

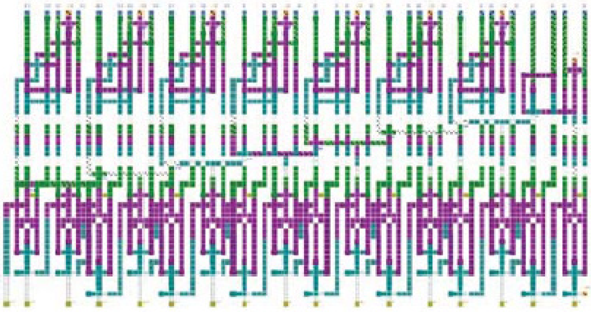

Fig. 3. Novel 16-bit adder.

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Temperature	1 K
Relaxation time	1×10^{-15} s
Time step	1×10^{-16} s
Total simulation time	7×10^{-11} s
Radius of effect	80 nm
Relative permittivity	12.9
Layer separation	11.5 nm

With the main objective of trading off area and delay, the hybrid adder (HYBA) described in [14] combines a parallel prefix adder with the RCA. In the presence of n-bit operands, this architecture has a worst computational path consisting of 2 × log2 n + 2 cascaded MGs and one inverter. When the methodology recently proposed in [15] was exploited, the worst case path of the CLA is reduced to 4 × _log4 n_ + 2 × _log4 n_ − 1 MGs and one inverter. The above-mentioned approach can be applied also to design the BKA. In this case the overall area is reduced with respect to [13], but maintaining the same computational path. By applying the decomposition method demonstrated in [16], the computational paths of the CLA and the CFA are reduced to 7 + 2 × log2(n/8) MGs and one inverter and to (n/2) + 3 MGs and one inverter, respectively.

III. NOVEL QCA ADDER To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two n-bit addends A = an−1, . . . , a0 and B = bn−1, . . . , b0 and suppose that for the i th bit position (with i = n − 1, . . . , 0) the auxiliary propagate and generate signals, namely pi = ai + bi andFPGA architecture logic block can be connected to the switch block. In the switch block there are four signals 1) data signal (first bit) 2) data signal (second bit) 3) acknowledgement signal 4) data arrival signal. The above four signal acknowledgement signal and data arrival signal connected to pervious logic block.

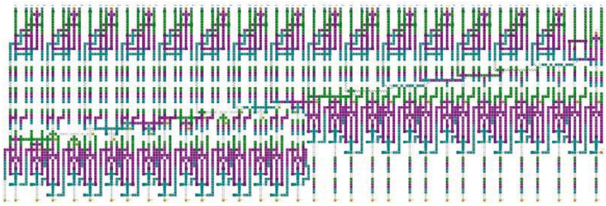

Fig. 4. Novel 32-bit adder.

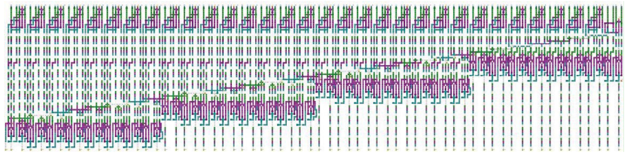

Fig. 5. Novel 64-bit adder.

gi = ai • bi , are computed. ci being the carry produced at the generic (i−1)th bit position, the carry signal ci+2, furnished at the (i+1)th bit position, can be computed using the conventional CLA logic reported in (2). T

he latter can be rewritten as given in (3), by exploiting Theorems 1 and 2 demonstrated in [15]. In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation.

In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.**Equation (3) is exploited in the design of the novel 2-bit module shown in Fig. 1 that also shows the computation of the carry ci+1 = M(pi gici). The proposed n-bit adder is then implemented by cascading n/2 2-bit modules as shown in Fig. 2(a).**

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Having assumed that the carry-in of the adder is cin = 0, the signal p0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in Fig. 2(b). It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position (i.e., g0 = 1) and then it is propagated through the subsequent bit positions to the most significant one.

In this case, the first 2-bit module computes c2, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to (n – 2)/2. Considering that further two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of (n/2) + 3 MGs and one inverter

ci+2 = gi+1 + pi+1 • gi + pi+1 • pi • ci (2)
ci+2 = M(M (ai+1, bi+1, gi) M (ai+1, bi+1, pi) ci). (3)

IV. RESULTS:

The proposed addition architecture is implemented for several operands word lengths using the QCA Designer tool [16] adopting the same rules and simulation settings used in [11]–[16]. The QCA cells are 18-nm wide and 18-nm high; the cells are placed on a grid with a cell center-to-center distance of 20 nm; there is at least one cell spacing between adjacent wires; the quantum-dot diameter is 5 nm; the multilayer wire crossing structure is exploited; a maximum of 16 cascaded cells and a minimum of two cascaded cells per clock zone are assumed.

The coherence vector engine is used for simulations with the options shown in Table I. Layouts for the 16-, 32- and 64-bit versions of the novel adder are shown in Figs. 3–5, respectively. Simulation results for the 64-bit adder is shown in Fig. 6.There, the carry out bit is included in the output sum bus. Because of the limited QCA Designer graphical capability, input and output busses are split into two separate more significant and less significant busses. Fig. 6 also shows the polarization values of few single output signals (i.e., sum64, sum32, sum31, and sum). Simulations performed on 32- and 64-bit adders have shown that the first valid result is outputted after five and nine latencyclock cycles, respectively. As an example, the 20 clock phases (or five cycles delay) of the 32-bit adder are as follows: one clock phase is needed for inputs acquisition; the carry c2 related to the least significant bit positions is then computed within the two subsequent clock phases; 15 phases are required for the carry propagation through the remaining bit positions; finally, two more phases are needed for the sum computation.

Critical path consistencies and post layout characteristics, such as cell count, overall size, delay, number of clock phases, and ADP, are shown in Table II for all the compared adders. The number of cascaded MGs within the worst case computational path directly impacts on the achieved speed performances as an MG always adds one more clock phase. However, it is worth noting that because of their different basic logics, designs with the same critical path can achieve different numbers of clock phases. As an example, the novel adder requires less clock phases than the CFA proposed in [16] to perform the generic addition operation. Table II shows that the layout strategy is also quite important.

In fact, designs using the same basic logic with the same worst case theoretical path can have different number of clock phases due to differently compact layouts.It should also be noted that the critical path of the HYBA [14] contains the fewest MGs, while the novel adder, the RCA [13] and the CFA [12] require less additional clock phases exceeding the number of cascaded MGs. This means that their layouts do not contain overlong wires, thus demonstrati ng that the novel architecture inherits logic advantages of CLA and parallel-prefix adders (i.e., the short computational path), but limiting, as happens in the RCA and CFA structures, detrimental layout effects. Comparison results shown in Table II for operands wordlengths ranging from 8- to 64-bit also show that the novel adder achieves the lowest delay and spans over an area similar to that occupied by the cheaper designs known in literature.

Therefore, our design approach allows the best area-delay tradeoff to be achieved. Table II also shows the numbers of wire crossovers for some competitors. As it is well known, wire crossovers are sensitive to fabrication imperfections and consequently they can represent a reliability issue [19]–[21]. It can be seen that the number of crossovers used in the novel 8- and 16- bit adder was 33.6% and 37% lower than the CLA

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and the BKA proposed in [15]. Unfortunately, for the adders presented in [11]–[14], [16] similar information was not available. The robustness of the proposed circuit was evaluated as a function of temperature using a simulation set-up identical to that used in [13]. Obtained results demonstrated that at 22 K, all the output cells assume correct polarizations. In fact, the cells furnishing output signals equal to zero are polarized to −0.534, whereas those providing output bits equal to 1 assume the polarization 0.534.

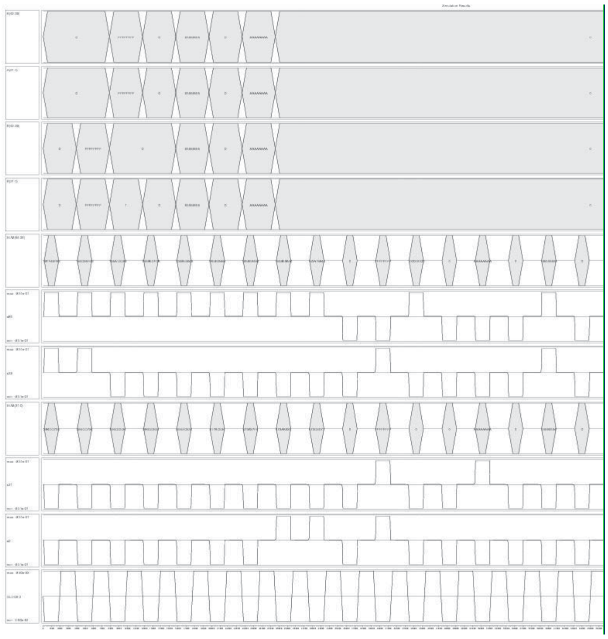

Fig. 6. Simulation results obtained for the novel 64-bit adder.

V. CONCLUSION:

A new adder designed in QCA was presented. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated in [13] and [16]. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders.

In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. A 64-bit binary adder designed as described in this brief exhibited a delay of only nine clock cycles, occupied an active area of 18.72 μm2, and achieved an ADP of only 168.48.

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