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ASIC Design of Reversible Full Adder/Subtractor Circuits

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ABSTRACT:

Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. Adders are fundamental building blocks in many computational units. For this reason, simulation of several adder circuits using the reversible gates.

This paper implements a design of Adder/ Subtractor using reversible logic gates. The first design is the implementation of two's complement Adder /Subtractor suitable for signed/unsigned numbers. The Full Adder / Subtractor is then applied to design a reversible 4-bit ripple Adder/Subtractor. /t has been shown in Cadence's tools that the reversible circuits outperform the irreversible circuits in terms of delay and power dissipation.

Keywords:

Reversible logic, Garbage output, Semi custom ASIC.

1. INTRODUCTION:

The advancement in higher-level integration and fabrication process has emerged in better logic circuits and energy loss has also been dramatically reduced over the last decades. This trend of reduction of heat in computation also has its physical limit according to Landauer, who proved that in logic computation every bit of information loss generates kTln2 joules [2] of heat energy, where k is Boltzmann's constant of1.38xlO-23J/K, and T is the absolute temperature of the environment. At room temperature, the dissipating heat is around 2.9 x 10-21 1. Energy loss by Landauer limit is important because it is likely that the growth of heat generation due to information loss will be noticeable in future.

Bennett showed that zero energy dissipation would be possible if the network consists of reversible gates only. Reversible logic has also found its applications in several disciplines such as quantum computing, nanotechnology, DNA technology and optical computing.

In modern VLSI systems power dissipation is very high due to rapid switching of internal signals. In fact zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates [3].

The paper is organized as follows. Section 2 presents an overview of reversible logic. In Section 3, we present the related work. Section 4 describes the CMOS implementation of the reversible and normal circuits. Section 5 presents the comparison of delay and power dissipation of the two logic circuits. Section 6 discusses the future improvements and section 7 concludes the paper.

2. REVERSIBLE LOGIC :

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs.

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A reversible logic gate must have the same number of inputs and outputs [3]. In an n-output reversible gate the output vectors are permutation of the numbers o to 2n-1. A reversible gate is balanced, i.e. the outputs are is for exactly half of the inputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions.

It can realize non-balanced functions only with garbage outputs. Some of the major problems with reversible logic synthesis are fan outs cannot be used, and also feedback from gate outputs to inputs is not permitted. [3] Features for any gate to become reversible gate as follows: [1]

- Number of input and output lines must be the same.
- Feedback (loop) is not allowed in reversible logic.

- Fan-out is not allowed in reversible logic; Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.

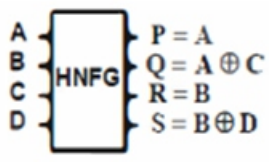
- One of the major constraints in reversible logic is to minimize the number of reversible gates used.

- Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations.

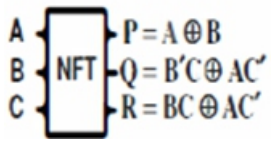
- Garbage is the number of outputs added to make an n-input koutput Boolean function «n,k)function) reversible Using minimum number of input constants.

The examples 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7 and 2.8 of Reversible gates are as follows:

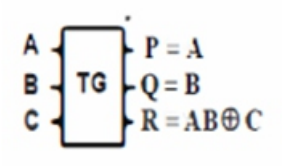
2.1 HNFG gate:



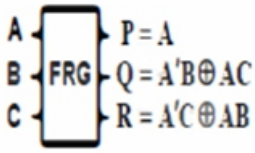
2.2 NFT gate:



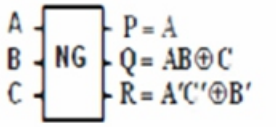
2.3 Toffoli gate:



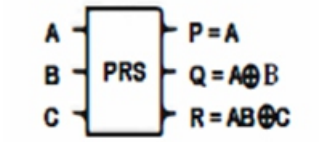
2.4 Fredkin gate:



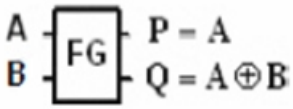
2.5 New gate:



2.6 Peres gate:



2.7 Feynmann gate:



2.8 TSG gate:

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3. RELATED WORK:

The basic building blocks of the adder circuits that are designed are initially coded and simulated to verify its functionality. The ripple carry adder is designed, simulated and synthesized. The circuit delay, number of gates, garbage output and power dissipation is found out. The comparison of ripple carry adder designed using basic gates and the ripple carry adder designed using reversible gates, with respect to power dissipation and delay is done.

4. DESIGN AND ANALYSIS REVERSIBLE AND NORMAL ADDERISUBTRACTOR:

The first design of reversible full adder/Subtractor implements the addition and subtraction of signed/ unsigned numbers. This Adder/Subtractor circuit [I] using combinational gates is shown in Figure 4.1.

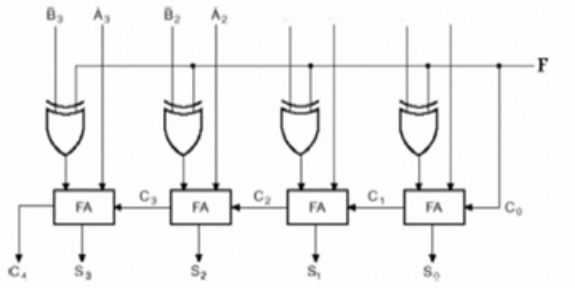


Figure 4.1 4-bit Ripple Adder/Subtractor with combinational gates

The design of reversible adder/Subtractor [1] is as shown in figure 4.2 (circuit 4.1).

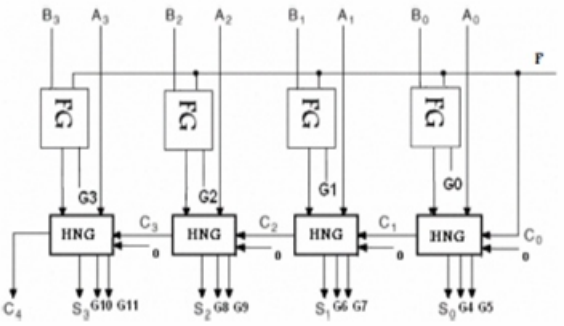


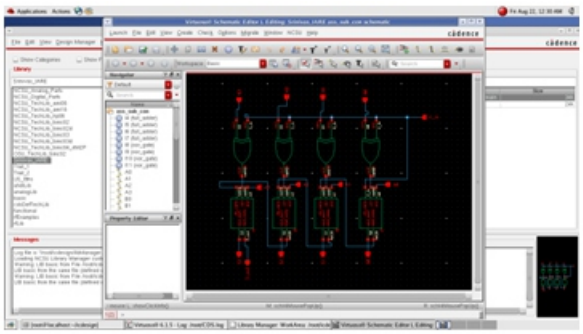
Figure 4.2 Reversible 4-bit Ripple Adder/Subtractor with ADD/SUB gate (circuit 4.2).

5. SEMI CUSTOM ASIC DESIGN:

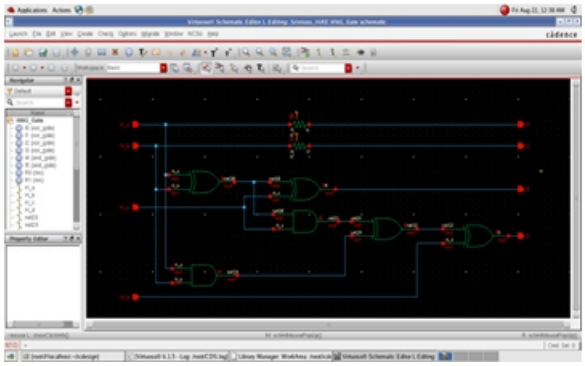
Semicustom design includes giving design specifications to schematic using Cadence's Virtuoso tool and verifying the functionality in SPECTRE. The obtained transient characteristics for the schematics and the circuit delays.The layouts for these circuits are designed using tool Assura and checked for DRC, ERC and LVS match. The post layout synthesis is obtained for both the circuits and calculated power dissipation values for both the circuits.

6. RESULTS:

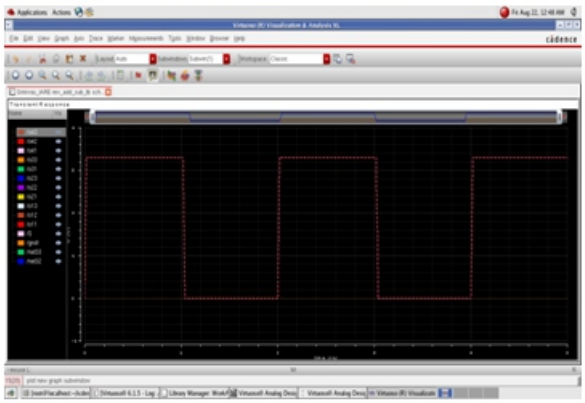
6.1 Schematic for adder/Subtractor:



6.2 Schematic for HNG gate:



6.3 Visualization & Analysis:



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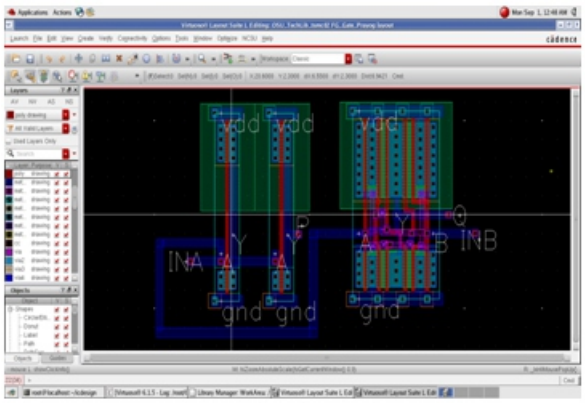
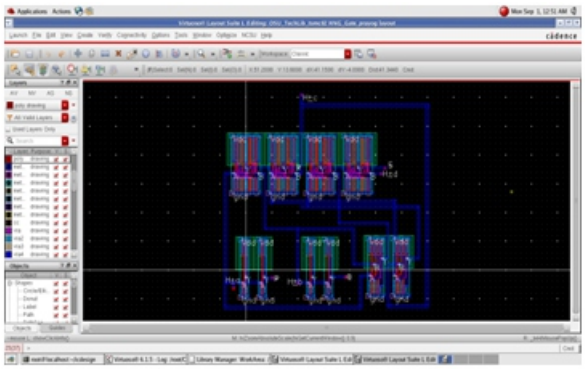
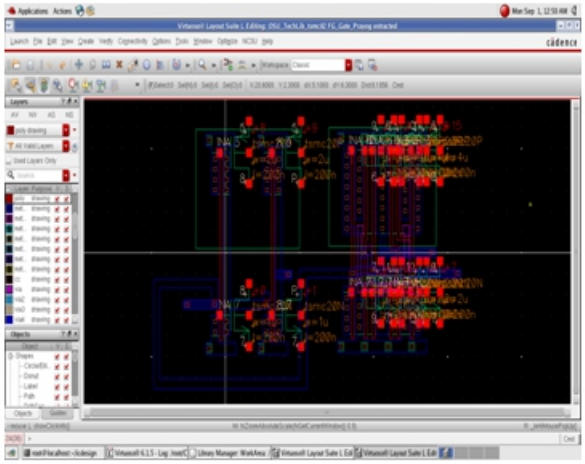
6.4 Layout of FG gate:



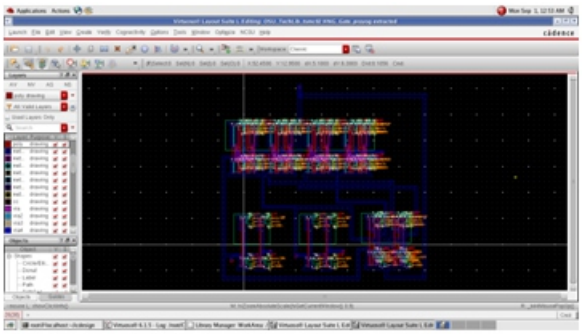
6.5 Layout of HNG gate:



6.6 Extract layout of FG gate:



6.7 Extract layout of HNG gate:



6.8 Layout of Reversible adder / Subtractor:

7. SCOPE FOR FUTURE WORK:

The Reversible adder circuits design which has combined advantages of less chip area, improved power dissipation and timing delay can be used as the building blocks in the design of reversible multipliers, arithmetic logic unit (ALU), successive approximation registers etc...

The number of garbage outputs, delay, power dissipation of the reversible adder circuits can be reduced further by improvising the design.

8. CONCLUSION:

In this paper the implementation of two types of adder circuits is presented .The simulated and synthesized results shows that reversible logic design is useful for low power digital circuits We have been successful in verifying the advantages of reversible gates over basic gates circuits.

The obtained results of our paper are as follows:

- Reversible full adder circuit has been synthesized in Cadence's RTL complier.

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• Semi-custom ASIC design of reversible full adder/ Subtractor circuit has been implemented.

• The power dissipation and worst case delay for 4-bit reversible full adder/ Subtractor are 6618.66nW and 401.6 ns.

9. REFERENCES:

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