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A Low-Power Phase locked loop using self healing Prescalar/VCO

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Abstract:

This paper deals with different approaches to design low power Phase Locked Loop (PLL) using self healing Prescalar/VCO. PLL system responds to both frequency and phase of the input signals, automatically raising or lowering the frequency of controlled oscillator until it is matched to the reference in both frequency and phase.

The performance of PLL frequency synthesizer is improved by using different Voltage controlled Oscillator (VCO) and their varactor or magnetic tuning scheme.

The self healing VCO is implemented in this paper. For the self-healing VCO, its measured frequency range is from 60 to 1489 MHz when this PLL operates at 855 MHz, the measured rms and peak-to-peak jitters are 8.03 and 55.6 ps, respectively.

A 5-stage prescaler operating up to 84GHz is presented. The prescaler requirements, design considerations, simulations, and performance measurements are presented. The first divide-by-2 stage consumes 17.7mW at 1.8V, or 26.4fJ power-delay product per gate.

The prescaler's phase noise gain degeneration at the sensitivity curve boundary is reported for the first time. It is generally desired to design low Phase noise, wide tuning, low power consumption, high quality factor and independent to Process, Voltage, and Temperature (PVT) variation.

Today's CMOS IC technology is used in many critical design aspects such as thermal noise cancelling, low-frequency noise reduction on MOSFETs, and distortion cancelling. However, here various improvements in technology from µm to nm, supply voltage from 0.7 to 1.8V,frequencygenerated from 2to78 GHz

Introduction:

The cmos –technology approches to a nanometer scale, the non-idealities such as variability and lekage curreent may significantly affect the circuit performance.

The process variability leads to the large variations to degrade the device matching and performances.It may result in only a few design a walfer to meet the target performance specifications.

The undesired leakage currents also degrade the accuracy and resolution of analog circuits and make digital dynamic circuits not to work properly.For a PMOS transistor with W/L=8Um in 65-nm process, its source and gate are connected to the supply voltage of12v.The drain current leakage current is 68.7na,0.12ua,and21ua for the typical slow-slow and fast corners respectively and 40c.

The leakage current is highly dependent upon the process varitation.The current under different corners and tempeactures with a constant VSD=1.22v the leakage current grows very fast in a high tempeacture environment.A phase locked loop (PLL) is widely employed in wire -line and wire-less communication systems .

The poor device matching and leakage current vary the common mode voltage of a ring-based voltage-controlled oscillator.It may limit the oscillation freqency range of a VCO and causes a VCO not to oscillator in a worst case.

The lekage current and likage mismatch charge will be degrade the refer spur and jitter significantly. To mitigate above problems a self healing divided by prescaler andaselfhealing VCO are presented.

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CIRCUIT DESCRIPTION:

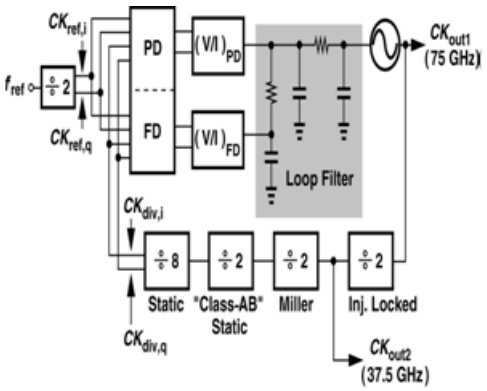
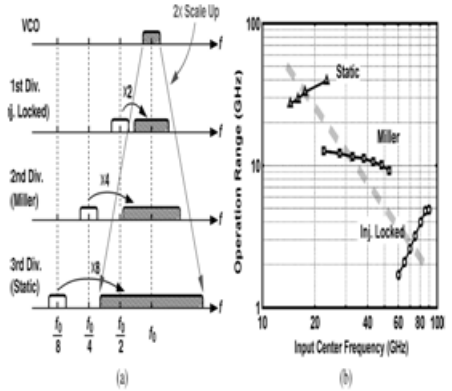


FIG:1 PLL ARCHITECTURE

The PLL circuit consists of a differential VCO a divider chain with total modulus of 64 a phase and frequency detector, and a third-order loop filter.The phase locking and frequency acquisition loops are decomposed to achieve low jitter and wide operation range simultaneously.The phase and frequency detector is implemented with SSB mixers and low-pass filters to suppress the reference feed through. An extra divider -by-2 circuit is incorporated to provide quadrature reference inputs. Similarto that in the frequency detector along with its V/I converter are automatically turned off upon lock to minimize the disturbance to the VCO. The loop filter is realized on chip to minimize the noise coupling through bonding wires. The 9-layer interconnectmetals in 90-nm process provide high density fringe capacitor2making the loop filter occupy only m To accommodate the severe tradeoffs between the input frequency and operation range, different types of dividers need To be employed here. Generally speaking, the injection-locked dividers achieve the highest operation frequency due to the narrowest locking the simplest structure, but usually with



Divider arrangement. (a) Locking range normalization with presumed 2 scale-up requirement. (b) Simulated locking ranges for each divider.

PROPOSED ARCHITECTURE PLL:

In that MOSTALYcomposed of a 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler. The division ratio is from 4 to 131. The parameters of this PLL are listed in

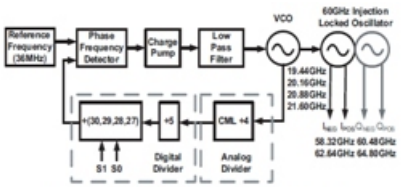


Fig. 1. The proposed 60GHz synthesizer architecture

Since the phase error of a PLL is highly dependent upon the current mismatch of a CP. The static phase error of a PFD is given as

$$\Delta\varnothing=\Delta icp.ton/icp$$

VCO gain	K_{VCO}	1.5GHz/V
Reference frequency	f_{ref}	15MHz
Charge pump current	I_P	200uA
Passive components	R	1800hm
	C_1	16.4nF
	C_2	1.3nF

where isICP the current IUP &IDN,TONdifference between the pull-up and pull-down currents, and , is the turn-on time of a PFD,ICP is the averaging current of the pull-up and pull-down currents. When this PLL locks, the LD is enabled to turn on the TDC and an encoder.

4-BIT CONTROLLER IN PLL:

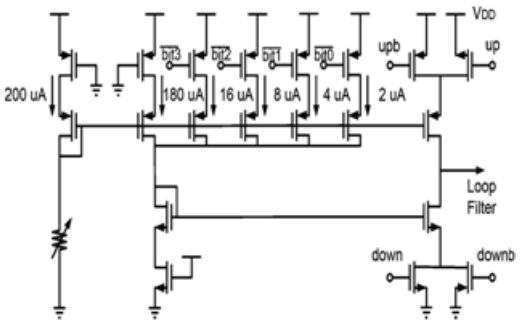


FIG:4-BIT CONTROLLER IN PLL

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A 4-bit TDC digitizes this static phase error to reflect the amount of the currentmismatching. Then, the digital code of this TDC is used to calibrate the charge pump.The simulated power of this TDC is 0.24 mW. Its timing resolution is 0.3 ns and the dynamic range is 4.8 ns.A 4-bit digitally-controlled CP is shown in fig4. The up current has a nominal value of 200 A and the down current.A digitally controlled within 180 and 210 A. The minimum current step is chosen as 2 A to relieve the worst-case current mismatch to 1% in this digitally-controlled CP.

The traditional replica-biased CP needs an operational amplifier which needs a high gain and its stability must be concerned. In addition, this operational amplifier may consume a static power. The CP calibration can be finished quickly due to this digital calibration.Once the calibration is completed, the digital code is fixed and the TDC is power-downed to save a power.

Self-healing System:

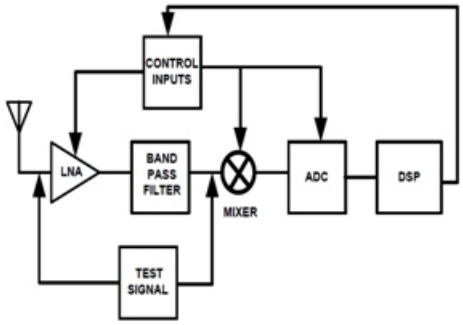


FIG:5SELF -HEALING SYSTEM

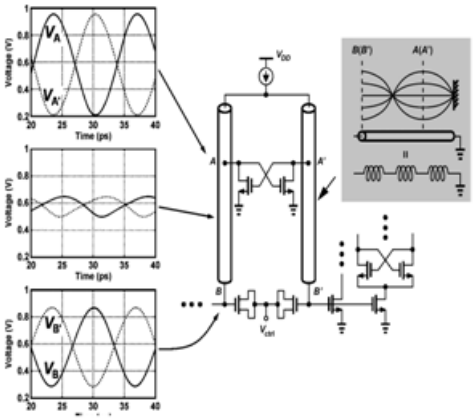
Healing goes beyond simple BIST by adding a layer of hardware and software intelligence to the system that enables autonomous calibration. The present work seeks to show case two wideband test signal source for on-die self healing of an 8-18 GHz (X to Ku band) receiver chain intended for use in radar applications. In order to exhibit healing, the second test signal source is integrated on die with a 6-20 GHz image-reject mixer. Automated IRR healing is performed on die as a demonstration of local block-level self-healing.

VCO:

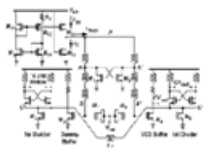
of whether the oscillating "tube" is indeed a transmission line.4Fig. 4(a) introduces a typical high-speed VCO design witha simple buffer , an injection locked divider (and a MOS varactor .

The circuit oscillates at a frequency such that the corresponding wavelength is 4 times as large as the equivalent length , leaving the ends (node and) as maximum swings. However, as the resonance frequency increases, the loading of the varactors, the buffers,and the dividers becomes significant as compared with that of the cross-coupled pair itself.

These indispensable capacitances burden the VCO substantially. Note that none of these devices can be made arbitrarily small: pair must provide sufficient negative resistance, transistor needs to inject large signal current, and has to provide enough frequencytuning.With the device dimension listed in Fig. 4(a), the circuit oscillates at only 46 GHz. Note that the device sizes haveapproached the required minimum and further shrinking maycause significant swing degradatio.



VECTOR FIRST STAGE:



The firsst two stages the freqency is brought down to below 20GHZ, allowing satic implementation on the sub seqent dividers, to extend theband width without using inductors we realize the 3-dividers stage as class-AB structure.The large in stantaneous currents creae high gain in the signal path and therefore high speed. beyond this point the divider design becomes much more relaxed.the succeeding stage are implemented as stand static dividers with the power and bandwidth optimized.

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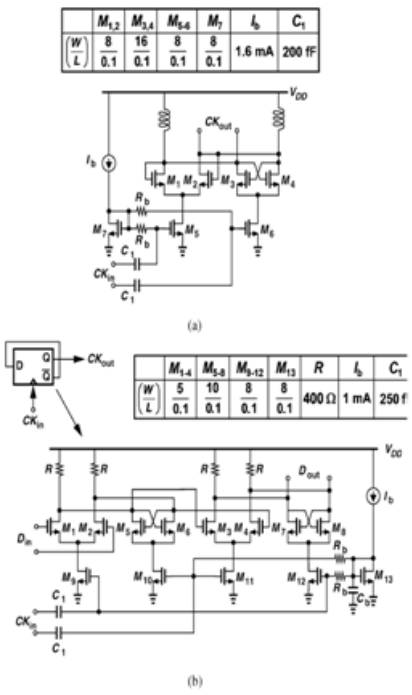
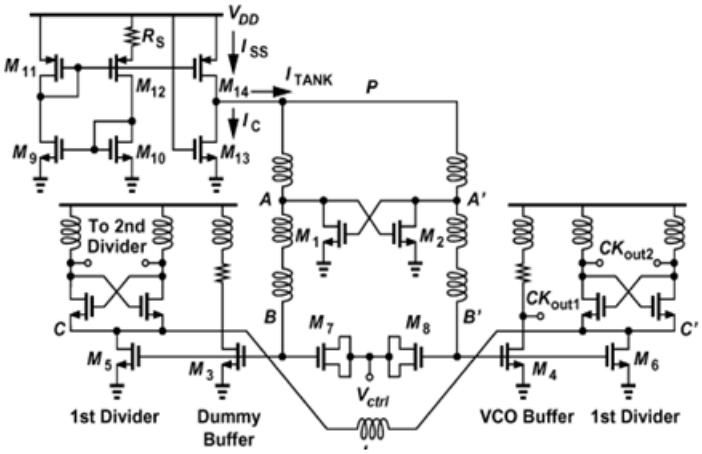
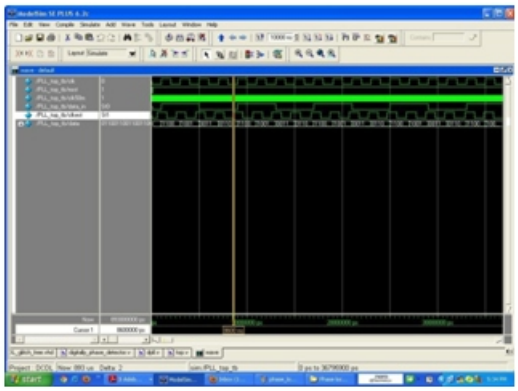


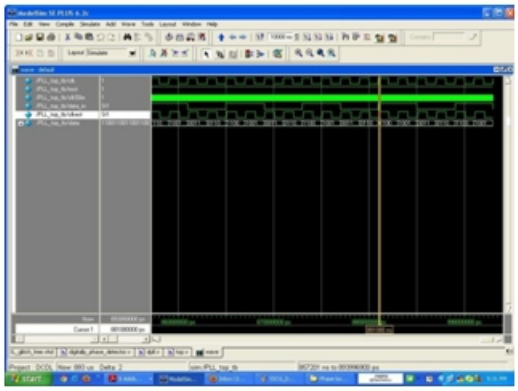
FIG(a):SECOND STAGE FIG(b):THIRD DIVIDER STAGE

Δ win represents the freqency difference between ckref and ck div.Obviously wether V1 is leading in log in v2 depends on the sign ofΔwin,and itcan be easily obtained by using a flip-flop output the VI converter designed to the freqency detection loop.Injects a positive or negative current to the loop fliter.This current is 3-times larger than the peack current of (V/I)PD to ensure a smooth freqency acquisition.

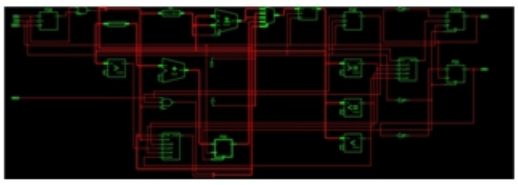


SIMMULATION:





Synthesis Results:



THE FIGURES ARE MEASURED THROUGH THE JITTER AT 855MHZ(a)WITHOUT AND (B)WITH THE SELF HEALING RESCALER/VCO AND TDC/ ENCODER:

To avoide the mal functionΔv1 leakage show be lower the throsld voltage vthrosld or the subseqent stage as Δvleakage<vthresholdThe lowest clock freqency of this "TSPCDEF" isFclock,low≥Ileakage/2.ctot.vthreshol For example Ileakage~400na at25c ctotal~15fF,and v throshld=0.6v the calculated lowest freqency is 2202MHz that the leakage current is propational to the tempeacture.When the tempeacture increases the lowest freqency is also incresases.The highest freqency of thTspis more than 10GHZ.measured specturm and jitter(a)120HZ and 100c and(b) then measured specturm and jitteer.

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Where Γ2=RMBZ.CH,RMBZ is the equivalent resistance of the transistor Mb2,and v2 is the initial volatage during the dischraging interval the voltages vbl changes from the voltage Vo~ov to the reference voltages Vsw assume Γ2<<Γ1,the required time trackisapproximated asTrack-~T1Ln(VDD/VDD-vsw) Then required capacitor CH~TRACK/ln(VDD/VDD-VSW).RMB1In this work the minimum freqency step Δfmin of this PLL is equal to the reference freqency fref Δ vctrl=Δfmin/kvco=fref/kvcoRequired time for this PLL to reachΔt=(c1+c2)/IP .ΔvctrlThe output is obtained by aself biased buffer.A common-mode dector can be used todetect the common-mode voltage.

<table>
<tr><td></td><td colspan="2">This work</td><td colspan="2">[5]</td><td colspan="2">[6]</td><td colspan="2">[9]</td><td colspan="2">[10]</td></tr>
<tr><td>CMOS</td><td colspan="2">65nm</td><td colspan="2">130nm</td><td colspan="2">130nm</td><td colspan="2">130nm</td><td colspan="2">65nm</td></tr>
<tr><td>Supply</td><td colspan="2">1.2V</td><td colspan="2">1V</td><td colspan="2">1.5V</td><td colspan="2">1V</td><td colspan="2">1.2V</td></tr>
<tr><td rowspan="2">Measured VCO frequency</td><td>w/o self-healing</td><td>w/i self-healing</td><td colspan="2" rowspan="2">10 ~ 700 MHz</td><td colspan="2" rowspan="2">30~650 MHz</td><td colspan="2" rowspan="2">200 ~ 950 MHz</td><td colspan="2" rowspan="2">470 ~ 1130 MHz</td></tr>
<tr><td>105 ~ 950MHz</td><td>60MHz ~ 1489MHz</td></tr>
<tr><td>Divider Ratio</td><td colspan="2">4 ~ 131</td><td colspan="2">N.A.</td><td colspan="2">1~4096</td><td colspan="2">4 ~ 160</td><td colspan="2">16 ~ 63</td></tr>
<tr><td rowspan="3">Jitter [ps]</td><td colspan="2">w/o calibration*</td><td colspan="10">w/o calibration</td></tr>
<tr><td>rms 43.62</td><td>pk-pk 284.4</td><td colspan="2" rowspan="2">N.A.</td><td colspan="2" rowspan="2">N.A.</td><td>rms 70.9</td><td>pk-pk 420</td><td colspan="2" rowspan="2">Does not lock</td></tr>
<tr><td colspan="2">@855MHz</td><td colspan="2">@640MHz</td></tr>
<tr><td rowspan="3">Jitter [ps]</td><td colspan="2">w/i calibration*</td><td colspan="10">w/i calibration</td></tr>
<tr><td>rms 8.03</td><td>pk-pk 55.6</td><td>rms 24.3</td><td>pk-pk 155</td><td>rms 4.9</td><td>pk-pk 44.6</td><td>rms 8</td><td>pk-pk 62.6</td><td>rms 5.13</td><td>pk-pk 46.2</td></tr>
<tr><td colspan="2">@855MHz</td><td colspan="2">@360MHz</td><td colspan="2">@240MHz</td><td colspan="2">@640MHz</td><td colspan="2">@800MHz</td></tr>
<tr><td>Ref. Spur</td><td>w/o calibration* -33.42dBc @855MHz</td><td>w/i calibration* -52.89dBc @855MHz</td><td colspan="2">N.A</td><td colspan="2">-35 dBc @240MHz</td><td colspan="2">N.A.</td><td colspan="2">N.A.</td></tr>
<tr><td>Area [mm²]</td><td colspan="2">0.0182**</td><td colspan="2">0.1681</td><td colspan="2">0.18</td><td colspan="2">0.063</td><td colspan="2">0.065</td></tr>
<tr><td>Power</td><td colspan="2">4.3@855MHz</td><td colspan="2">7@200MHz</td><td colspan="2">7@240MHz</td><td colspan="2">3@640MHz</td><td colspan="2">3.6@800MHz</td></tr>
</table>

EXPERMENTAL RESULTS:

This chip fabricated in a 65-nm cmos cmos technology. The active area occupies 0.0182mm external capacitors are adopted in the loop filter for this work.

CONCLUSION:

A wide-range PLL is fabricated in a 65-nm cmos process.To deal with the process variability and lekage current in nanoscale cmos process.A self-healing prescaler a self-healing,VCO, and a calibratedCP are presented experimental results are given to demonstrate the the feasibility.

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