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An Efficient SOC approach to Design CRT controller on CPLD's

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Abstract:

The design of CRT controller is studied, which is applied in the Speech Interactive System based on ASIC.CRT controller based on CPLD is presented. MCU flexible read and write to RAM with CPLD. Meanwhile, the simulation is also given based on Maxplus. The simulating results prove that the design can reach the demand of real time exchanging, and has integrality, reliability and good applications in the Speech Interactive System.

I.INTRODUCTION:

The main function is to form the address code of character buffer and attribute memory, and generate horizontal scanning, vertical scanning synchronization signal to the video control logic. Due to the complexity of co-ordination with the microcontroller and memory RAM, its peripheral circuits is so large and lack of flexibility. On the one hand, the design of CRT controller based on CPLD, can improve the integration and reliability of the system; on the other hand, it can significantly enhance design flexibility, especially refresh the entire screen to less than one second in line with SCM and through control of the memory RAM read and write, which is the Motorola 6845 cannot be achieved and is an important innovation of this design.

CATHODE RAY TUBE:

This is the part of the oscilloscope that displays the input signal as a trace. By this stage, most of the work has already been done by the vertical and horizontal circuitry stages. The display circuitry is essentially the Cathode Ray Tube (CRT) and the graticule, which is the calibration marking.

The CRT section consists of an electron gun, vertical and horizontal deflection plates, and the coating that produce the visual colors. The CRT's electron gun produces a stream of electrons. These are accelerated to the front end of the tube and on the way focused into a narrow electron beam. The vertical and horizontal plates, mentioned earlier, deflect this narrow beam of electrons to a particular orientation. This forms the shape of the input signal. The display end of the tube has a coating which when struck by this electron beam emits a particular colour (usually green). This is the trace, which appears on the display end of the tube.

CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs).

COLOR CRT DISPLAY:

Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see illustration). Electron beams emanate from "electron guns" which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid". The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes.

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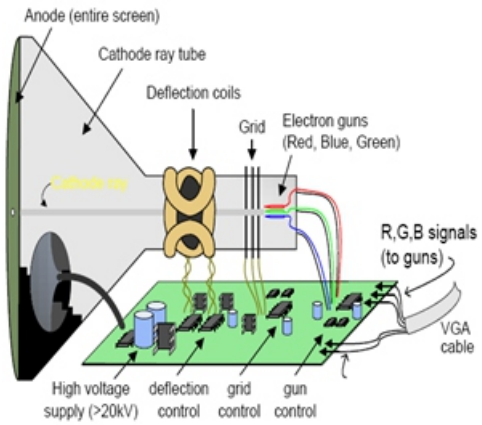

figure.1: cathode ray tube

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

Display surface:

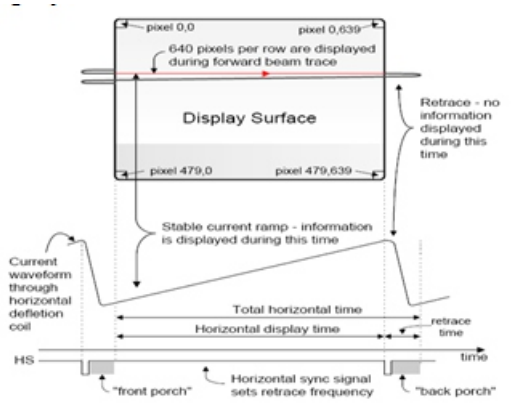

Figure 2: display surface

Information is only displayed when the beam is moving in the "forward" direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display.

Much of the potential display time is therefore lost in "blanking" periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution.

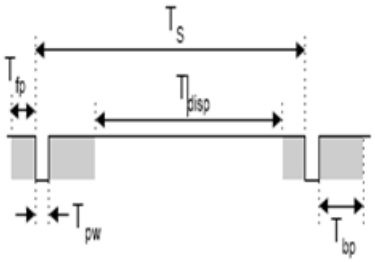

Figure 3: resolution of display

Video data typically comes from a video refresh memory; with one or more bytes assigned to each pixel location (the Nexys3 uses three bits per pixel).

The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information.

The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range.

The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in the table at right can be derived.

Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.

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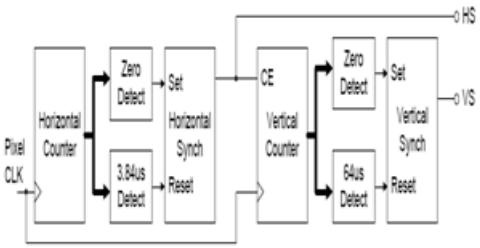

Figure 4: VGA controller

II.ANALOG TO DIGITAL CONVERTER:

The ADC used is the 8bit Flash ADC0820, from National Semiconductor. The timing diagrams of the ADC. I then wire up the ADC to see that it functions. First a brief description of how the ADC works.

Starting from the left we have an adjustable attenuator. This module scales the input signal, down or up, to the input sensitivity of the ADC. The user selects the scaling factor. This block should have high impedance in order to minimize the loading of the circuit from which the input signal is being measured.

This input impedance should also be compatible with the electrical characteristics of standard scope probes. Next we have the ADC. This module is responsible for the conversion of the analogue input signal to its digital form, for further processing.

The conversion rate should be as fast as possible as it has a direct bearing on the bandwidth of the scope. A faster conversion rate implies a faster sampling time, and thus a higher range of frequencies that can be measured.

The trigger controller is responsible for the selection of the triggering modes of the oscilloscope. The user sets the trigger mode and level. This should be designed with high impedance to minimize loading.

III.CPLD CONTROLLER:

The CPLD controller is the brain of the whole system. Essentially it implements the 2-process architecture mentioned earlier. The software that describes this controller will be described in detail in the later chapters. For now it is enough to know that this module is responsible for:

- The controlling of the ADC;
- Controlling the sampling rate.
- Starting a sampling frame in response to a trigger signal.
- The transformation of input digital data from ADC, to a form that can be displayed on a VGA monitor;
- The controlling of the VGA monitor.

The configuring processor configures the CPLD at start up. This could be a configuring ROM, especially made for this function, or a simple microprocessor. Finally, the interface electronics simply provides the appropriate signal levels for the VGA monitor control lines. The Memory module of the CPLD system.

General description of Memory module:

Memory is a passive system, in that it is completely controlled by processes external to it. It is also a relatively simple module. Figure 8.1 shows a complete breakdown of Memory.

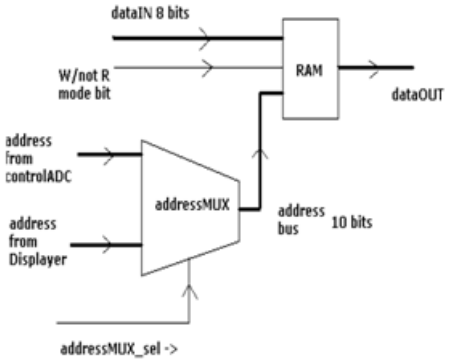

Figure 5: design of memory module.

The Displayer module of the CPLD system:

This module describes the functionality of the Displayer module. This module takes care of the visuals of the oscilloscope.

Description of VGA monitor:

The VGA monitor was explained earlier in more detailed. It is now enough to say that it consists of a 480 x 640 matrix of pixels; RGB data

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is sent serially to the monitor; and that control is accomplished by setting the VSYNC and HSYNC signals at the appropriate times.

General description of Displayer module:

Displayer is responsible for conditioning the value of the data sample stored in memory, in order for it to be displayed on a VGA monitor. It then goes on to display the trace stored in memory. Displayer runs continuously. Figure summarizes the Displayer module.

IV.SYSTEM DESIGN:

The Working Principle and design parameters of a CRT Display:

CRT display use lum signal to control the electron gun eradiating electrons, use two scan signals to control the electrons shooting the given dot of the screen, so that a picture forms. The CRT monitor is composed of five parts, which are electron gun, defection coil, shadow mask, the phosphor layer and scanning circuit.

Raster scan can be used by the electron beam, which scans point from the top left of the screen, point by point to the right, then form a horizontal line; to reach the far right, back to the next horizontal line of the left, repeat the above procedure. When the electron beam scans the lower right corner point of scanning, the frame is formed. Since then, the electron beam back to the top left of the starting point begin the next frame scan. In this way the images and texts are displayed on the monitor.

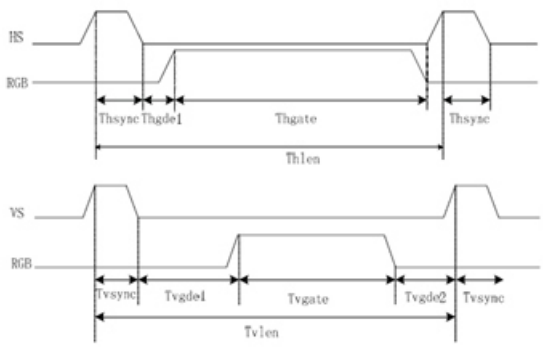

Figure 6: Horizontal and vertical scan timing schematic

System Structure:

Microcontroller indexes the character dot matrix of the text information (character code) which will be displayed in the Chinese character dot matrix library ROM (29C040), when then horizontal and vertical signals retrace period, and extracts 32 bytes of Chinese character dot matrix data, then deposit them in the 32K display buffer RAM (62256). 2. The CPLD produces the line synchronization, frame synchronization signal at speed of 72Hz field frequency and 31KHz line frequency, at the same time generates the address code and read the dot matrix bytes in the display buffer RAM, then sends into the shift register and shifts out to the video control logic to form the output signal of the display.

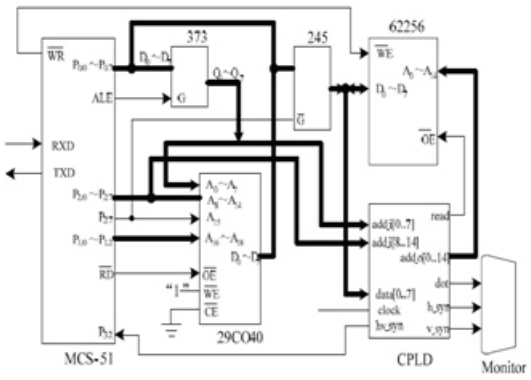

Figure 7: the structure of CRT controller based on CPLD

In the video viewing area, the CPLD reads RAM memory for dot matrix display, while generating inverting field signal hv_syn is high, so that the microcontroller stops write character dot-matrix information to the memory. When the hv_syn signal is low at the inverting blanking field, the CPLD will output the address switch to the address bus of the microcontroller. The microcontroller opens the tri-state data bus 245 by movx instruction and the A15=0, to write dot matrix Chinese character to the memory RAM, in order to avoid the conflict of memory read and write data.

Memory ROM, according to Chinese character code from small to large in turn stores the primary and secondary Chinese character dot matrix. Because the character dot matrix is16×16, so each character takes up 32 bytes. For each Chinese character, to retrieve the corresponding 32 bytes dot-matrix information and then write to the display buffer RAM.

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The way of character dot-matrix datum stored in RAM, is called "screen memory-mapped", which is each pixel on the screen corresponds to a RAM storage unit. Because CRT controller display line by line on the screen, so 32 bytes written to memory is to increase every two byte address 50H, then the pointer to the next line at the same colum.

V.RESULTS:

Simulation result of cathode ray tube:

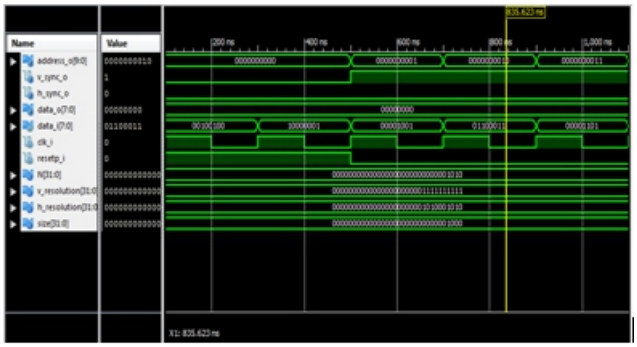

Figure 8: simulation result of cathode ray tube

TIMING REPORT:

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Timing Summary:
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Speed Grade: -3

   Minimum period: 3.642ns (Maximum Frequency: 274.608MHz)
   Minimum input arrival time before clock: 3.692ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found
```

Figure 9: timing report of cathode ray tube

RTL SCHEMATIC:

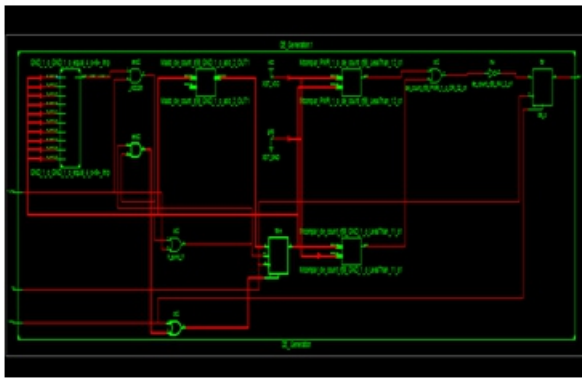

Figure 10: RTL schematic of cathode ray tube

DEVICE UTILIZATION REPORT:

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Device utilization summary:
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Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:                11  out of  18224      0%
 Number of Slice LUTs:                     29  out of   9112      0%
    Number used as Logic:                  29  out of   9112      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:       29
   Number with an unused Flip Flop:        18  out of     29     62%
   Number with an unused LUT:               0  out of     29      0%
   Number of fully used LUT-FF pairs:      11  out of     29     37%
   Number of unique control sets:           1

IO Utilization:
 Number of IOs:                            4
 Number of bonded IOBs:                    4  out of    232      1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                 1  out of     16      6%
```

Figure 11: device utilization report of cathode ray tube

VI.CONCLUSION:

According to the working principle and technical indicators of the display, combined with design requirements, the paper puts forward system parameters about text display to achieve a CRT controller based on CPLD, which is achieved by simulating and testing. The design of CRT controller based on EDA, which is applied to the digital speech terminals, not only reduces the complexity of the digital electronic system, but also significantly enhances the flexibility of design, system integration and reliability. Which is also once again confirmed Electronic Design Automation (EDA) technology has infiltrated into the electronic system and ASIC design chain, the software has been applied to a variety of electronic design and simulation, the circuit design, adjustment and improvement are more efficient and convenient.

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