ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Simulation of Three-Phase Multilevel Inverter with Few Numbers of Components for Industrial Application

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Abstract

Multilevel inverters have more advantages in comparison with the traditional two-level inverter, which consist of better harmonic performance, lower semiconductor voltage stress, low-electromagnetic interference and lower switching losses. For high-voltage applications, the CHB topology is very suitable since this structure needs few number of power electronic components than other classic topologies. The CHB topology consists of several H-bridges and dc sources. This topology is implemented to three-phase system. In the symmetric structure, the values of the dc voltage sources are same. However, in asymmetric topology the magnitudes of the dc voltage sources are unequal. Asymmetric CHB topology generates a large number of levels for the same number of components in comparison with symmetric topology for the same number of power electronic components. For asymmetric inverters, a new structure has been recommended in, which reduces the number of switches and dc voltage sources compared with the CHB inverter. However, for creating a large number of output. Multilevel inverters with more number of levels can produce high quality voltage waveforms. In this concept three-phase is used instead of single-phase and implemented for nineteen levels, which can generate a large number of levels with reduced number of IGBTs, gate driver circuits and diodes. A comparison is presented between proposed multilevel inverter and conventional cascade topology. The proposed topology is implemented with MATLAB/SIMULAITON software and the simulation results are analyzed.

*Keywords--**Induction Motor, Multi-Level Inverter, Total Harmonic Distortion (THD), switching losses.***

I. INTRODUCTION

In recent era, the multilevel inverter is state of art power conversion system for high voltage and high power quality applications. The two-level inverter with existing semiconductor technology may not suit for high voltage application which may increase the high voltage stress on switch, high Electro Magnetic Interference (EMI) and poor power quality output [1], [2]. In order to solve these issues the conventional multilevel inverters are introduced, but it may require high number of power semiconductor devices. So, the researchers are developing new multilevel inverter topologies with existing semiconductor technology to meet require high power quality with reduced power semiconductor devices [3]. Because of these advantages multilevel converters are more attractive in high power applications.

The conventional multilevel inverter topologies are (i) Neutral Point Clamped (NPC) (ii) Flying Capacitor (FC) and (iii) Cascaded H-Bridge (CHB). These converters provide better output quality by increasing smaller voltage level; they are applied for commercial applications and industrial applications like AC Drives and FACTS Devices [4]. Theoretically, these topologies are capable of generating infinite number of equal stepped voltage level. Whereas, practically, the number of level increases as it requires more number of power switches, clamping diode, flying capacitor and associated components respectively. Furthermore, this may increase the installation area, cost of the

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International Journal & Magazine of Engineering, Technology, Management and Research
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converter and complex control circuits. In last few decades several authors were finding solution by introducing novel multilevel inverter topologies with reduction of power switches [5]-[8]. In symmetrical method all the dc sources voltage have unique value and it ensures good modularity. Different rating of switches are required in asymmetrical method due to different dc sources voltage magnitude, this may generate high number of output voltage with minimum dc source. But multilevel inverter modularity may reduce. An Attempt has been made in [9] to propose a new multilevel inverter topology with reduced power switches.

The outputs of dc–ac converters contain common-mode voltage switched at high frequencies with voltage magnitudes that are comparable to the inverter pole voltages. High frequency switching of the common-mode voltage in the induction motor causes several issues like leakage currents through the stray capacitance between the winding and the body of the motor and create shaft voltages causing bearing currents resulting in bearing failures of the motors[3] – [6]. The effects of common-mode voltage are much more adverse in the case of medium- and high-voltage drives due to high frequency switching of common-mode voltage in the order of few kilovolts. High dV /dt switching in common-mode voltage causes breakdown of bearing lubricant insulation and causes pitting in the bearing surfaces. This leads to quick failure of bearings

II. PROPOSED SYMMETRIC MULTILEVEL INVERTER

The basic unit for the proposed symmetric multilevel inverter is shown in Fig.1. In this circuit, when the switch Sis turned off, the current flows from the diode, but when the switch Sis turned on, the diode is reverse biased and the current flows from dc voltage source (V) which is connected in series with switches. Hence, using this method the output voltage is controlled. This method is the base of the proposed multilevel inverter. This basic circuit can generate five levels in output voltage and Table 1 gives the values of output voltages (VO) for different states of S, T1, andT4 switches. Fig.2 shows the extended proposed basic circuit. The magnitudes of the dc voltage sources are equal. Therefore this structure is called symmetric multilevel inverter, which consists of a symmetric basic unit and a full-bridge converter. Table2 gives the values of output voltages (VO) for different states ofS1, S2, Sn, T1, and T4 switches. Note that there are several different switching patterns for generating the zero level, and in Table2, only one of them is shown

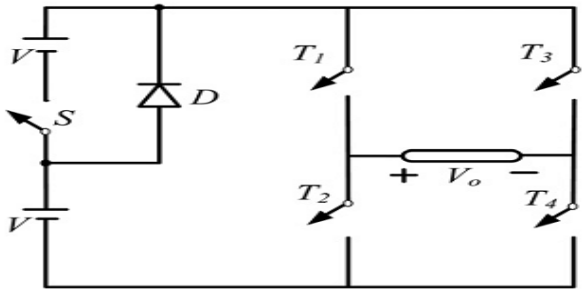

Fig.1.Basic Circuit of the Proposed Multilevel Inverter.

Table I ON Switches Look-Up Table for Basic Circuit of the Proposed Multilevel Inverter

State	Switches states					Output voltage
	S	T_1	T_2	T_3	T_4	
1	0	1	0	1	0	0
2	0	1	0	0	1	V
3	0	0	1	1	0	−V
4	1	1	0	0	1	2V
5	1	0	1	1	0	−2V

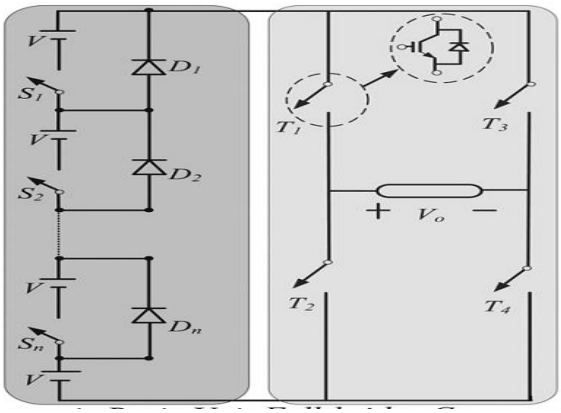

Fig.2.Proposed Symmetric Multilevel Inverter Topology

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International Journal & Magazine of Engineering, Technology, Management and Research
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Table II Switches States for Symmetric Topology

State	Switches states								Output voltage
	S_1	S_2	...	S_n	T_1	T_2	T_3	T_4	
1	0	0	...	0	1	0	1	0	0
2	0	0	...	0	1	0	0	1	V
3	0	0	...	0	0	1	1	0	–V
4	1	0	...	0	1	0	0	1	2V
5	1	0	...	0	0	1	1	0	–2V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2n+2	1	1	...	1	1	0	0	1	(n+1)V
2n+3	1	1	...	1	0	1	1	0	–(n+1)V

The number of output voltage levels and the total number of switches in the recommended symmetric multilevel inverter are obtained as follows, respectively

$$N_{\text{level}} = 2n + 3 \quad (1)$$

$$N_{\text{IGBT}} = n + 4 \quad (2)$$

Where represents the number of IGBTs in the symmetric basic unit structure. In this topology, the maximum output voltage (VO, max) is

$$V_{\text{o, max}} = (n + 1) \times V \quad (3)$$

Using (1) and (2), we have

$$N_{\text{level}} = 2N_{\text{IGBT}} - 5 \quad (4)$$

Fig.3.acompares the number of IGBTs against the number of output voltage levels in the proposed symmetric topology

III. PROPOSED ASYMMETRIC MULTILEVEL INVERTER

An asymmetric multilevel inverter structure can provide an increased number of voltage levels for the same number of power electronic devices than its symmetric counterpart. Fig.4 shows the structure of the proposed asymmetric inverter, which consists of an asymmetric basic unit and a full-bridge inverter. Table3shows the ON switches look-up table for the proposed asymmetric structure. For the proposed asymmetric structure, the dc voltage sources values are suggested to be chosen according to the

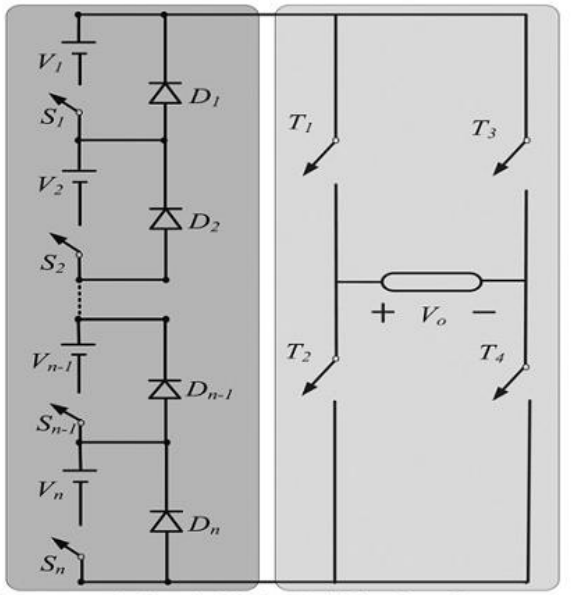

Fig.4 Proposed Asymmetric Multilevel Inverter Topology Following Algorithm.

$$V_1 = V \quad (5)$$

$$V_j = 2^{(j-1)} \times V \quad \text{for} \quad j = 2, 3, \ldots, n \quad (6)$$

In this method, the number of levels and maximum output voltage are given by (7) and (8), respectively

$$N_{\text{level}} = 2^{(n+1)} - 1 \quad (7)$$

$$V_{\text{o, max}} = \left(2^{n-1}\right) \times V \quad (8)$$

Where represents the number of IGBTs in the asymmetric basic unit. In the proposed asymmetric topology, the number of IGBTs can be determined by the following equation where represents the number of IGBTs in the asymmetric basic unit. In the proposed asymmetric topology, the number of IGBTs can be determined by the following equation

$$N_{\text{IGBT}} = n + 4 \quad (9)$$

From (7) and (9), it is clear that

$$N_{\text{level}} = 2^{(N_{\text{IGBT}}-3)} - 1 \quad (10)$$

the comparison between the proposed asymmetric multilevel inverter with binary and trinary configurations of CHB topology and those proposed in [13, 14] in terms of the number of IGBTs. This comparison shows that the proposed asymmetric

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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inverter can produce the maximum number of levels with minimum power electronic IGBTs. Therefore this topology reduces the cost and control complexity and tends to reduce the overall reliability and efficiency in comparison with other topologies. In [13, 14], each bidirectional and unidirectional switch needs one gate driver circuit. The gate driver circuits are the electronic part of the circuit and increasing the number of gate driver circuits is a considerable deficiency since increasing the gate driver's causes increasing costs and control complexity. However, all the switches in the proposed asymmetric topology are unidirectional and the number of IGBTs and gate driver circuits are the same. Gate driver circuits against the number of levels in the proposed asymmetric topology.

IV. INDUCTION MOTOR

In recent years the control of high performance induction motor drives for general industry applications and production automation has received widespread research interests. Induction machine modeling has continuously attracted the attention of researchers not only because such machines are made and used in largest numbers but also due to their varied modes of operation both under steady and dynamic states. Traditionally, DC motors were the work horses for the Adjustable Speed Drives (ASDs) due to their excellent speed and torque response. But, they have the inherent disadvantage of commutator and mechanical brushes, which undergo wear and tear with the passage of time. In most cases, AC motors are preferred to DC motors, in particular, an induction motor due to its low cost, low maintenance, lower weight, higher efficiency, improved ruggedness and reliability. All these features make the use of induction motors a mandatory in many areas of industrial applications. The advancement in Power electronics and semiconductor technology has triggered the development of high power and high speed semiconductor devices in order to achieve a smooth, continuous and low total harmonics distortion (THD).Three phase induction motors are commonly used in many industries and they have three phase stator and rotor windings. The stator windings are supplied with balanced three phase ac voltages, which produce induced voltages in the rotor windings due to transformer action. It is possible to arrange the distribution of stator windings so that there is an effect of multiple poles, producing several cycles of magneto motive force (mmf) around the air gap. This field establishes a spatially distributed sinusoidal flux density in the air gap. In this paper single phase induction motor as a load. The equivalent circuit for one phase of the rotor is shown in figure.5.

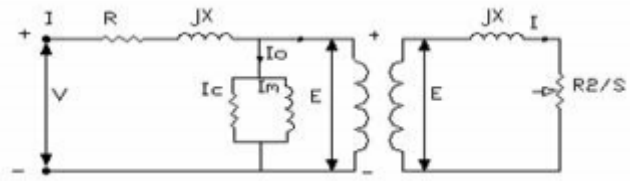

Fig.5. Steady state Equivalent circuit of an induction Motor.

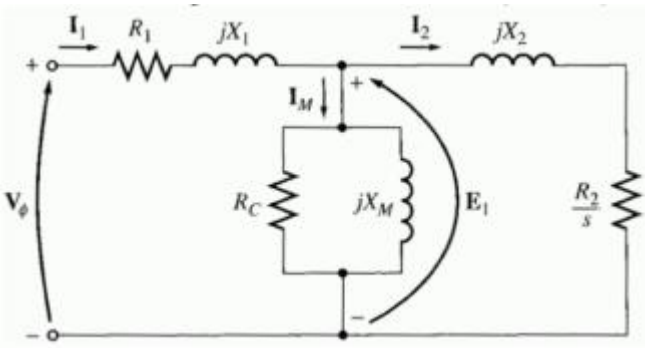

Fig.6. Equivalent Circuit Refer To Stator.

The rotor current is

$$I_r = \frac{sE_r}{R_r + jX_r}$$

$$= \frac{E_r}{\frac{R_r}{s} + jX}$$

The complete circuit model with all parameters referred to the stator is in figure. Where Rs and Xs are the per phase resistance and leakage reactance of the stator winding. Xm represents the magnetizing reactance. R'r and X'r are the rotor resistance and reactance referred to the stator. I'r is the rotor current referred to the stator. There will be stator core loss,

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

when the supply is connected and the rotor core loss depends on the slip.

V.MATLAB/SIMULINK RESULTS

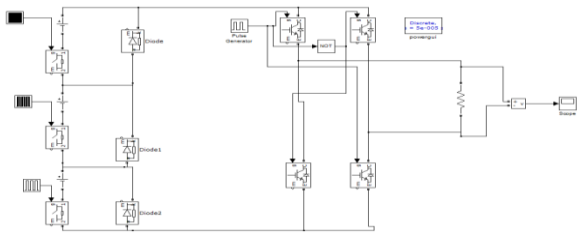

Fig.7.Matlab/Simulink Model of Fifteen-Level Asymmetric Multilevel Inverter.

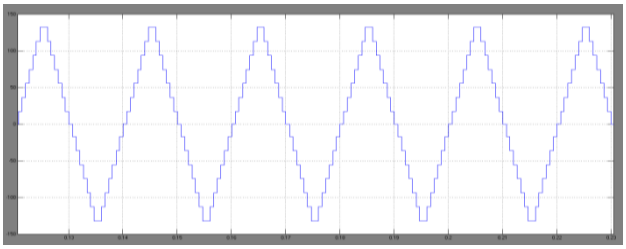

Fig.8.Fifteen Level Asymmetric Multi Level Inverter Output Voltage.

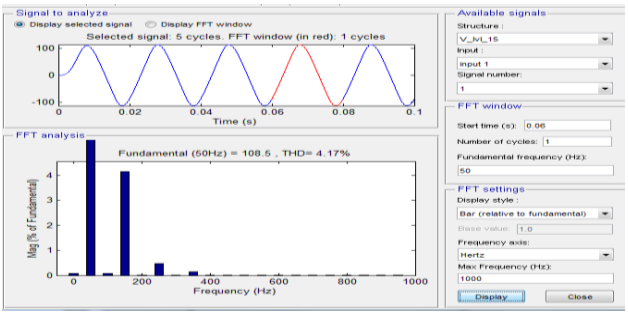

Fig.9.FFT Analysis of Fifteen Level Inverter Voltage for single phase 15 levels.

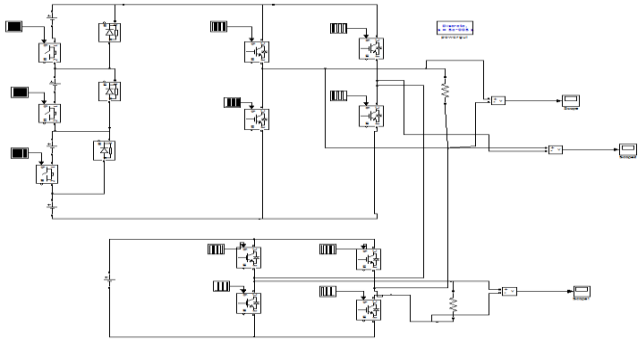

Fig. 10. Matlab/Simulink Model Of Nineteen-Level Based On Symmetric Topology.

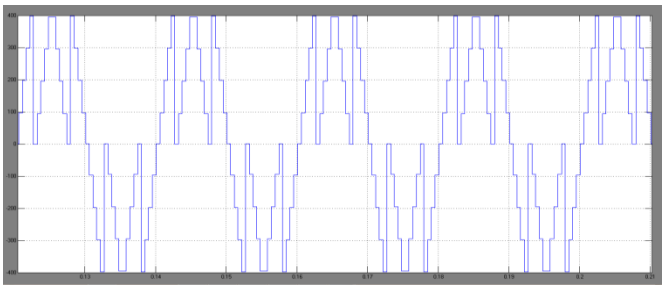

Fig.11. Output Voltage on V01.

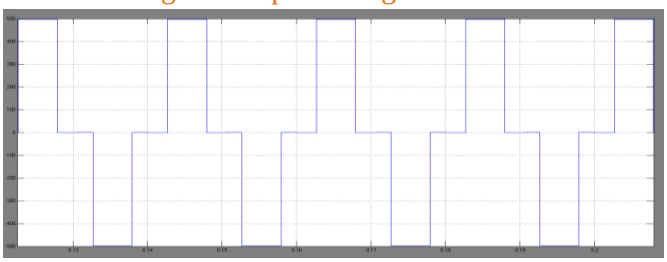

Fig.12.Output Voltage on V02.

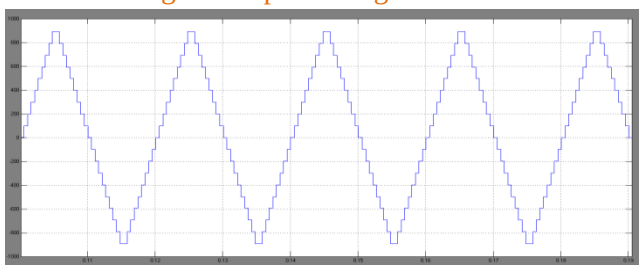

Fig.13. Nineteen-Level Hybrid Inverter output voltage.

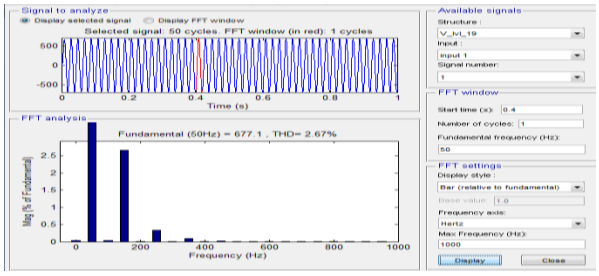

Fig.14.FFT Analysis of Output Voltage single phase 19 levels.

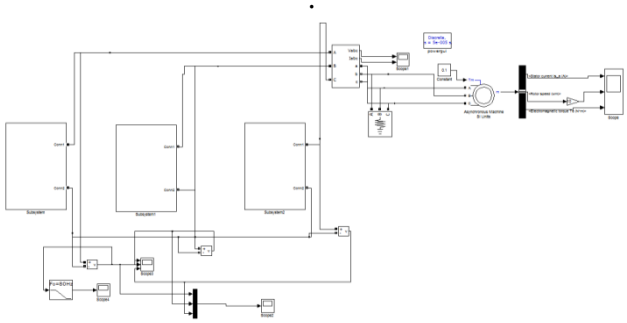

Fig.15.Nineteen-Level Based on Symmetric Topology with Induction Motor.

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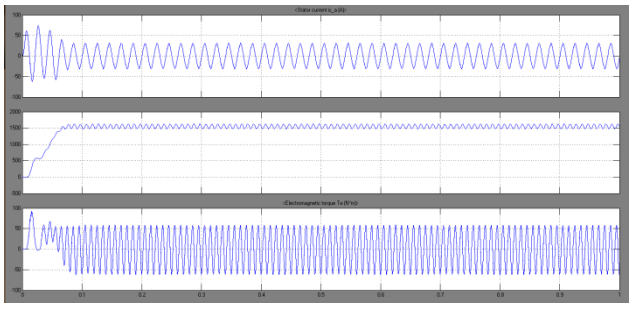

Fig.16.Current, Speed and Torque for Induction Motor.

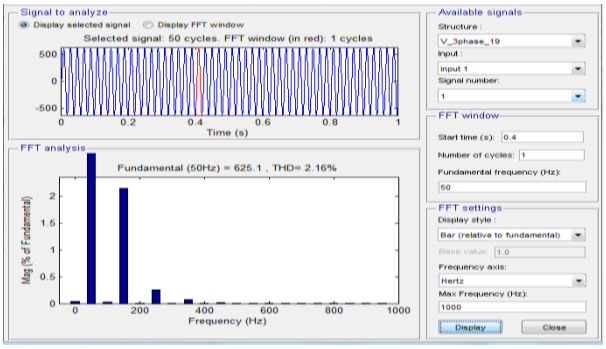

Fig.17.FFT Analysis of Output Voltage three phase 19 levels

VI.CONCLUSION

In this paper, new symmetric and asymmetric multilevel inverter structures have been recommended, firstly. The proposed concept is extended with three phase configuration for 19 levels and also the converter output is implemented to induction motor drive.The comparison between the recommended symmetric and asymmetric topologies with other topologies has been presented considering several factors. It was shown that the proposed topologies need few numbers of IGBTs and gate drivers. These factors reduce the installation area, circuit size and cost. It was shown that the value of the blocked voltage by the switches of the proposed asymmetric structure is less than the other asymmetric structures.

The simulation and experimental results for a 15-level asymmetric inverter and a 19-level. Multilevel inverter is very useful in high power and power quality application. Modulation method are getting trend on multilevel inverter for better performance. When this topology is applied on induction motor its performance gets increase compared to conventional inverter. Torque pulsation get reduced and motor run smoothly

REFERENCES

1) Tranquillo, L.G., Rodriguez, J, Leon, J.I., Koura, S., Portillo, R., Prats, M.M.:'The age of multilevel converters arrives', IEEE Trans. Ind. Electron., 2008, 2, (2), pp. 28–39

2) Barkati, S., Baghli, L., Berkouk, E.L.M., Boucherit, M.S.:'Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms', Electr. Power Syst. Res., 2008, 10, (78), pp. 1736–1746

3) Marquardt, R., Legnica, A.:'A new modular voltage source inverter topology'. Proc. EPE'03, Toulouse, France, 2003, pp. 1–10

4) Legnica, A., Marquardt, R.: 'An innovative modular multilevel converter topology suitable for a wide power range'. IEEE Power Tech. Conf. Proc., Bologna, 2003

5) Xiaoping, Y., Barbi, I.: 'Fundamentals of a new diode clamping multilevel inverter', IEEE Trans. Power Electron., 2000, 4, (15), pp. 711–718

6) Abdul Kadir, M.N., Mekhilef, S., Ping, H.W.:'Dual vector control strategy for a three -stage hybrid cascaded multilevel inverter', J. Power Electron., 2010, 2, (10), pp. 155–164

7) Hunag, J., Corzine, K.: 'Extended operation of flying capacitor multilevel inverters', IEEE Trans. Power Electron., 2006, 1, (21), pp. 140–147

8) Feng, C., Liang, J., Agelidis, V.G.: 'Modified phase-shifted PWM control forflying capacitor multilevel converters', IEEE Trans. Power Electron., 2007, 1, (22), pp. 178–185

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

9) Gupta, K.K., Jain, S.:'A multilevel voltage source inverter (VSI) to maximize the number of levels in output waveform', Elsevier J. Electr. Power Energy Sys. 2012, 1, (44), pp. 25–36

10) Lai, Y.S., Shyu, F.S.:'Topology for hybrid multilevel inverter', IEE Proc. Electro. Power Appl., 2002, 149, (6), pp. 449–458

11) Banaei, M.R., Dehghanzadeh, A.R., Salary, E., Khounjahan, H., Alizadeh, R. :'Z-source-based multilevel inverter with reduction of switches', IET Power Electron., 2012, 3, (5), pp. 385–392

12) Kangarlu, M.F., Babaei, E., Laali, S.:'Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources', IET Power Electron., 2012, 5, (5), pp. 571–581

13) Babaei, E., Hussein, S.H., Gharehpetian, G.B., Tarafdar Haque, M., Sabah, M.: 'Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology', Elsevier J. Electr. Power Syst. Res., 2007, 77, (8), pp. 1073–1085

14) Babaei, E.: 'A cascade multilevel converter topology with reduced number of switches', IEEE Trans. Power Electron., 2008, 23, (6), pp. 2657–2664

15) Rotella, M., Penailillo, G., Pereda, J., Dixon, J. :'PWM method to eliminate power sources in a non-redundant 27-level inverter for machine drive applications', IEEE Trans. Ind. Electron., 2009, 1, (56), pp. 194–201.