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Closed Loop Control of a High Voltage Gain DC–DC Converter Integrating Coupled-Inductor

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Abstract:

In recent high step up dc-dc converter based on integrating coupled inductor and switched capacitor techniques for renewable energy application is proposed in. The output is verified for both open loop and closed loop control strategies. The converter consists of a coupled inductor and two voltage multiplier cells, in order to obtain a high voltage gain. The capacitors which are charged using the energy stored in the coupled inductor increases the voltage transfer gain. The proposed converter achieves extremely large voltage conversion ratio with appropriate duty cycle and reduction of voltage stress on the power devices. These characteristics make it possible to design a compact circuit with high static gain and high efficiency for industry applications. This paper proposes a new converter strategy with closed loop control action, with the help of closed loop system attains low steady state error value and system operates in high stability factor for autonomous. Overall performance of the renewable energy system is then affected by the efficiency of step-up DC/DC converters, which are the key parts in the system power chain. The results are obtained through Matlab/ Simulink software package.

Index Terms:

Coupled Inductor, Closed Loop Controller, PI Controller, Step-up, Diode-Capacitor.

I.INTRODUCTION:

This paper presents a novel high step up dc-dc converter renewable energy applications. The proposed circuit consists of a coupled inductor and two voltage multiplier cells in order to obtain high voltage step up .In addition a capacitor is charged using the energy stored in the coupled inductor, which increases the voltage transfer gain. The energy used in the leakage inductance is recycled with the use of active clamp circuit. In this proposed topology the voltage stress across the switch is reduced. Therefore a main power switch with low resistance RDC (on) can be used to reduce the conduction losses. Comparison of the proposed converter with open loop and closed loop control is presented. The closed loop control is achieved by using Proportional Integral (PI) controller. First, a literature survey is carried out which necessitates the need for a new topology. Theoretically, conventional step-up converters, such as the boost converter and flyback converter, cannot achieve a high step-up conversion with high efficiency because of the resistances of elements or leakage inductance; also, the voltage stresses are large. Thus, in recent years, many novel high step up converters have been developed [6]–[8]. Despite these advances, high step-up single-switch converters are unsuitable to operate at heavy load given a large input current ripple, which increases conduction losses. The conventional boost converter is an excellent candidate for high-power applications and power factor correction. Unfortunately, the step-up gain is limited, and the voltage stresses on semiconductor components are equal to output voltage.

Hence, based on the aforementioned considerations, modifying a conventional boost converter for high step-up and High-power application is a suitable approach. To integrate switched capacitors into an boost converter may make voltage gain reduplicate, but no employment of coupled inductors causes the step-up voltage gain to be limited [9], [10]. Oppositely, to integrate only coupled inductors into a boost converter may make voltage gain higher and adjustable, but no employment of switched capacitors causes the step-up voltage gain to be ordinary. Thus, the synchronous employment of coupled inductors and switched capacitors is a better concept; moreover, high step-up gain, high efficiency, and low voltage stress are achieved even for high-power applications [11].

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Many boost converters based on a coupled inductor or tapped inductor provide solutions to achieve a high voltage gain, and low voltage stress on the active switch without the penalty of high duty ratio. However, the input current is not continuous. Particularly, as the turn ratio of the coupled inductor or tapped inductor is increased to extend the voltage conversion ratio, the input current ripple becomes larger. Thereby, an input filter is inserted into a coupled-inductor boost converter. In order to satisfy the extremely high step-up applications and low input current ripple, a cascaded high step-up converter with an individual input inductor was proposed.In this paper, a novel single switch dc–dc converter with high voltage gain is presented. The features of the proposed converter are as follows:

1) the voltage gain is efficiently increased by a coupled inductor and the secondary winding of the coupled inductor is inserted into a diode-capacitor for further extending the voltage gain dramatically;
2) a passive clamped circuit is connected to the primary winding of the coupled inductor to clamp the voltage across the active switch to lower voltage level. As a result, the power devices with low voltage rating and low on-state resistance RDS (ON) can be selected. On the other hand, this diode–capacitor circuit is useful to increase voltage conversion ratio;
3) the leakage inductance energy of coupled inductor can be recycled, improving the efficiency; and 4) the potential resonance between the leakage inductance and the junction capacitor of output diode may be cancelled [13].

II.OPERATING PRINCIPLES OF THE PROPOSED CONVERTER:

Fig. 1(a) shows the circuit structure of the proposed converter, which consists of an active switch Q, an input inductor L1 and a coupled inductor T1, diodes D1, D2, and DO, a storage energy capacitor C1 and a output capacitor CO, a clamped circuit including diode D3 and capacitor C2, an extended voltage doubler cell comprising regeneration diode Dr and capacitor C3, and the secondary side of the coupled inductor. The simplified equivalent circuit of the proposed converter is shown in Fig. 1(b). The dual-winding coupled inductor is modeled as an ideal transformer with a turn ratio N (n2 /n1), a parallel magnetizing inductance Lm, and primary and secondary leakage inductance Lk1 and Lk2.

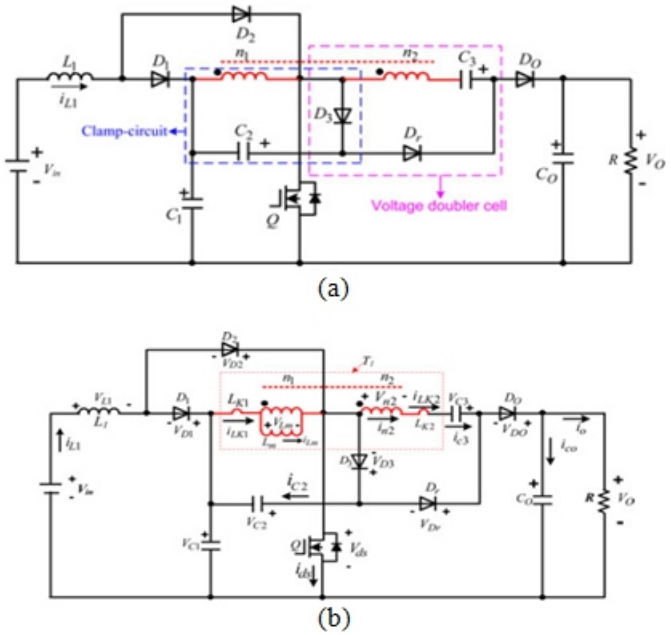

Fig.1.Circuit Configuration of Proposed Converter.

In order to simplify the circuit analysis of the converter, some assumptions are as follows:

1) The input inductance L1 is assumed to be large enough so that iL1 is continuous; every capacitor is sufficiently large, and the voltage across each capacitor is considered to be constant during one switching period;

2) All components are ideal except the leakage inductance of the coupled inductor;

3) Both inductor currents iL1 and iLm are operated in continuous conduction mode, which is expressed as C-CCM; the inductor current iL1 is operated in continuous conduction mode, but the current iLm of the coupled inductor is operated in discontinuous conduction mode, which is called C-DCM.

A.C-CCM:

Based on the aforementioned assumption, Fig.2 illustrates some key waveforms under C-CCM operation in one switching period.

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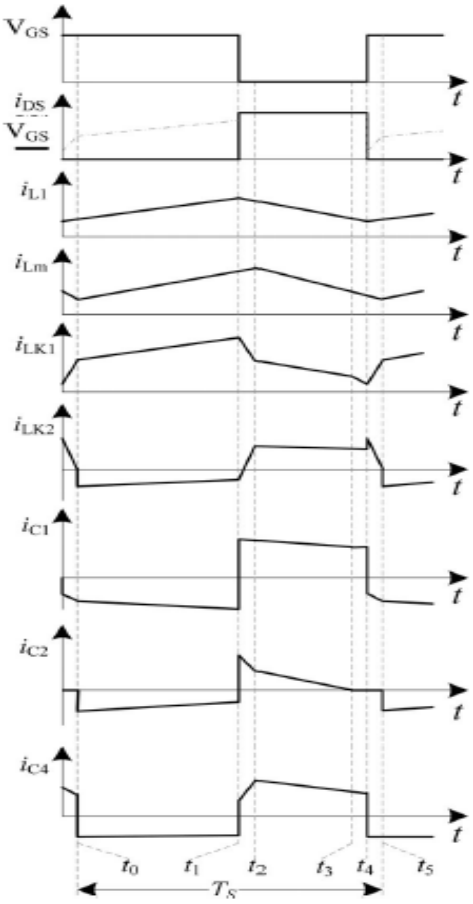


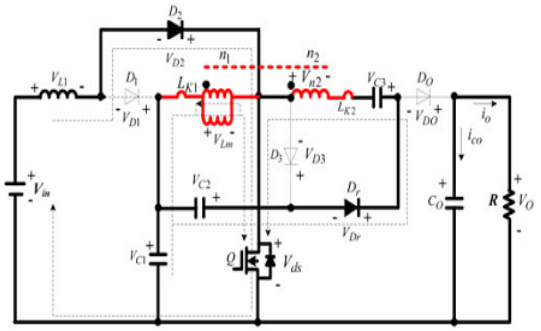
Fig.2. The Key Waveforms of The Proposed Converter At C-CCM Operation.

1) Mode1 [t0 –t1]:

The switch Q is conducting at t = t0. Diodes D1, D3, and DO are reverse-biased by VC1, VC1+VC 2 and VO − VC1 − VC2, respectively. Only Diodes D2 and Dr are turned ON. The current-flow path. The dc source Vin energy is transferred to the inductor L1 through D2 and Q.

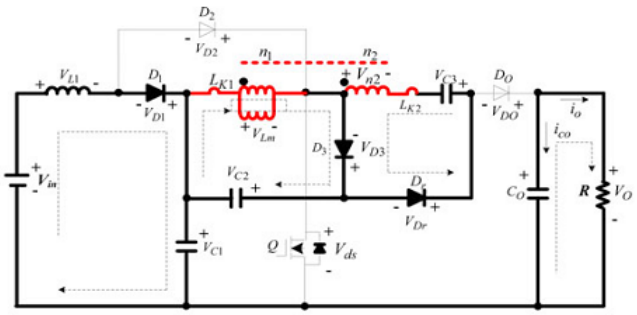
Therefore, the current iL1 is increasing linearly. The primary voltage of the coupled inductor including magnetizing inductor Lm and leakage Lk1 is VC1 and the capacitor C1 is discharging its energy to the magnetizing inductor Lm and primary leakage inductor Lk1 through Q.

Then currents iD2, iLm, and ik1 are increasing. Meanwhile, the energy stored inC2 and C1 is released toC3 through Dr. The load R energy is supplied by the output capacitor CO. This Mode ends at t = t1.



2) Mode 2 [t1 –t2]:

In this transition interval, depicts the current-flow path of this mode. Once Q is turned OFF at t = t1, the current through Q is forced to flow through D3. At the same time, the energy stored in inductor L1 flows through diode D1 to charge capacitor C1 instantaneously and the current iL1 declines linearly. Thus, the diodeD2 is reverse biased by VC2. The diode DO is still reverse biased by VO − VC1 − VC2. The energy stored in inductor Lk1 flows through diodeD3 to charge capacitor C2. Therefore, the energy stored in Lk1 is recycled to C2. The iLK2 keeps the same current direction for charging capacitor C3 through diode D3 and regeneration-diode Dr. The voltage stress across Q is the summation of VC1 and VC2. The load energy is supplied by the output capacitors CO. This Mode ends when iLK2 reaches zero at t = t2.



3) Mode 3 [t2–t3]:

During this transition interval, switch Q remains OFF. Since iLK2 reaches zero at t = t2, VC2 is reflected to the secondary side of coupled inductor T1 ; thus, regeneration-diode Dr is blocked by VC3 + NVC2 . Meanwhile, the diode DO starts to conduct. Depicts the current-flow path of this mode. The inductance L1 is still releasing its energy to the capacitor C1. Thus, the current iL1 still declines linearly. The energy stored in Lk1 and Lm is released to C2. Moreover, the energy stored in Lm is released to the output via n2 and C3.

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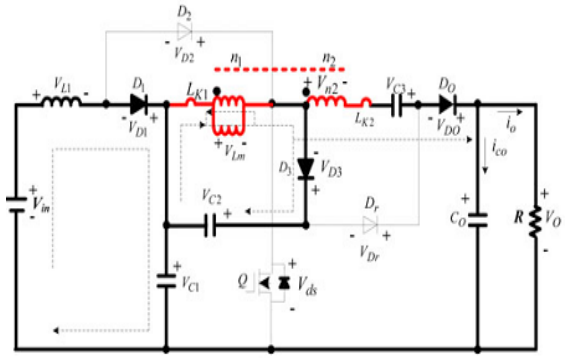
The leakage inductor energy can thus be recycled, and the voltage stress of the main switch is clamped to the summation of VC1 and VC2. This Mode ends when current iLK1 = iLK2, thus the current iC2 = 0 at t = t3.



4) Mode 4 [t3 –t4]:

During this time interval, the switch Q, diodes D2 and Dr is still turned OFF. Since iC2 reaches zero at t = t3, the entire current of iLK1 flows through D3 is blocked. The current-flow path of this mode. The energy stored in an inductor L1 flows through diode D1 to charge capacitor C1 continually, so the current iL1 is decreasing linearly. The dc source Vin, L1, Lm, Lk1, the winding n2, Lk2 and VC3 are series connected to discharge their energy to capacitor Co and load R. This Mode ends when the switch Q is turned ON at t = t4.

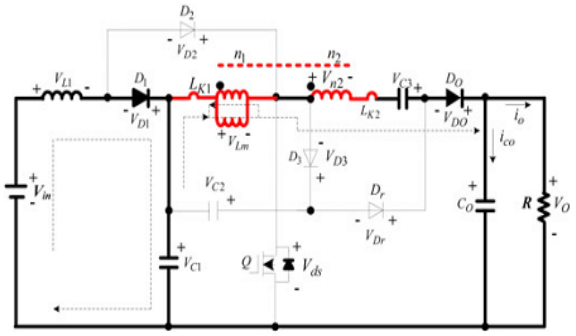
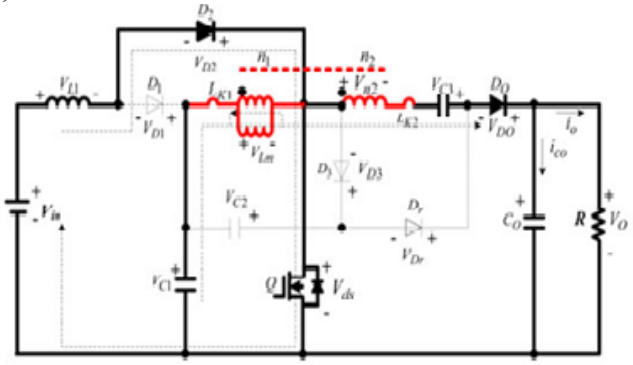


Fig.3. Equivalent Circuits of Five Operating Stages during One Switching Period at C-CCM Operation.

5) Mode 5 [t4 –t5]:

The main switch Q is turned ON at t4. During this transition interval, diodes D1, D3, and Dr are reverse-biased by VC1, VC1+VC 2 and VO − VC1 − VC2, respectively. Since the currents iL1 and iLm are continuous, only diodes D2 and DO are conducting. The current-flow path. The inductance L1 is charged by input voltage Vin , and the current iL1 increases almost in a linear way.

The blocking voltages VC1 is applied on magnetizing inductor Lm and primary-side leakage Lk1, so the current iLk1 of the coupled inductor is increased rapidly. Meanwhile, the magnetizing inductor Lm keeps on transferring its energy through the secondary winding to the output capacitor CO and load R. At the same time, the energy stored in C3 is discharged to the output. Once the increasing iLK1 equals the decreasing current iLm and the secondary leakage inductor current ik2 declines to zero at t = t5, this Mode ends.



B.C-DCM:

To simplify the C-DCM analysis, all leakage inductances of the coupled inductor are neglected. The coupled inductor is modeled as a magnetizing inductor Lm and an ideal transformer. The key waveforms of the proposed converter are shown in Fig.4.

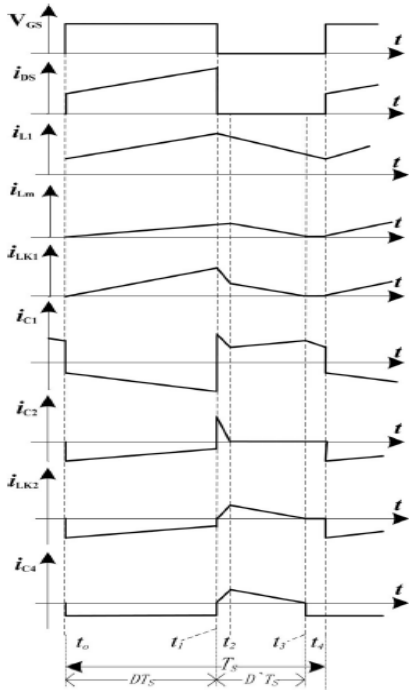


Fig.4. The Key Waveforms Of The Proposed Converter At C-DCM Operation.

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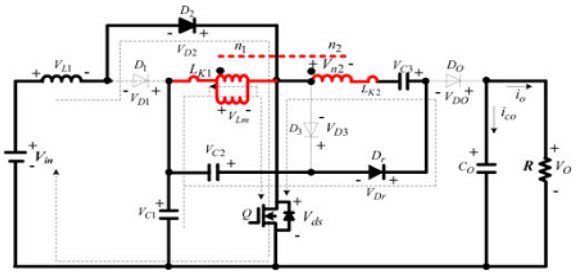
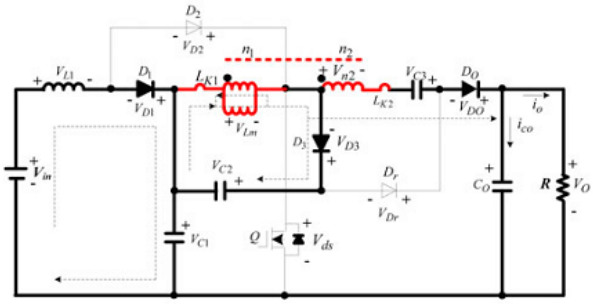
1) Mode 1 [t0 –t1]:

During this time interval, Q is turned ON. Diodes D2 and Dr are conducted but diodes D1, D3, and DO are blocked by VC1, VC1+VC2, and VO − VC1 − VC2, respectively. The current-flow path. The inductance L1 is charged by input voltage Vin; thus, the current iL1 increases linearly. The energy from capacitor C1 transfers to magnetizing Lm and current iLm increases linearly. Meanwhile, capacitor C3 is charged through the secondary winding coil n2 by capacitors C1 and C2. The output capacitor CO provides its energy to load R. The clamped diodeD3 is biased forward when the main switch Q is turned OFF at t = t1, and this Mode ends.



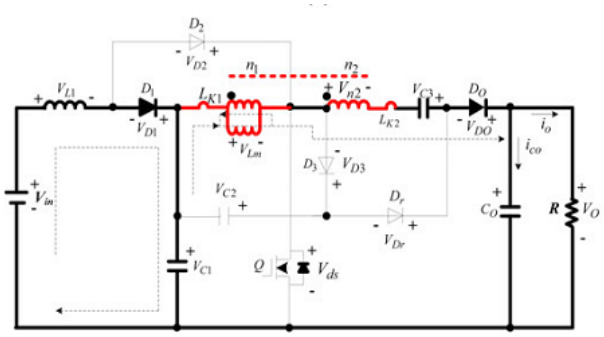
2) Mode 2 [t1–t2]:

At t = t1, the switch Q is turned OFF, resulting in a current commutation between the switch Q and diode D3 immediately. During this transition time interval, diodes D2 and Dr are turned OFF because they are respectively anti biased by VC2 and VO − VC1 − VC2, and other diodes are conducting. The current-flow path. The dc sources Vin is series-connected with inductor L1 and transfer their energies to the capacitor C1 through D1. The capacitors C2 is charged by the magnetizing inductor Lm via D3. Similarly, the dc source Vin, inductor L1, magnetizing inductor Lm and capacitor C3 are series connected to transfer their energy to capacitor Co and load R. This Mode ends when the rising current iC3 equals to current iLm at t = t2. At the same instant, the diode D3 is reverse biased at t = t2.



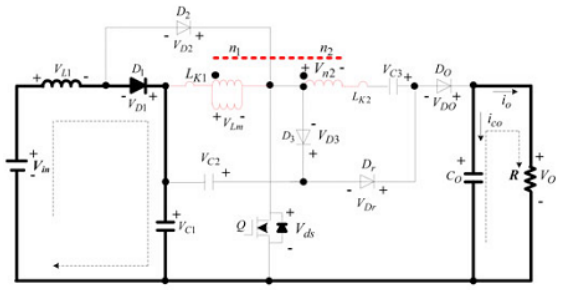
3) Mode 3 [t2 –t3]:

During this time interval, the switch Q, D2 and Dr remain turned OFF. The diodes D1 and Do are still turned ON. Since iC2 reaches zero at t2, the coupled inductor transfers energy to the output, and diode D3 is also blocked. The current-flow path. The dc source Vin and the input inductor L1 are still connected serially to charge capacitor C1. Thus, the current iL1 continues to decrease. Meantime, the primary and secondary sides of doubled-inductor are serially connected, and serially connected with VC3, delivering their energy to the output capacitor CO and load R. This Mode ends when the current iLm reduces to zero at t = t3.



4) Mode 4 [t3 –t4]:

During this transition time interval, the switch Q and the diode D2 is still turned OFF. Meanwhile, the primary and secondary currents of the coupled inductor have run dry at t3. Therefore, the diode D3 is still blocked by VC1+VC2, and only diode D1 is conducting for continuous iL1. The current-flow path. The capacitor C1 is still charged by the energy stored in L1 and dc sources Vin. Since the energy stored in Lm is empty, the energy stored in CO is discharged to load R. This Mode ends when Q is turned ON at t = t4, which is the beginning of the next switching period.



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III.STEADY-STATE ANALYSIS OF PROPOSED CONVERTERS

A.C-CCM Operating Conduction:

To simplify the analysis, the leakage inductances of the coupled inductor are neglected in the steady-state analysis. Also, the losses of the power devices are not considered. Only modes 1 and 3 are considered for C-CCM operation because the time durations of modes 2, 4, and 5 are short significantly. At mode1, the main switch Q is turned ON, the inductor L1 is charged by the input dc source Vin, and the magnetizing inductor Lm is charged by the voltage across C1. The following equations can be written from Fig. 4.

$$V_{L1} = V_{\text{in}} \tag{1}$$

$$V_{Lm} = V_{C1} \tag{2}$$

And the voltage of the switched capacitor$C3$ can be expressed by

$$V_{C3} = NV_{C1} + V_{C1} + V_{C2} \tag{3}$$

During modes 3, the main switch Q is in the OFF state, the inductor $L1$ and magnetizing inductor Lm are discharged, respectively. The voltages across the inductor $L1$ and Lm can be obtained by

$$V_{L1} = V_{\text{in}} - V_{C1} \tag{4}$$

$$V_{Lm} = -V_{C2} \tag{5}$$

$$V_O = V_{C1} + (N+1)V_{C2} + V_{C3} \tag{6}$$

Using the inductor volt-second balance principle to the inductor $L1$ and magnetizing inductor Lm, the following equations can be expressed as:

$$\int_0^{DT_s} V_{\text{in}}dt + \int_{DT_s}^{T_s} (V_{\text{in}} - V_{C1})dt = 0 \tag{7}$$

$$\int_0^{DT_s} V_{C1}dt + \int_{DT.}^{T_s} (-V_{C2})dt = 0. \tag{8}$$

From (1)–(8), the voltages across capacitors $C1$, $C2$, and $C3$ are derived as follows:

$$V_{C1} = \frac{V_{\text{in}}}{1-D} = \frac{(1-D)V_O}{2+N} \tag{9}$$

$$V_{C2} = \frac{D \cdot V_{\text{in}}}{(1-D)^2} = \frac{DV_O}{2+N} \tag{10}$$

$$V_{C3} = \frac{(N+1-DN)V_{\text{in}}}{(1-D)^2} = \frac{(N+1-DN)}{2+N}V_O \tag{11}$$

Substituting (9)–(11) into (6), the dc voltage gain MC-CCM is obtained as

$$M_{\text{C-CCM}} = \frac{V_O}{V_{\text{in}}} = \frac{(2+N)}{(1-D)^2}. \tag{12}$$

B.C-DCM Operating Condition:

In C-DCM operation, there are four Modes. During the time of mode 1, the switch Q is turned ON, and only diodesD2 and Dr are turned ON. The following equations can be written as:

$$V_{L1} = V_{\text{in}}$$

$$V_{Lm} = V_{C1}$$

$$V_{n2} = NV_{Lm} = V_{C3} - V_{C2} - V_{C1}.$$

During the time of mode 3, the switch Q is turned OFF, and only diodesD1andDO are conducting. The voltage levels across inductorL1 and magnetizing Lm and the secondary winding coil n2 are given as follows:

$$V_{L1} = V_{\text{in}} - V_{C1}$$

$$V_{Lm} = \frac{V_{C3} + V_{C1} - V_O}{N+1}$$

$$V_{n2} = \frac{N(V_{C3} + V_{C1} - V_O)}{N+1}.$$

During the time of mode 2, the output voltage VO can be expressed as

$$V_o = V_{C1} + V_{C3} + (N+1)V_{C2}.$$

If $D\_$ is defined as the duty cycle of the magnetizing inductor current from peak point ramped down to zero. By applying the volt-second balance principle to the inductor $L1$, magnetizing inductor Lm and the secondary side of winding coil $n2$, the following equations are derived:

$$\int_0^{DT_s} V_{\text{in}}dt + \int_{DT_s}^{(D+D')T_s} (V_{\text{in}} - V_{C1})dt = 0$$

$$\int_0^{DT_s} V_{C1}dt + \int_{DT_s}^{(D+D')T_s} \frac{V_{C3} + V_{C1} - V_O}{N+1}dt = 0$$

$$\int_0^{DT_s} (V_{C3} - V_{C1} - V_{C2})dt + \int_{DT_s}^{(D+D')T_s} \times \frac{N(V_{C3} + V_{C1} - V_O)}{N+1}dt = 0.$$

The voltages of $C1$, $C2$, $C3$, and $D\_$ are obtained

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$$V_{C1} = \frac{V_{in}}{1-D}$$

$$V_{C2} = \frac{D \cdot V_{in}}{(1-D)D'}$$

$$V_{C3} = \frac{[(N+1)D' + D]V_{in}}{(1-D)D'}$$

$$M_{C-DCM} = \frac{V_O}{V_{in}} = \frac{(2+N)(D'+D)}{(1-D)D'}$$

IV.MATLAB MODELING AND SIMULATION RESULTS:

Platform to the practicability of the proposed converter. Here simulation is carried out in two different cases 1) Implementation of Proposed Converter with constant DC Sources operated in CCM mode Operating under Open Loop System 2) Implementation of Proposed Converter with constant DC Sources operated in DCM mode Operated under Open Loop System 3) Implementation of Proposed Converter Operating Under Closed Loop System.

Case 1: Implementation of Proposed Converter with constant DC Sources Operated in CCM Mode Operating under Open Loop System.

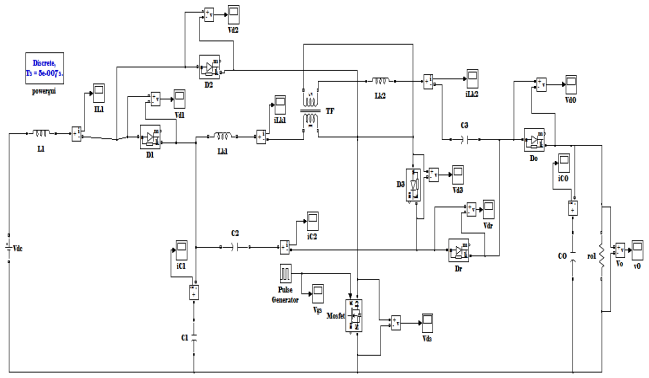

Fig 5. Matlab/Simulink Model of Proposed High Step up DC/DC Converter Operated in CCM Mode.

Fig.5. shows the Matlab/Simulink Model of Proposed High Step up DC/DC Converter Operated in CCM Mode under Open Loop System using Mat lab/Simulink platform.

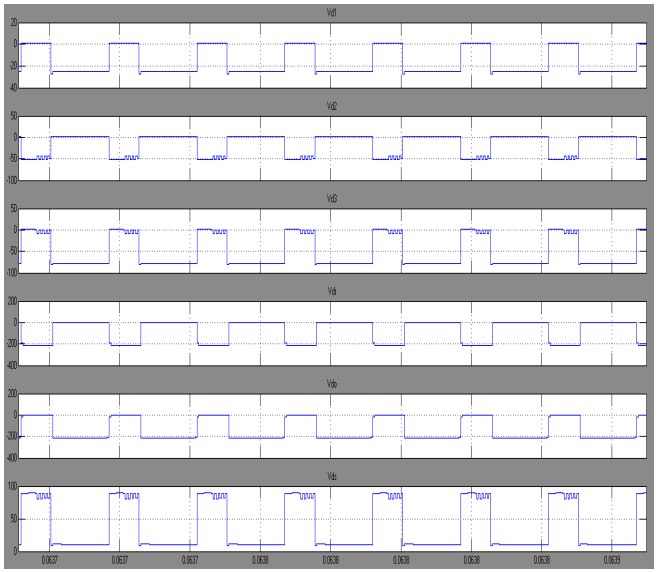

Fig.6. Diode across Voltages & Switch across Voltage

Fig.6. shows the Diode across Voltages & Switch across Voltage of Proposed High Step up DC/DC Converter Operated in CCM with Open Loop Mode.

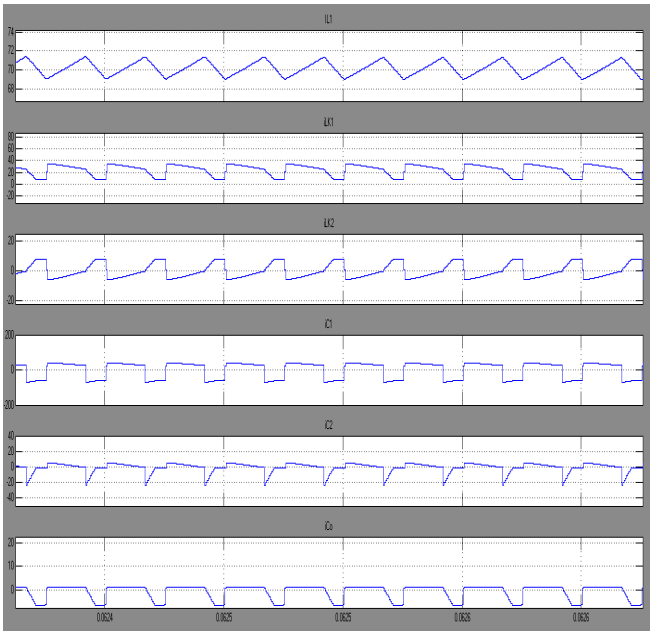

Fig.7. Capacitor Currents, Input Inductor Currents, Output Capacitor Current

Fig.7 shows the capacitor currents, input inductor currents, output capacitor current of Proposed High Step up DC/DC Converter Operated in CCM with Open Loop Mode.

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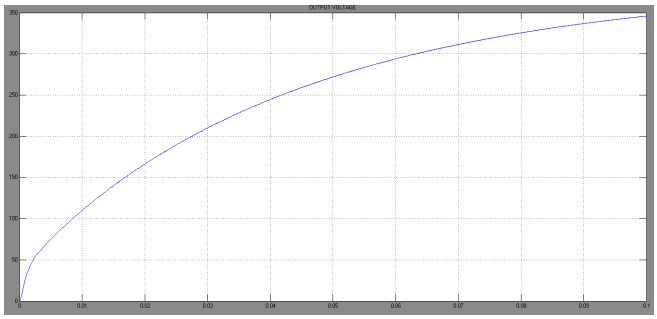

Fig.8. Output Voltage

Fig.8. Output Voltage of Proposed High Step up DC/DC Converter Operated in CCM with Open Loop Mode.

Case 2: Implementation of Proposed Converter with constant DC Sources operated in DCM mode operating Under Open Loop System.

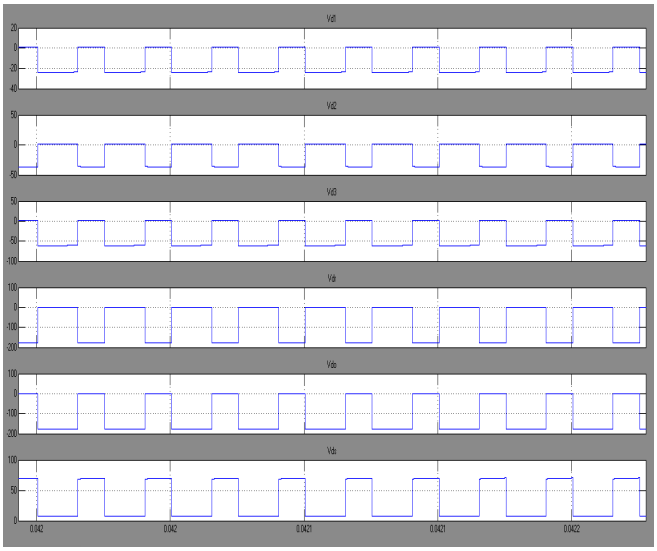

Fig.9. Diode across Voltages & Switch across Voltage

Fig.9. shows the Diode across Voltages & Switch across Voltage of Proposed High Step up DC/DC Converter Operated in DCM with Open Loop Mode.

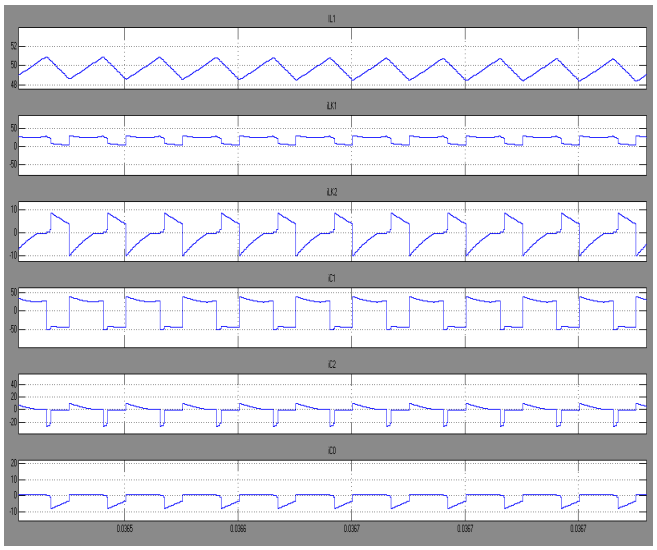

Fig.10. Capacitor Currents, Input Inductor Currents, Output Capacitor Current.

Fig.10. shows the capacitor currents, input inductor currents, output capacitor current of Proposed High Step up DC/DC Converter Operated in DCM with Open Loop Mode.

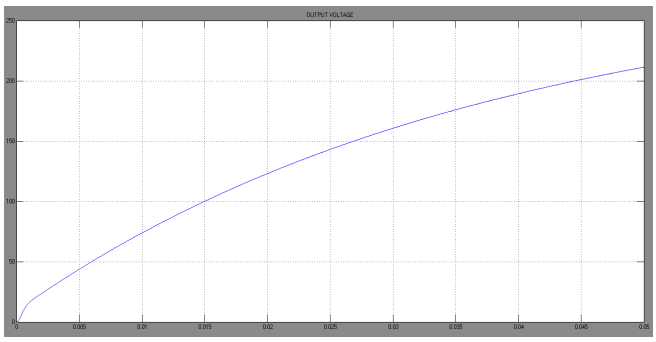

Fig.11 Output Voltage

Fig.11 Output Voltage of Proposed High Step up DC/DC Converter Operated in DCM with Open Loop Mode.

Case 3 Proposed Converter Operating under Closed Loop System

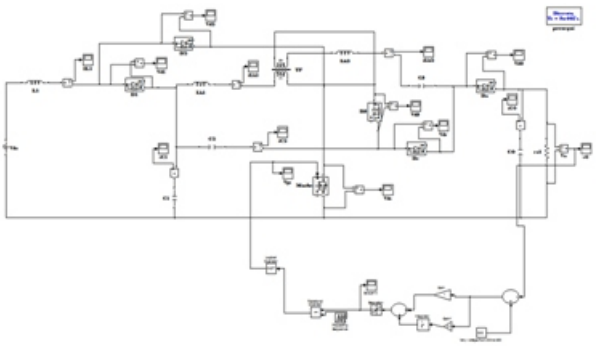

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Fig.12 Matlab/Simulink Model of Proposed Converter Operating under Closed Loop System.

Fig.12 shows the Matlab/Simulink Model of Proposed Converter Operating under Closed Loop System using Matlab/Simulink platform.

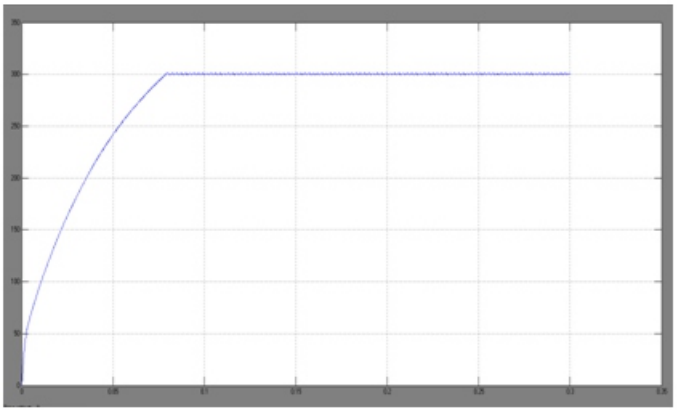

Fig.13.Converter Output Voltage

Fig.13 shows the Converter Output Voltage of Proposed Converter Operating under Closed Loop System compare to open loop system, here attain fast response because of low steady stare error value and system may operate under good stability factor.

V.CONCLUSION:

Power electronics applications requiring high-voltage high-power converters have been steadily growing in fields such as interfacing RES system, power quality, power systems control, adjustable speed drives, and uninterruptible power supplies (UPS), and co-generation. Most applications demand high voltage gain converters. Various converter topologies have been proposed in the literature, to improve performance, adapt to requirements and avoid proprietary technologies. This paper proposes the non-isolated high step-up converter operating under closed loop system for industry applications. This proposed converter combines a quadratic boost converter with coupled inductor and diode–capacitor techniques for attaining high voltage values. A clamped-capacitor circuit is connected to the primary side of the coupled inductor, the voltage stress of the active switch is reduced greatly and the clamped capacitor also transfers the primary leakage energy to the output.

At last a same converter applied to DC bus system and is controlled by closed loop PI control strategy with good dynamic response and low steady state error value with high stability factor.

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