ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Low Power Vedic Sutras for an Advanced Square and Cube Architectures

C.Suneetha
Assistant Professor
Department of ECE,
Kallam Harnadha Reddy Institute of Technology,
Guntur, Andhrapradesh, India.

C. Aruna Bala
Professor,
Department of ECE,
Ravindra College of Engineering for Women,
Kurnool, Andhra Pradesh, India.

ABSTRACT

Square and cube architectures can be uses as element in such applications like DSP, DIP, and communication and etc., there are different ways for designing this circuit as if with the multiplier. That is not the ideal approach of designing in present advanced systems with the power, speed and area. We proposed a novel approach of designing the square and cube architectures by using the one of the fast and less power method called Anurupyena sutra of Vedic mathematics. These are very efficient because the operation not as with the normal, and also the have the pipelined execution feature. In proposed design Vedic multiplication method Urdhwa Tiryakbhyam Sutra is chosen for the sub module design. There by decreases the critical path delay compare to that of any other alternative method. The designing can done using VERILOG and simulated using model-sim and synthesized using Xilinx

Keywords— ***Square, Cube, Anurupyena, Urdhwa Tiryakbhyam Sutra, Vedic Mathematics***

INTRODUCTION

As expanding the application of the present modern systems high speed architecture are necessitate in demand. These arithmetic operations needs higher throughput ids desired for the real time processing applications like image processing (compression and decompression), image encoding and decoding, communications, adaptive networking, least means square and data encryption and decryption requires square and cube architectures. They also requires the time delay and power consumption is more essential Up till now the square and cube systems are designed using normal methods composes of multiplier. Normally the multiplier is more power consumed digital design as this internally consists the partial product generation and multi operand addition and final addition that causes the increases the area and power in advancement of present VLSI features we cannot accept this type of designing . Even in for the design of performance increased multiplier the present researches are moving to vedic mathematic approaches. vedic mathematic is one of the promising alternative for the present ALU requirements. In this work we have put into effect a high speed and less power square and cube architectures. The architectures implemented by Anurupyena sutra due to its feature fat operation and multiplier less architecture. The Urdhwa Tiryakbhyam Sutra used at different levels of design drastically reduces the delay when compared to conventional designs. The hardware implementation of square and cube Vedic designs using Anurupyena sutra contributes to adequate improvement of the speed in order to achieve high outturn.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Section II provides a related introduction towards Vedic sutras. Section III describes the proposed architecture. Section IV simulation results and design analysis of square and cube architectures and proposed design. Section V represents the conclusions. Followed by references

VEDIC MATHEMATICS

Vedic math is taken from the traditional Indian Vedas; they are very much used in India for fast oral calculation without paper and pen.

The technique in that the calculation are carried out by using the different main 16 sutras, different upa sutras and inferences derived from these Sutras. Algebra, arithmetic, geometry or trigonometry etc any mathematical calculation can be carried out by this sutra efficiently. Vedic Mathematics is more tenacious than modern mathematics.

Generally the "Vedic mathematics" is comprised of sixteen simple mathematical formulae from the Vedas [5].

1. Ekadhikena Purvena
2. Nikhilam navatascaramam Dasatah
3. Urdhva - tiryagbhyam
4. Paravartya Yojayet
5. Sunyam Samya Samuccaye
6. Anurupye - Sunyamanyat
7. Sankalana - Vyavakalanabhyam
8. Puranapuranabhyam
9. Calana - Kalanabhyam
10. Ekanyunena Purvena
11. Anurupyena
12. Adyamadyenantya - mantyena
13. Yavadunam Tavadunikrtya Varganca Yojayet
14. Antyayor Dasakepi
15. Antyayoreva
16. Gunita Samuccayah.

PROPOSED DESIGN

Square Architecture

There are different sutras for the square calculations but those are limited with some bases. In our proposed method Square Architecture designed using dwandwa yoga property of urdhvatiryagbhyam sutra.

The "Dwandwa Yoga" means the duplex or dual. Here it senses as squaring and cross multiplication. In order to calculate the square using dwandwa yoga the urdhvatiryagbhyam sutra can be used. It described that first calculate the square of lower half (LSP) and higher upper half (MSP) and multiply LSP and MSP and twice then from the final result by concatenating the all internal results. Proposed square architecture is shown in figure.1.The algorithm steps with example are stated below.

Example:

Consider a=1011

Step 1: calculate the square of LSP and MSP

10*10=0100 (MSP square)

11*11=1001 (LSP square)

Step 2: multiply LSP and MSP

10*11=110

Step 3: add multiplication result twice

110+110=1100

Step 4: add and concatenate the intermediate results

1. Concatenate MSP square lower half and LSP square upper half (00&10) =0010
2. Add with twice added multiplied result (1100) and concatenated intermediate squares (0010)

1100+0010=1110

Step 5: concatenate the all results

(01&1110&01)=01111001

In our proposed architecture we use the advance multi-operand addition method along with parallel processing of the internal method shown in figure 1. The Vedic square has all the vantages of the Vedic multiplier.lot more it is degree faster and smaller foot print compared to that of the array, Booth.

Rather than adding the multiplier result twice and then adding to the Concatenate MSP square lower half and LSP square upper half. We add them together that consumes the less area and increases speed of operation.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Cube Architecture

The cube architecture can be designed by using the Vedic sutra called Anurupyena Sutra even though there are different sutras for the cube calculations but this Anurupyena Sutra is ideal choice. In this method we use the hierarchy design for the sub modules design. For multiplication we use the urdhvatiryagbhyam sutra.

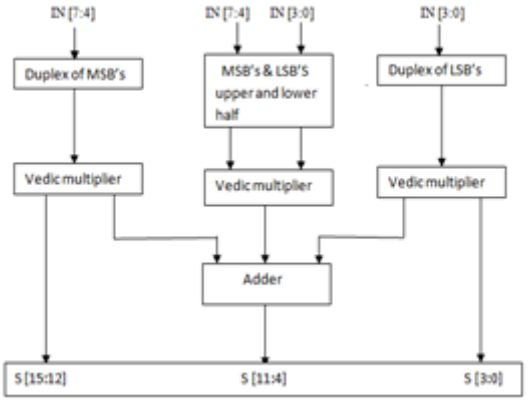

Fig 1. 8-bit Vedic Square Architecture

The steps that are involved in Anurupyena Sutra are described below.

Step 1: calculate the cubes of LSP and MSP

Step 2: calculate the squares of LSP and MSP

Step 3: multiply the squared LSP result with MSP and squared MSP result with LSP (Intermediate results)

Step 4: multiply the intermediate results with '3' (0011)

Step 5: concatenate the all results

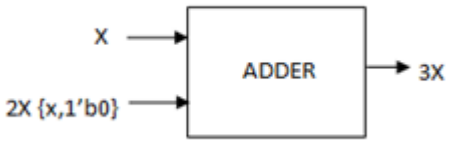

Fig 2: Proposed multiplied by 3 Circuit(3MCM)

For multiple contant multiplication we add the input (X) and left shifted input (2X) to produce the 3X output.There by unnesissary multiplier can be avioded. Proposed MCM-3 is shown in fig.2

The proposed mthod can have less foot print and can run very efficient performance with the proposed MCM-3 method ,for designin the left shift operation in MCM-3 we should not uses the any other shifter.

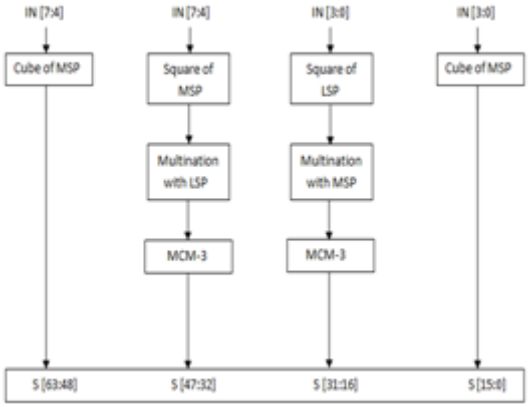

Fig 3. 8-bit Vedic Cube Architecture

For square calculations we use the above square architecture III (a) .and for the intermediate multiplication with the constant '3' can be done with the multiple constant multiplication which is the better method for multiplication .that causes the only one adder can be used as excess. By that the area can be reduced and performance also will be increased.*-bit cube architecture is shown in figure.3

SIMULATION RESULTS

In our work, 8-bit squaring and cube architectures are designed in Verilog HDL. Simulate using model-sim and Synthesis is done using Xilinx - Project Navigator and Xilinx ISE simulator. Synthesis results are compared with previous method.

Thus, proposed method outperforms previous method in terms of speed, area and low power. The proposed squaring architecture may be useful for the design of hardware for computer arithmetic.

Fig 4&5 shows obtained the result of proposed Vedic square and cube. These architectures are faster than conventional square and cube.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

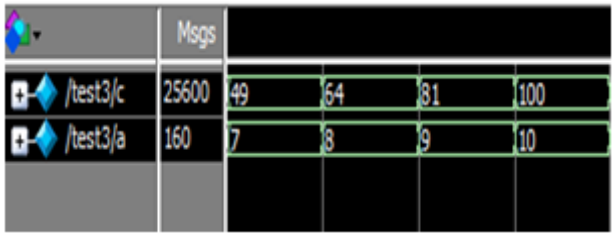

Fig 4: Square design output

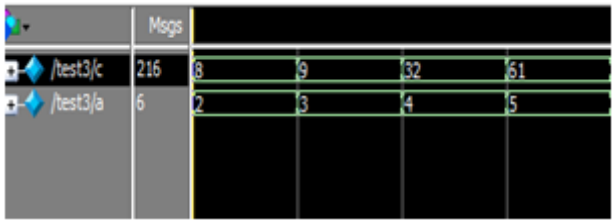

Fig 5: cube design output

CONCLUSION

Vedic square and cube multiplier can be designed with the advanced design methods can be done that makes the efficient design and reduces the operation time. The extra advanced logic MCM based design can be done. Rather than using the normal multiplier MCM can uses the very less area. We designed the 8-bit, 16-bit and 32- bit architectures are designed and comparison evaluation can be carried out in this paper.

REFERENCES

[1] Vaijyanath kunchigi, Linganagouda Kulkarni and Subhash Kulkarni "Low Power Square and Cube Architectures Using Vedic Sutras" 2014 Fifth International Conference on Signals and Image Processing

[2] Y.Yu Fengqi and A. N.Willson,"Multirate digital squarerarchitectures," in Proc. 8th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS 2001), Malta, Sept. 2–5, 2001, pp. 177–180.

[3] Swami Bharati Krisna Tirtha, "Vedic Mathematics," Motilal Banarsidass Publishers, Delhi, 1965.

[4] H. D. Tiwari, G. Gankhuyag, C. M. Kim, and Y. B. Cho, "Multiplier design based on ancient Indian Vedic Mathematics," in Proceedings IEEE International SoC Design Cotiference, Busan, Nov. 24-25, 2008,pp. 65-68

[5] Kunchigi, V.; Kulkarni, L.; Kulkarni, S., "High speed and area efficient vedic multiplier," Devices, Circuits and Systems (ICDCS), 2012 International Conference on , vol., no., pp.360,364, 15-16 March 2012

[6] Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni. Article: Simulation of Vedic Multiplier in DCT Applications.International Journal of Computer Applications 63(16):27-32, February 2013. Published by Foundation of Computer Science, New York, USA.

[7] Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni 32-BIT MAC UNIT DESIGN USING VEDIC MULTIPLIER – published at: "International Journal of Scientific and Research Publications (IJSRP), Volume 3, Issue2, Feburary 2013 Edition".

[8] H. Thapliyal, M. B. Srinivas and H. R. Arabnia , "Design And Analysis of a VLSI Based High Performance Low Power Parallel quare Architecture", in Proc. Int. Conf. Algo. Math. Comp. Sc., Las Vegas, June 2005, pp. 72–76.

[9] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global J. of Engg. Edu., vol. 8, no. 2, pp. 153–158, 2004.

[10] H. Thapliyal and M. B. Srinivas, "High Speed Efficient N × N Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Enformatika Trans., vol. 2, pp. 225-228, Dec. 2004.

[11] J.Bhasker, "Verilog HDL Primer" BSP Publishers, 2003.

[12] Himanshu Thapliyal, S. Kotiyal and M.B. Srinivas, "Design and Analysis of a Novel Parallel Square and Cube Architecture Based on Ancient Indian Vedic Mathematics", Proceedings on 48th IIEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),

[13] Himanshu Thapliyal and Hamid R. Arabania, "A Time- Area – Power Efficient Multiplier and Square Architecture Based on Ancient Indian Vedic Mathematics", proceedings on VLSI04, Las Vegas, U.S.A, June 2004

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Author Details

C. Suneetha, she has received her bachelor's degree in ECE from Acharya Nagarjuna University, Guntur and master's degree in VLSI form JNTUK, Kakinada. Currently, she is working as an assistant professor in Kallam Harnadha Reddy Institute of Technology, Guntur, Andhrapradesh. She has an experience of 8 years. Her current research interested areas are low power VLSI.

Prof. Smt. C. Aruna Bala is working as Professor in the Department of ECE at Ravindra College of Engineering for Women, Kurnool. She has 6 years of experience in the field of R&D (computers) at Bangalore and 18 years of teaching experience. She has completed her Ph.D. She is waiting for Ph.D. certificate. She has obtained her master's degree in Communication Engineering from JNTUH. She has obtained her bachelor's degree in Electronics and Communication Engineering from Bapatla Engineering College, Nagarjuna University. Her area of Research is "High Resolution ADC using Micron Technology". She has published 11 research publications and 10 National and International Conferences in the area of ECE.