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Design and Implementation of A Low Power Modified Viterbi Decoder With T-Algorithm

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Abstract:

We propose a pre-computation architecture incorporated with T-algorithm for VD, which can effectively reduce the power consumption without degrading the decoding speed much. A general solution to derive the optimal pre-computation steps is also given in the paper. The Add Compare Select (ACS) unit in path metric unit is designed to reduce the latency of ACS loop delay by using Modified Carry Look Ahead Adder and Digital Comparator. We also consider the design of Survivor Memory Unit (SMU) which combines the advantages of both Register Exchange method and Trace Back method, to reduce the decoding latency and total area of the Viterbi decoder. The proposed Viterbi decoder design is described using Verilog HDL Implementation result of a VD for a rate-3/4 convolutional code used in a TCM system shows that compared with the full trellis VD, the precomputation architecture reduces the power consumption by as much as 70% without performance loss, while the degradation in clock speed is negligible.

Index Terms:

ACS Unit, viterbi decoder, VLSI.

I. INTRODUCTION:

Convolutional encoding is considered to be one of the forward error correction scheme. This coding scheme is often used in the field of deep space communications and more recently in digital wireless communications. Adaptive Viterbi decoders are used to decode Convolutional codes. This technique is used for error correction. It is very efficient and robust. The main advantage of Viterbi Decoder is it has fixed decoding time and also it suites for hardware decoding implementation. But the implementation requires the exponential increase in the area and power consumption to achieve increased decoding accuracy.

Convolution coding with Viterbi decoding is a FEC technique that is particularly suited to a channel in which transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN). In most of real time applications like audio and video applications, the Convolutional codes are used for error correction. Different architectures have been proposed to achieve high throughput and low area for Viterbi decoder. Methods available to achieve high throughput are look ahead method, pipeline architecture, block based concept, compare select add method and sliding block method. Register Exchange method is used to reduce the overall area of Viterbi decoder and Trace Back method is used to minimize the power consumption of Survivor Memory Unit (SMU).

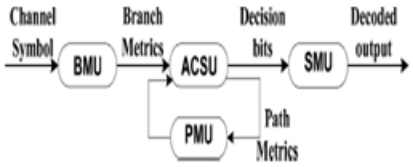

Fig. 1. Functional Diagram of Viterbi Decoder

It Proposed the look-ahead technique to speed up the Add Compare Select (ACS) unit. It proposes the MSB First ACS unit with pipeline architecture to reduce the ACS loop latency. Bit level high speed Viterbi decoder is proposed. And also it proposes different design techniques to reduce the latency of ACS unit and SM unit for hard decision Viterbi decoder. Block based approach is described in to increases the throughput of ACS unit in Viterbi decoder. An efficient pre-trace back architecture to reduce the memory access and area of the survivor memory unit is presented in this paper. In this paper we proposes implementation of trace-back unit for reconfigurable Viterbi decoder to reduce the power consumption and area of survivor memory unit. The remainder of this paper is organized as follows. Section II gives the background information of VDs.

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Section III presents the precomputation architecture with T -algorithm and discusses the choice of precomputation steps. Details of a design example including the modification of survivor-path memory unit (SMU) are discussed in Section III. Simulation results are reported in Section IV and conclusions are given in Section V.

II.VITERBI DECODER:

A typical functional block diagram of a Viterbi decoder is shown in Fig. 1. First, branch metrics (BMs) are calculated in the BM unit (BMU) from the received symbols. In a TCM decoder, this module is replaced by transition metrics unit (TMU), which is more complex than the BMU. Then, BMs are fed into the ACSU that recursively computes the PMs and outputs decision bits for each possible state transition. After that, the decision bits are stored in and retrieved from the SMU in order to decode the source bits along the final survivor path. ThePMs of the current iteration are stored in the PM unit (PMU).T -algorithm requires extra computation in the ACSU loop for calculating the optimal PM and puncturing states. Therefore, a straightforward implementation of T-algorithm will dramatically reduce the decoding speed. The key point of improving the clock speed of T–algorithm is to quickly find the optimal PM.

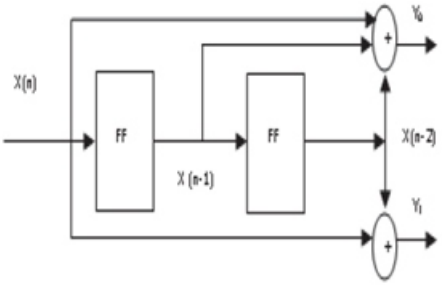


Fig.2. Rate ½ Encoder

Y1Yo- Encoder output bits,
X (n-1) X (n-2) – previous state of Encoder,
X (n)-input bit to Encoder.

The convolutional encoder is basically a finite state machine. The k bit input is fed to the constraint length K shift register and the n outputs are calculated from the generator polynomials by the modulo-2 addition. The generator polynomial specifies the connections of the encoder to the modulo-2 adder. The '1' in the generator polynomial indicates the connections and zero indicates no connections between the stage and modulo -2 adders.

For a rate 1/2 encoder with constraint length of 3, the code can correct up to 2 errors in 16 bits of transmitted data. Here it is assumed that errors do not occur in consecutively. The code rate, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. A rate 1/2 encoder is implemented in the design.

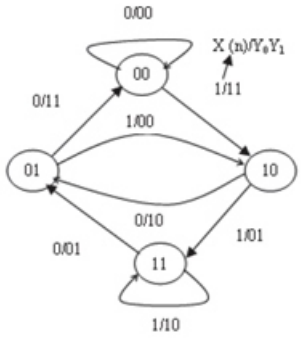
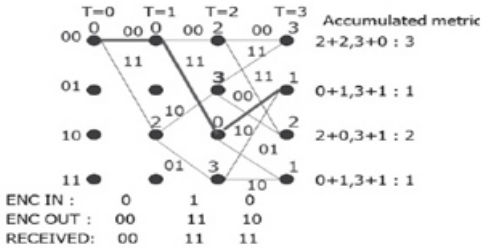


Fig.3. State Diagram

State diagram: This offers a complete description of the system. However, it shows only the instantaneous transitions. It does not illustrate how the states change in time.
Trellis diagram: To include time in state transitions,



III.PROPOSED VITERBI DECODER:

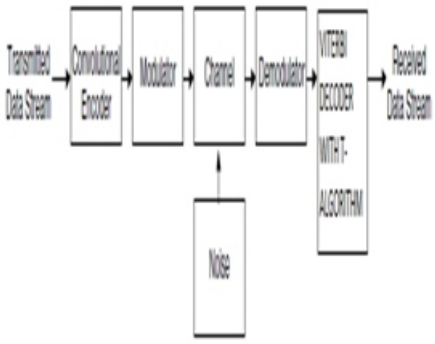


Fig.5. Block diagram of the system with T-algorithm.

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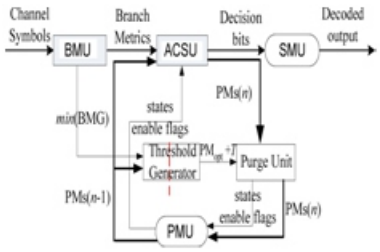

Fig.6. Architecture of Viterbi Decoder With T-Algorithm

A.Branch Metric Unit:

The branch metric is a measure of the distance between what was transmitted and what was received and is defined each arc in the trellis. In hard decision decoding, where we have given a sequence of parity bits, the branch metric is the hamming distance between the expected parity bits and the received bits. As example is shown in Fig. 3.3.1.1.1 where received bits are 00. For each state transition, the number on the arc shows branch metric for its transition. Two of the branch metrics are 0, corresponding to only states and transitions where the corresponding hamming distance is 0.

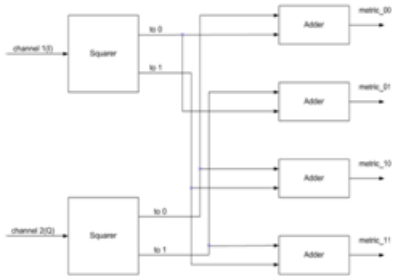

Fig.7. Block Diagram BMU

An attractive soft decision metric is the square of the difference between the received and expected. If the convolutional code produces the p parity bits, and the corresponding analog samples are v= v1, v2, v3,…..,vp, then we can construct the branch metric as (1)

$$BM[U,V] = \sum_{i=1}^{P} (Ui - Vi)2 \qquad (1)$$

Where $u = u_1, u_2, u_3, \ldots, u_p$ are expected parity bits.

B.Path Metric Unit:

Path metric unit (PMU) is comprised of Add Compare Select unit and a Memory to store the partial state metrics.

The proposed Add Compare Select (ACS) unit is designed for code rate 1/2, constraint length K=3 and generator polynomials (101,111)8. The ACS unit is critical in terms of throughput and area due to the presence of feedback loop referred as the ACS loop. The ACS loop is non-linear in nature. This ACS loop recursively selects the minimum state metric and gives an output of a decision bit based upon minimum state metric. The selected minimum state metric is updated for the particular node or state in next clock cycle for the next operation. A survivor path is selected and its state metric updated for each state at each recursion.Suppose the receiver has computed the path metric PM[s, i] for each state s (of which there are 2k1 , where k is the constraint length) at time step i. The value of PM[s, i] is the total number of bit errors detected when comparing the received parity bits to the most likely transmitted message, considering all messages that could have been sent by the transmitter until time step I (starting from state '00' , which we will take by convention to be the starting state always).

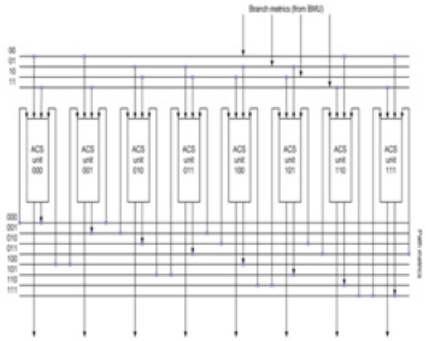

Fig.8. Implementation of PMU (Path Metric Unit)

Add Compare Select Unit:

A new value of the state metrics has to be computed at each time instant. In other words, the state metrics have to be updated every clock cycle. Because of this recursion, pipelining, a common approach to increase the throughput of the system, is not applicable. The Add-Compare-Select (ACS) unit hence is the module that consumes the most power and area In order to obtain the required precision, a resolution of 7 bits for the state metrics is essential, while 5 bits are needed for the branch metrics. Since the state metrics are always positive numbers and since only positive branch metrics are added to them, the accumulated metrics would grow indefinitely without normalization. In this project we have chosen to implement modulo normalization, which requires keeping an additional bit (8 instead of 7).

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The operation of the ACS unit is shown in Figure 6 The new branch metrics are added to previous state metrics to form the candidates for the new state metrics. The comparison can be done by using the subtraction of the two candidate state metrics, and the MSB of the difference points to a larger one of two.Hamming distance between the received code word and the allowed code word is calculated by checking the corresponding bit positions of the two code words. For example hamming distance between the code words 00 and 11 is 0 or the hamming distance between the code words 00 and 11 is 2. The hamming distance metric is cumulative so that the path with the largest total metric is final winner. Thus the hard decision Viterbi decoding makes use of maximum hamming distance in order to determine the output of the decoder.

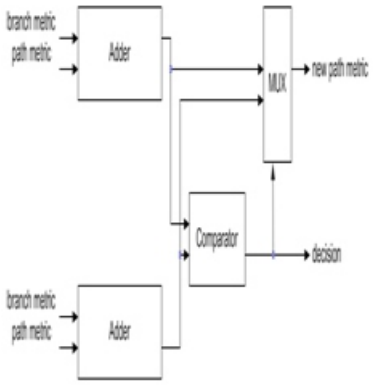

Fig.9. ACSU (Add-Compare-Select unit) Architecture

Purge Unit:

When a state is purged in ACSU, the corresponding registers in SMU are not updated; thus, the power consumption is reduced. purged computation changes accordingly in the case of the T-algorithm on PMs, whereas in the case of the T–algorithm on BMs, the number of purged computation remains almost the same, regardless of the channel condition.

C.Survivor Memory Unit:

In this section, we address an important issue regarding SMU design when T-algorithm is employed. There are two different types of SMU in the literature: register exchange (RE) and trace back (TB) schemes. In the regular VD without any low-power schemes, SMU always outputs the decoded data from a fixed state (arbitrarily selected in advance) if RE scheme is used, or traces back the survivor path from the fixed state if TB scheme is used, for low-complexity purpose.

IV.SIMULATION RESULTS:

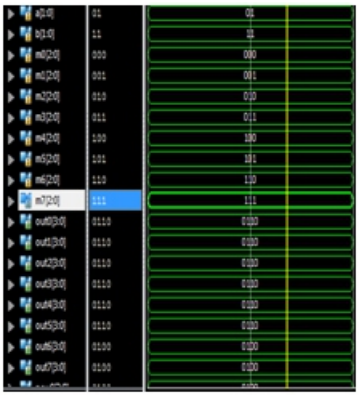

Fig.10. Simulation results of proposed Viterbi

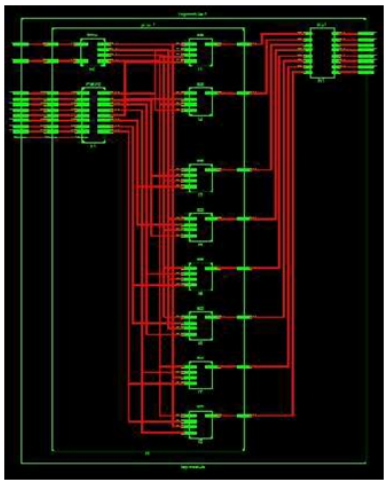

Fig.11. Enlarged Tech schematic of proposed Viterbi

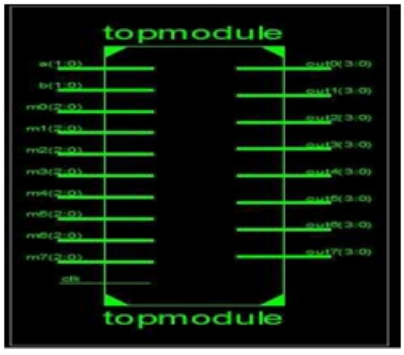

Fig.12. RTL Schematic diagram for Proposed Viterbi

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V.CONCLUSION:

We have proposed a high-speed low-power VD design. The pre-computation architecture that incorporates T –algorithm efficiently reduces the power consumption of VDs without reducing the decoding speeds appreciably. This algorithm is suitable for TCM systems which always employ high-rate convolution codes. Finally, we presented a design case. Both the ACSU and SMU are modified to correctly decode the signal.

VI.FUTURE SCOPE:

We can implement viterbi decoder with SPEC T-algorithm. Here, we take advantage of the SPEC-T algorithm proposed in to reduce the length of critical path. The key idea of the SPEC T-algorithm is to use an estimated optimal PM value derived from the optimal BM value, instead of searching for the optimal PM in each cycle.

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