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# Design of a Low-Voltage Low-Dropout Regulator

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## Abstract:

A low-voltage low-dropout (LDO) regulator that converts an input of 1 V to an output of 0.85–0.5 V, with 90-nm CMOS technology is proposed. A simple symmetric operational transconductance amplifier is used as the error amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency, a 28-mV output variation for a 0–100mA load transient, and a power supply rejection of roughly 50 dB over 0–100kHz. The area of the proposed LDO regulator is only 0.0041 mm2, because of the compact architecture.

## Index Terms:

Fast transient response, high power supply rejection, low-dropout (LDO) regulator, low-voltage, small area.

## I.INTRODUCTION:

Power management unit with several integrated regulators is widely used in modern battery-powered portable devices. These power management schemes often use a primary switching regulator and several post regulators [1], [2]. The primary switching regulator converts the high dc voltage level of the battery (e.g., 4.2–2.7 V) into a low dc voltage level (e.g., 1 V) with a high conversion efficiency (>90%). The post regulators also generate several independent power sources for multiple voltage domains. The switching regulator inevitably generates voltage ripples over the range of the switching frequency. The switching frequency of the regulator often lies within a low-frequency band of a few 10–100 kHz to reduce switching power loss.The post-regulators should, therefore, be able to provide a good power supply rejection (PSR) ability to suppress these unwanted low-frequency noises. To further maintain high power efficiency, minimize the impact on target load circuits, and reduce cost, the post regulators must operate at low voltage and low quiescent current (IQ), achieve a fast transient response with a small output variation, and minimize their area. The low-dropout (LDO) regulator has a simple architecture and a fast-responding loop, which makes it the best candidate to implement these postregulators.A number of previous papers focused on enhancing the transient response [3]–[10] or the PSR [2], [4], [5], [10], [11] or both of LDO regulators. The designs in [3]–[5] and [8] use either a large driving current or additional circuits, whichconsume a significant IQ. The design in [6] consumes a small IQ, yet has a large output variation during the load transient. The dynamic biasing technique is widely adopted by conducting a very small IQ under a light load condition [9], [10]. This inevitably sacrifices the transient response during a light to heavy load current transition. The LDO regulators proposed in [2] and [11] achieved a high PSR over a very wide frequency range (up to 10 MHz). Using bipolar junction transistor process technology [11] or a complex ripple cancellation circuit [2] to achieve a PSR >10 MHz at the expense of a high IQ is, however, unnecessary for the postregulator of a general purpose switching regulator. Further, a complex compensation circuit [6] or a high-gain cascode error amplifier (EA) [7] complicates the LDO regulator design and is not feasible for low-voltage systems (≤1 V) that are using advanced technology. All the previous regulators [2]–[11] are unable to achieve sub 1-V operation.

## II. DESIGN CHALLENGES AND CONCEPTS OF THE PROPOSED LOW-VOLTAGE LDO REGULATOR:

A basic LDO regulator is mainly composed of a biasing circuit, an EA, a power MOS transistor (MP ), and a feedback network, as shown in Fig. 1.

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Now, the transient accelerator (TA) is removed. An off-chip output capacitor (CL) is used to mitigate the output variations during the load transient. The design challenges and concepts in designing a low voltage LDO regulator are summarized briefly in the following sections.

## A. Low Supply (Input) Voltage and Low IQ:

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable IQ that are proposed to enhance performance. A MP with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA requires a higher current slew rate to drive the MP. To achieve low-voltage operation, an EA with not more than three stacked transistors between the supply voltage and ground is preferred; each of the transistors, therefore, has more voltage space to stay in the saturation region. A possible candidate can be as simple as an operational transconductance amplifier (OTA) with a low-cost gain-boosting technique like current splitting [12]. The EA also requires a wide output swing to minimize the size of the MP , and hence relieve the requirement on output current slew rate of the EA.

## B. Fast Transient Response:

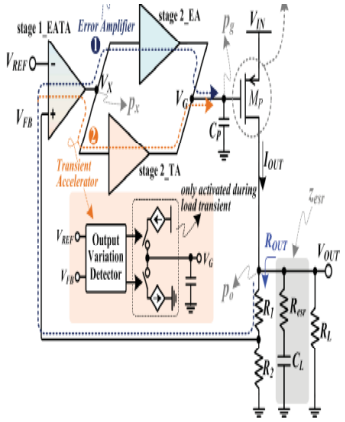
The transient response includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation (e.g., 50 mV) can cause severe performance degradation to the load circuit operating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required [13]. Increasing the closed-loop bandwidth may, however, affect the pole/zero locations and the circuitry may become too complex, consuming more IQ [4], [8]. The concept of the TA, shown in Fig. 1, is, therefore, adopted to conditionally provide extra charging/discharging current paths (slew current), depending on the status of the output variation detector.

## C. Power Supply Rejection:

To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An n-type power MOS transistor or a cascoded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a p-type power MOS transistor, either a high loop gain or good noise cancellation at node VG can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra IQ [2]. The concept of resources sharing power noise cancellation mechanism as shown in Fig. 1 is thus proposed. The first stage (stage 1_EATA) of the EA attenuates the power noise, whereas the second stage (stage 2_EA) of the EA rejects the common mode noise (vicm) at its inputs, and creates a replica of the supply noise at the output. The stage 1_EATA is shared by the EA and TA, saving the cost and IQ.

## D. Small Area:

In a low-voltage LDO regulator design, several performance enhancing auxiliary circuits and a large MP occupy considerable space. A wide output swing EA can reduce the size of the MP. To support a wide load current range (e.g., 0–100 mA) and a wide output-voltage range (e.g., 0.5–0.85 V), the MP may enter the triode region when under a heavy load condition (large VSG) with a low-dropout voltage (small VSD). The MP should, therefore, be large enough to make the intrinsic gain of the MP close to one at the triode region and maintain a high loop gain in the LDO regulator. Similarly, the LDO regulator can respond to the load current transient in time for such a wide range of operating conditions.



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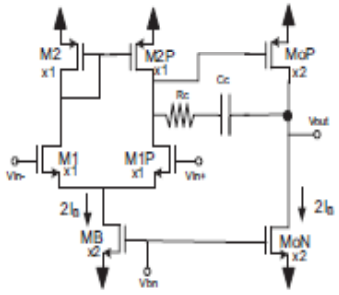
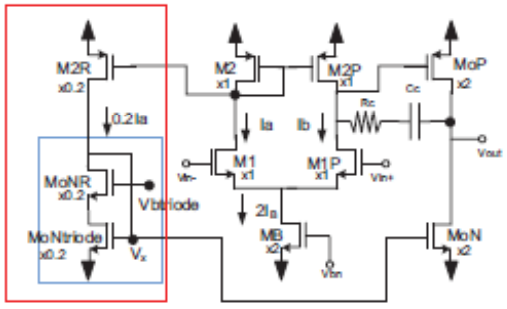


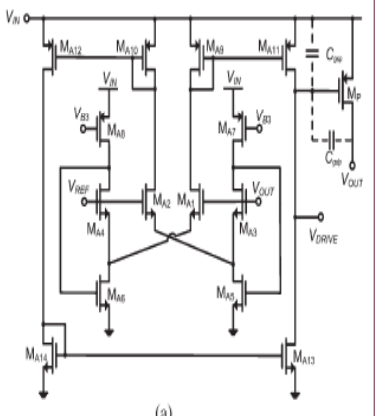

(a)

Fig.1: Conventional two-stage miller op-amp




(b)

Fig.3: Class-AB two stage op-amp with current replication branch and adoptive biasing.




(a)

Fig.2: Schematic of the LDO core circuit

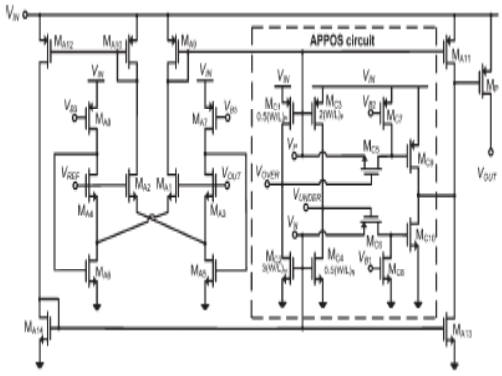



Fig. 4. Schematic of LDO with the APPOS circuit.

Fig.4: Schematic of the proposed LDO with the APPOS circuit

## E. Stability:

The dominant pole for an off-chip capacitor (e.g., CL = 1μF) compensated LDO regulator, exists at the output node (pO in Fig. 1). As a large MP contributes the first non-dominant pole (pg) at a relative low frequency, a large equivalent series resistance of CL (Resr) is required to generate a low frequency zero (zesr) to cancel pg. Therefore, large output variations during the load transient are induced by the large Resr.

A wide output swing EA can reduce the size of the MP implying that such pole-zero cancellation is taking place at a higher frequency with a related small Resr . Therefore, a smaller output variation during the load transient can be achieved.The second non-dominant pole (px) should be placed at a high frequency further, which implies a low resistance or low capacitance path at node VX.

## III. SIMULATION RESULTS:

The simulations of the above all designs are carried out by using H-SPICE tool in CMOS technology. The simulated waveforms for all above circuits are shown below.

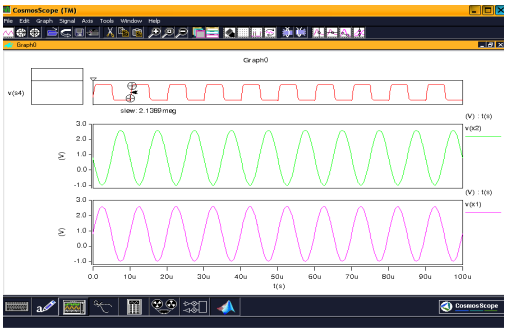



Fig.5: Simulation results for Conventional two-stage miller op-amp

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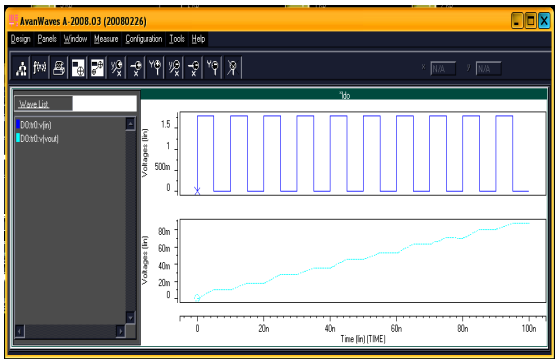

Fig.6: Simulation results of the LDO core circuit

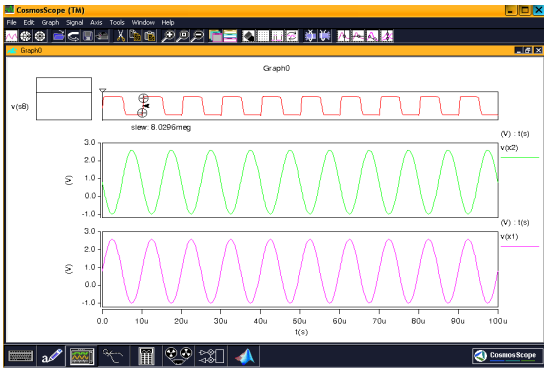

Fig.7: Simulation results of Class-AB two stage op-amp with current replication branch and adoptive biasing.

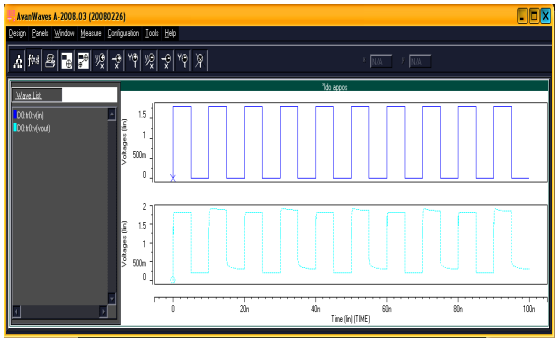

Fig.8: Simulation results of the proposed LDO with the APPOS circuit.

## IV.CONCLUSION:

This paper presented an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low IQ, and high PSR under a wide range of operating conditions. The proposed LDO regulator was designed and fabricated using a 90-nm CMOS process to convert an input of 1 V to an output of 0.85–0.5 V, while achieving a PSR of ~50 dB with a 0–100-kHz frequency range.

In addition, a 28-mV maximum output variation for a 0–100-mA load transient, and a 99.94% current efficiency was achieved. The experimental results verified the feasibility of the proposed LDO regulator.

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