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Fast Multiplication Energy-Efficient 7:2 Compressor

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Abstract:
In many of digital systems used in like graphical processors, digital signal processors fast parallel multiplication using adder trees are present. Multipliers have attracted lots of researchers' attention into making high-performance multipliers to consume less power and operate faster. This paper presents efficient implementation of comp ress tree adders on FPGAs. A new 7:2 compr essor architecture based on changing some internal equations are proposed. In addition, using an effi cient full-adder (FA) block is considered to have a high speed compressor. Three 7:2 compresso rs are considered for comparison. The proposed architecture is compared with the best existing designs presented in the state-of-the-art literature in terms of power, delay and area. The paper presents 7:2 compressors that are widely used as building blocks of multipliers. Lots of architectures for 5:2 compressors have been proposed in the literature. The number of transistors used in the design is less than the best existing 5:2 compr essor architectures. By a vast research on these structures, it has been revealed that the structures presented in and have better performance than others.

Index Terms—7: 2 compressor; multiplier; CMOS circuits

I. INTRODUCTION

Integrated circuit technology is the innovation technology for a whole host of innovative devices and systems which have changed our regular life. Integrated circuits are much smaller and consume low power than the discrete components used to build the electronic systems before the 1960. Integration allows us to build systems with many more transistors, allows more computing power to solve a problem. From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat produced into the rooms, the lower the electricity consumed and therefore, the less the impact on environment. The less the office noise (due to elimination of a fan from the desktop), and the less stringent the environment/office power delivery and cooling requirements. For high performance, portable computers, such as laptop and notebook computers, the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation (including that of display and hard disk). Finally, for high performance, non-battery operated systems, such as workstations, set-top computers and multimedia information processing and communication systems, the overall goal of power minimization is to reduce system cost (cooling, packaging and energy bill) and ensure long-term circuit reliability. These different requirements impact how power optimization is addressed and how much the designer is willing to sacrifice in cost or performance to obtain lower power dissipation. Integrated circuits are much easier to design and manufacture and are more reliable than discrete systems. Integrated circuits improve system characteristics in several ways.

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systems. Integrated circuits improve system characteristics in several ways.

Need For Low Power Design- The design of portable devices requires consideration for low power consumption to ensure reliability and proper operation. However, the time averaged power is often more critical as it is linearly related to the battery life. There are mainly four sources for power dissipation in digital CMOS circuits. They are: switching power, short-circuit power, leakage power and static power. The following equation describes these four components of power:

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} + P_{static} \quad (2.1)$$

$$= \alpha C_L V_{dd} V_s f_{ck} + I_{sc} V_{dd} + I_{leakage} V_{dd} + I_{static} V_{dd} \quad (2.2)$$

P switching is the switching power. For a properly designed CMOS circuit, this power component usually dominates, and may account for more than 90% of the total power. α denotes the transition activity factor, which is defined as the average number of power consuming transitions that is made at a node in one clock period. Vs is the voltage swing, where in most cases it is the same as the supply voltage, Vdd. CL is the node capacitance. It can be broken into three components, the gate capacitance, the diffusion capacitance, and the interconnect capacitance. The interconnect capacitance is in general a function of the placement and routing. fck is the frequency of clock. The switching power for static CMOS is derived as follows.

During the low to high output transition, the path from Vdd to the output node is con-ducting to charge CL. Hence, the energy provided by the supply source is

$$E = \int_0^\infty V_{dd} I(t) dt \quad (2.3)$$

where $I(t) = \frac{V_s}{R} e^{-t/RC_L}$ is the current drawn from the supply. Here, R is the resistance of the path between the Vdd and the output node. Therefore, the energy can be re written as

$$E = C_L V_{dd} V_s \quad (2.4)$$

During the high to low transition, no energy is supplied by the source. Hence, the average power consumed during one clock cycle is

$$P = \frac{E_{percycle}}{T} = C_L V_{dd} V_s f_{ck} \quad (2.5)$$

Eq. (2.4) and Eq. (2.5) estimate the energy and the power of a single gate only. From a system point of view, α is used to account for the actual number of gates switching at a point in time.

1.Pshortcircuit is the short-circuit power. It is a type of dynamic power and is typically much smaller than Pswitching. Isc is known as the direct-path short circuit current. It refers to the conducting current from power supply directly to ground when both the NMOS and PMOS transistors are simultaneously active during switching.

2.Pleakage is the leakage power. Ileakage refers to the leakage current. It is primarily determined by fabrication technology considerations and originates from two sources. The first is the reverse leakage current of the parasitic drain-/source-substrate diodes. This current is in the order of a few femto amperes per diode, which translates into a few microwatts of power for a million transistors. The second source is the sub threshold current of MOSFETs, which is in the order of a few nano amperes. For a million transistors, the total sub threshold leakage current results in a few milli watts of power.

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3.Pstatic is the static power and Istatic is static current. This current arises from circuits that have a constant source of current between the power supplies such as bias circuitries, pseudo-NMOS logic families. For CMOS logic family, power is dissipated only when the circuits switch, with no static power consumption. Energy is independent of the clock frequency. Reducing the frequency will lower the power consumption but will not change the energy required to perform a given operation, as depicted by Eq. (2.4) and Eq. (2.5). It is important to note that the battery life is determined by energy consumption, whereas the heat dissipation considerations are related to the power consumption. There are four factors that influence the power dissipation of CMOS circuits. They are technology, circuit design style, architecture, and algorithm. The challenge of meeting the contradicting goals of high performance and low power system operation has motivated the development of low power process technologies and the scaling of device feature sizes.

Design considerations for low power should be carried out in all steps in the design hierarchy, namely 1) Fundamental, 2) material, 3) device, 4) circuit, and 5) system.

Every 5:2 compressor has seven inputs and four outputs. Five inputs are primary inputs and the rest are two input carries which receive their values from the previous stage of one bit lower in significance. All the seven inputs, as well as output Sum bit have the same weight. The other three output bits weight one bit higher order.

A 5:2 compressor with five primary inputs X1, X2, X3, X4,X5 and two output bits Sum and Carry along with carry input bits, Cin1 and Cin2, and carry output bits, Cout1 and Cout2, is governed by the following equation:

$$x_1 + x_2 + x_3 + x_4 + x_5 + C_{in1} + C_{in2} = Sum + 2(Carrry + C_{out1} + C_{out2})$$

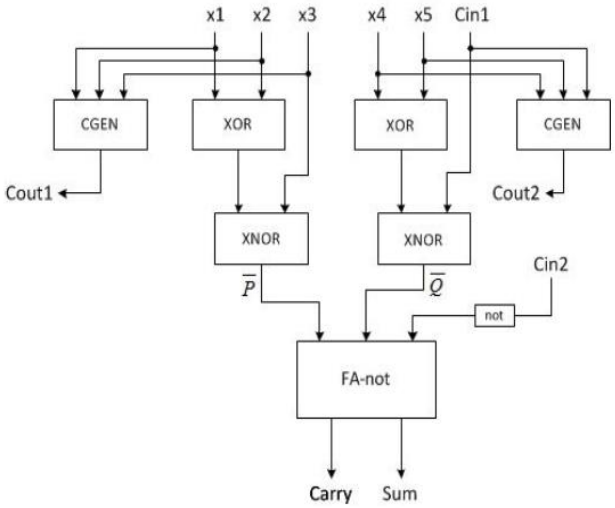

Figure.1 Figure of Proposed technique compressor

Historically, VLSI designers have used circuit speed 85the "performance" metric. Large gains, in terms of performance and silicon area**,** have been made for digital processors, microprocessors, Digital Signal Processors, Application Specific integrated circuits (ASICs), etc. In general, "small area" and "high performance" are two constraints for any design and the IC designer's activities have been involved in trading off these constraints**.** In fact, power considerations have been the ultimate design criteria in special portable applications such as wrist watches and pace makers for a long time.

The total Power Consumption for a CMOS circuit can be expressed by three types. They are: dynamic Power Consumption, leakage Power Consumption and direct-path consumption. The last two items are neglected due to their low contribution to the power. The dominant factor is the dynamic power based on the equation: $P= C_L f V^2$.

A. Power Consumption in CMOS circuits

Dynamic power dissipation:

$$P_{dynamic} = \alpha C_L V^2_{dd} f$$

Where C_L= total output capacitive load.

f = frequency of operation.

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α = switching activity factor.

Short circuit power dissipation:

This is the energy consumed during both pull-up and pull down transistors are conducting. This typically increases the total Power Consumption by 10%. This is also usually ignored in DSM.

B. Power dissipation in ALU

The instantaneous power P (*t*) drawn from the power supply is proportional to the supply current $I_{dd}(t)$and the supply voltage $V_{dd}(t)$.

$P(t) = I_{dd}(t)\, V_{dd}(t)$

The energy consumed over that time interval T is the integral of instantaneous power.

$E = \int I_{dd}(t)\, V_{dd}(t)$

This is the area under the current multiplied by voltage at the power supply. The average power used over this interval is the energy divided by the time. So in order to measure the power in the circuit we need to

able to measure the current from the power supply, plot that curve over time, integrate under that curve and multiply with V_{dd}.

Proposed new 7-2 compressor A 7-2 compressor gets a1, a2, a3, a4, a5, a6, a7 inputs with weights of one and generates two outputs Sum and Carry with weights of one and two, respectively. Also, it gets two input carry bits Cin1, Cin2 with the same weight of inputs and generates two output carry bits, Cout1, Cout2 with weights of two and four, respectively. As depicted our proposed design is constructed of a 5-4 arithmetic unit and two 3-2 counters. New 5-4 arithmetic unit The new 5-4 arithmetic unit gets seven inputs and generates four outputs as the following equations with the weights of one, two, two and two, respectively:

So1 and Co1 outputs are the main factors that determine the latency of the new (5-4) arithmetic unit. So decreasing of the delay depends on shortening these outputs critical paths. As depicted control signals X, Y and Z by their complementary outputs are generated simultaneously to be utilized in the proposed design. As XOR-XNOR circuit is utilized to generate E and F signals as the following equations. So1 and Co1 outputs are achieved after one inverter to avoid from driving problems. When the gate channel of a TG is ready to transmit its input to the output before receiving any inputs, its delay is decreased considerably. Z and Y signals are generated one gate level delay earlier than E and F signals. So, the channels of TGs are ready to transmit their input signals to outputs and so on, the latency is decreased considerably. As a result, So1 and Co1 outputs are generated after 2 gate level delays and plus 2 ready-channel transistors. The outputs Co2 and Co3 of the new 5-4 arithmetic unit are generated according to the following rewritten equations depict the implementations of Co2 and Co3 outputs. The advantage with these circuits is their full voltage swings at the output nodes and buffered output signals. Also, they decrease the driving problems in further stages, considerably. So, the delay of critical path in our proposed structure includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors.

II.LITERATURE REVIEW

Rapid growth of using multipliers has attracted lots of researchers' attention into making high-performance multipliers to consume less power and operate faster. Multiplication process includes three steps: 1) partial product generation; 2) partial product reduction; 3) final addition with carry propagating. The second step makes the worst-case delay consumes the main part of power, and occupies the high fraction of silicon area. To decrease the latency of this step, compressors have been widely employed. Therefore, designing a low-power and high-speed compressor is an important issue that should be raised to have a proper multiplication and subsequently a fast arithmetic computation.5:2 compressors are widely used as building blocks of multipliers [1, 2]. Lots of architectures for 5:2 compressors have been proposed in the literature [3-6]. By a vast research on these structures, have better performance than others. They

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have simulated their proposed compressor by CMOS XORXNOR modules and two different multiplexer implementations.

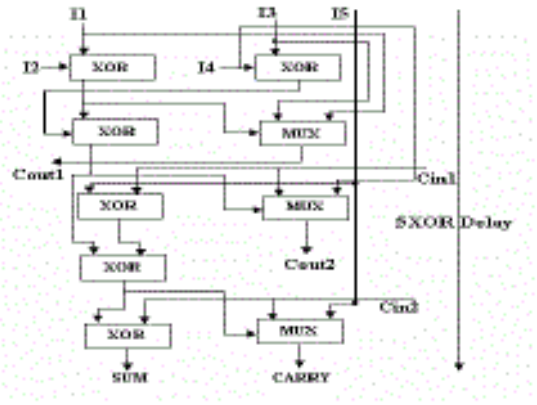

Fig.9. Alternative implementation of 5-2 compressor

Figure.2 Figure of Alternative implementation of 5:2 compressor

Every 5:2 compressor has seven inputs and four outputs. Five inputs are primary inputs and the rest are two input carries which receive their values from the previous stage of one bit lower in significance. All the seven inputs, as well as output Sum bit have the same weight. The other three output bits weight one bit higher order.

A 5:2 compressor with five primary inputs X1, X2, X3, X4, X5 and two output bits Sum and Carry along with carry input bits, Cin1 and Cin2, and carry output bits, Cout1 and Cout2, is governed by the following equation:

$$x_1 + x_2 + x_3 + x_4 + x_5 + C_{in1} + C_{in2} = Sum + 2(Carry + C_{out1} + C_{out2}) \quad (1)$$

Various structures for 5:2 compressors are available in the literature. The simplest implementation of 5:2 compressor is obtained by cascading three full-adders in a hierarchical structure. The structure has a critical path delay of 6Δ where Δ refers to delay of XOR-XNOR, XOR, MUX or CGEN module, as their critical delay difference is trivial. The structure of 5:2 compressor with critical path delay of4Δ has been proposed. A modified structure has been proposed in [8], which has a critical path delay of 5Δ.

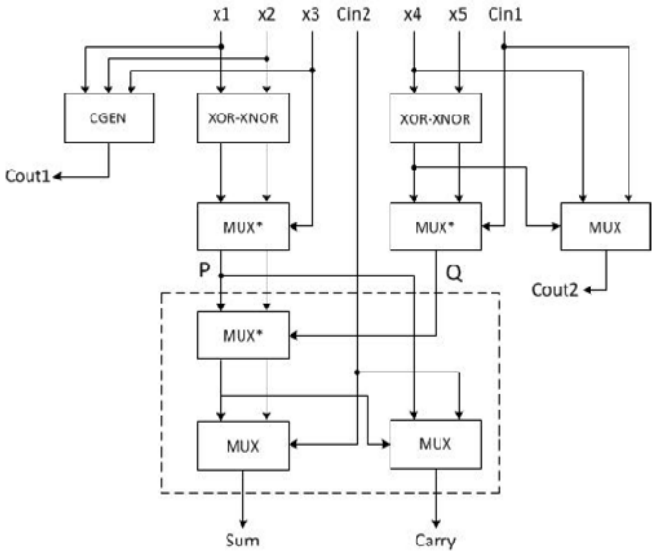

Fig.3. Figure of 5:2 compressor architecture proposed in -Arch-07

A. The compressor proposed in

Since CMOS implementation of MUX performs better than a XOR gate in terms of power and delay a 5:2 compressor based on using multiplexers in place of XOR gates. In CMOS implementation of the MUX and XOR-XNOR blocks, outputs and their comple ments are generated. But, complement outputs are not being utilized in architectures proposed. If the output of multiplexer is used as select bit of another multiplexer, it can be used efficiently, and an extra stage to compute the negation in multiplexer structure can be saved. The authors used CMOS-CGEN in their architecture to produce Cout1 signal. The architecture proposed called ***Arch-07*** in the rest of this paper and Arch-07 is one of the most efficient architectures that exist for 5:2 compressors and has been used in [2, 11, 12]. The authors performed simulation by using CMOS multiplexer and XOR-XNOR modules. In addition, has been used in Arch-07 as the MUX block of intermediate stages.

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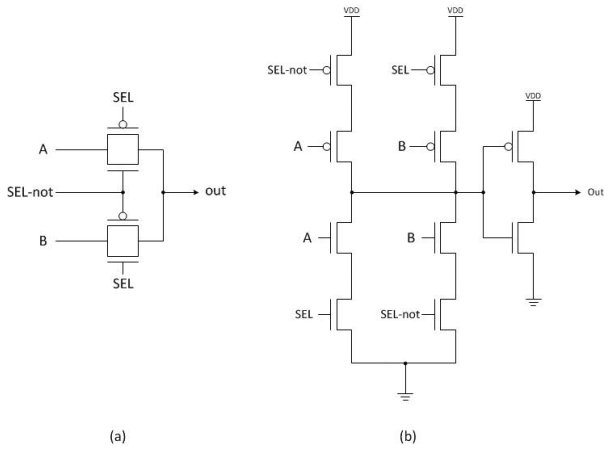

Fig. 4. (a) Transmission Gate implementation of multiplexer (b) CMOS implementation of multiplexer

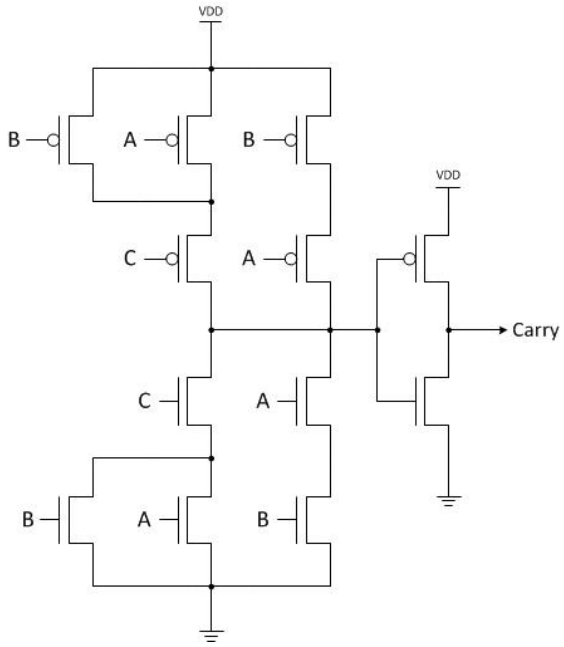

Fig. 5. CMOS implementation of Carry Generator module

In the proposed architecture changes are to be made, to efficiently use the generated outputs at every stage. To obtain efficient output, few XOR blocks are replaced by XOR blocks with MUX blocks. In the proposed architecture these outputs are utilized efficiently by using multiplexers at select stages in the circuit. In this additional inverter stages are also eliminated. This contributes to the reduction of delay, power consumed and number of transistors the combination of XOR-XNOR which is used to design the 5-2 compressor.

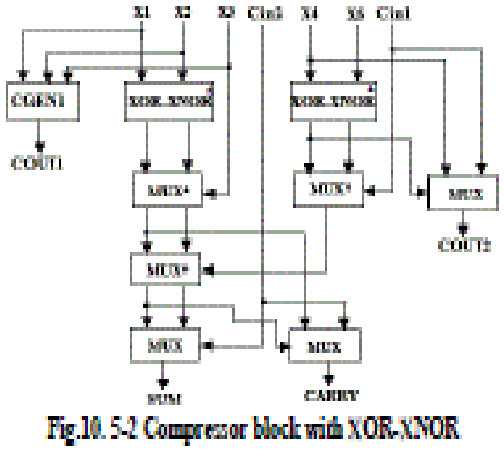

Figure.6 Figure of 5:2 compressor block with XOR, NOR

III. PROPOSED IMPLEMENTATION

In the proposed architecture two improvement approaches are used to propose the new 7:2 compressor. First, by a closer look at dashed box it represents the functionality of a conventional FA and can be replaced by variety of FAs presented in the literature. This replacement is expected to lead to considerable speed improvement, due to 34% faster operation of CMOS FA in comparison to two cascaded CMOS XOR gates. Therefore, the CMOS FA presented in 7:2 compressor architecture

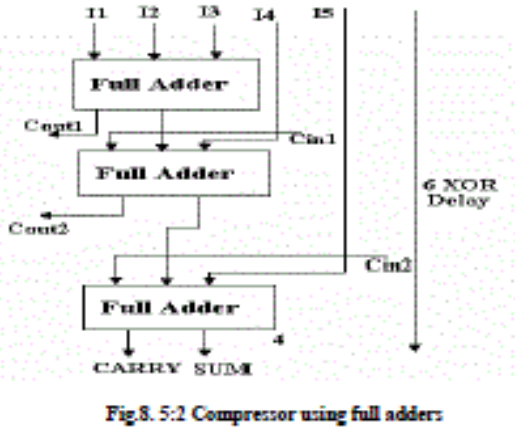

Figure.7 5:2 compressor with Full adders

To further improvement, we make some changes to internal equations of the 7:2 compressor to eliminate final Not gates of the CMOS FA. By doing so, we

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could have reduced power dissipation as well as improved operational speed. To achieve this goal, we have to use XNOR gates instead of XORs of the second stage of the architecture this design uses 82transistors in its architecture (i.e. 6 transistors less than Arch-13).

In this architecture, FA-not is CMOS FA which its final Not gates have been eliminated.

CGEN modules have been used to produce Cout1 and Cout2 output signals. In addition, outputs of the XOR gates have been fed to inputs of the XNOR gates. This way, outputs of the XNOR gates are negation of what it was before for conventional 7:2 compressors and by replacing a FA-not instead of a FA we can have valid Sum and Carry signal.

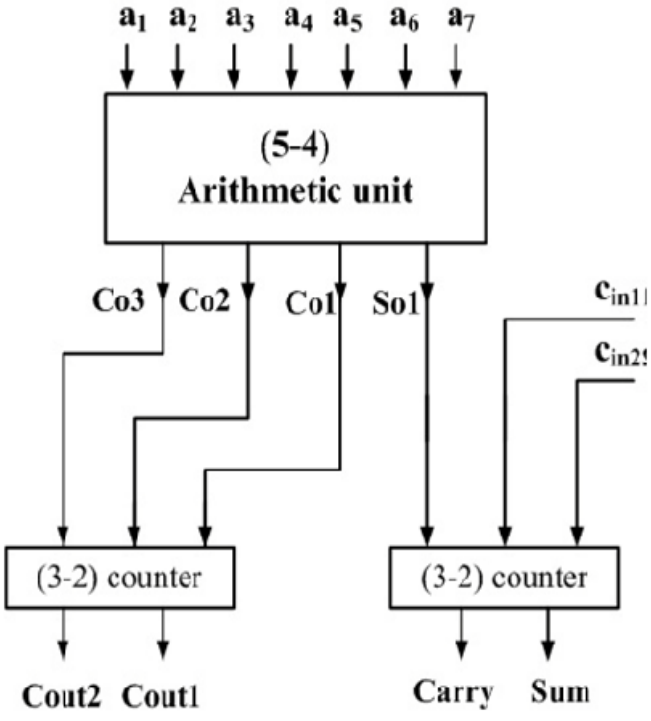

Fig. 8. Proposed 7:2 compressor design-New Arch

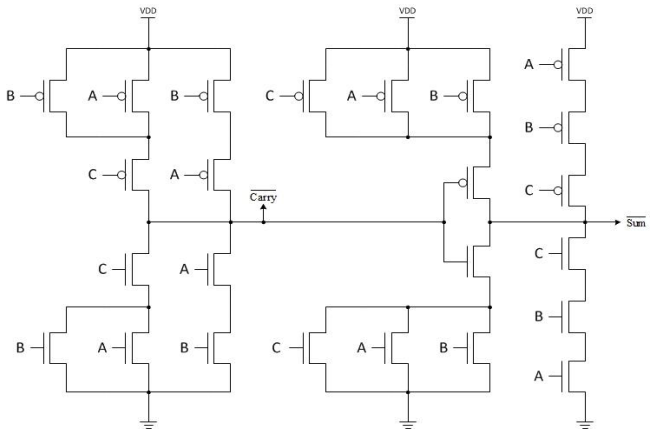

Fig. 9. CMOS implementation of FA-not cell

We know the following equation

$$\overline{x} \oplus \overline{y} = x \oplus y$$

$$\overline{x \oplus \overline{y}} = x \oplus y$$

Therefore, (3) and (4) proves the accuracy of the mentioned methods.

$$\overline{(\overline{P} \oplus \overline{Q}) \oplus \overline{C_{in2}}} = (P \oplus Q) \oplus \overline{C_{in2}} = P \oplus Q \oplus C_{in2} \quad (3)$$

$$\overline{(\overline{P} + \overline{Q}) \cdot \overline{C_{in2}} + \overline{PQ}} = PQ + PC_{in2} + QC_{in2} = (P+Q) \cdot C_{in2} + PQ \quad (4)$$

It is worth mentioning that P and Q are nodes which represent XNOR gates outputs of the proposed architecture. In addition, they are logical complement of P and Q nodes, respectively

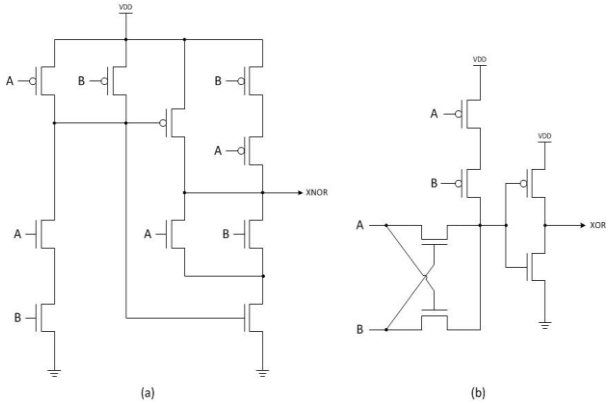

Fig. 10. (a) CMOS implementation of XNOR gate (b) XOR gate using pass transistor logic.

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The XOR and XNOR gates which have been used in the proposed architecture

The logic equations governing the proposed 5:2 compressor architecture are detailed in (5)-(8)

$$Sum = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus C_{in1} \oplus C_{in2} \quad (5)$$

$$C_{out1} = (x_1 + x_2) \cdot x_3 + x_1 x_2 \quad (6)$$

$$C_{out2} = (x_4 + x_5) \cdot C_{in1} + x_4 x_5 \quad (7)$$

$$Carry = ((x_1 \oplus x_2 \oplus x_3) + (x_4 \oplus x_5 \oplus C_{in1})) \cdot C_{in2} + (x_1 \oplus x_2 \oplus x_3) \cdot (x_4 \oplus x_5 \oplus C_{in1}) \quad (8)$$

4. SIMULATION RESULTS AND ANALYSIS

The 7-2 compressor is the another widely used buil ding block for high precision and high speed multipliers.

The basic block diagram of a 7-2 which has seven inputs and four outputs. Five inputs are the primary inputs x1, x2, x3, x4 and x5, x6,x7, and the other two inputs cin1and cin2 receive their values from the neighboring compressor of one binary bit order lower insignificance

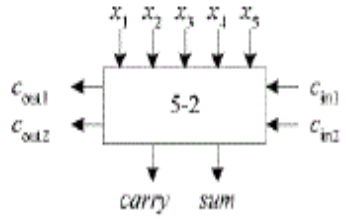

Fig.7. 5:2 compressor

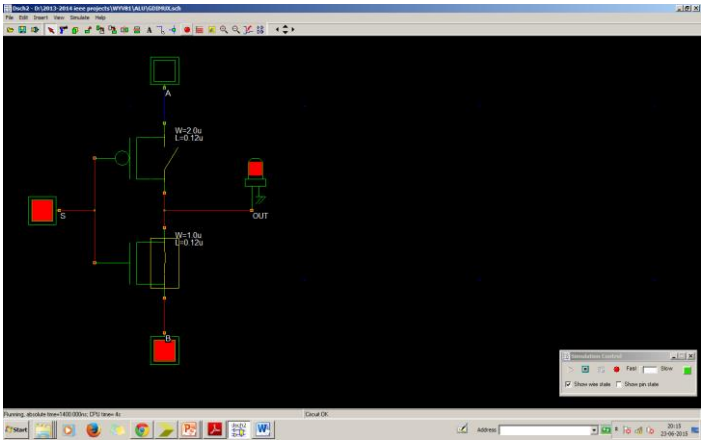

Figure.11 Figure of Simulation design of GDI_MUX

In 5-2 compressor all of the seven inputs have the same weight. This compressor generates an output of the same weight as the inputs, and three outputs cout1, cout2, and weighted one bit binary higher order

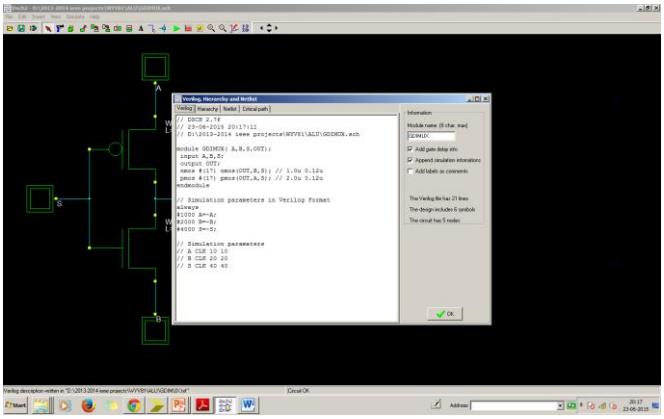

Figure.12 Figure of Simulation design of GDI_MUX

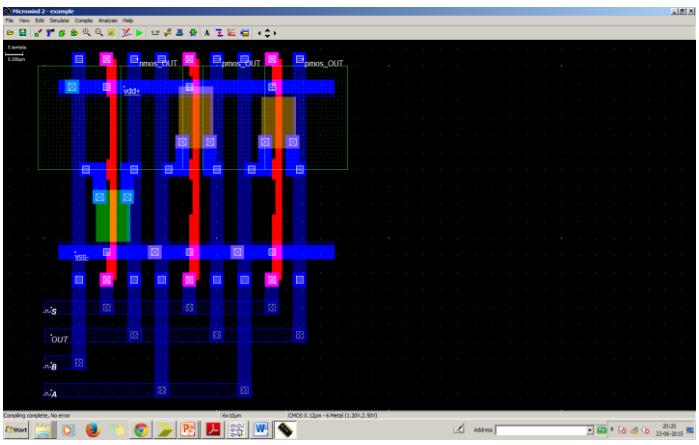

Figure.13 Figure of Layout design of GDI_MUX

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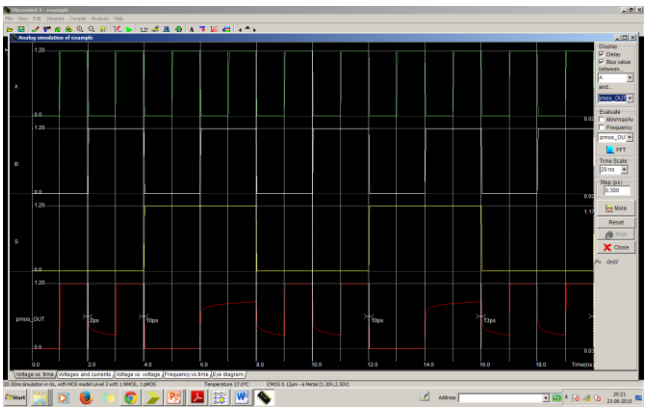

Figure.14 Figure of Simulation design of GDI_MUX

The overall delays of our proposed 7-2 compressor includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors in its critical path which confirms the superiority of our proposed design over prior works [6-11]. Since the output voltage of logics in this architecture keep full swing voltages, so it leads to a fast switching operation. Also, driving problems are decreased considerably by use of logic gates with no

Threshold problems, inverters after So1 and Co1 outputs and a XOR-XNOR gate for E and F signals' generation. Therefore, only two transmission gates (TGs) remain cascaded. If each four TGs is considered as one multiplexer cell (according to the pass transistor logics) the total gate count of our work reaches to 14 logic gates. Also, the sizes of NMOS and PMOS transistors of TGs are considered the same, while initial TGs are considered a little greater in size to avoid driving problems. Based on new arithmetic unit, the proposed architecture is reached to an area-efficiency and is constructed of only 124 transistors. Post layout simulations are performed based on TSMC 0.18 m CMOS technology and 1.8 supply voltage by HSPICE. The layout of the work consumes a small active area at the size of 58.33 m × 38.21 m. All measurements are considered at a frequency of 250MHz. Each input is driven by buffered signals and each output is loaded with buffers. The compressors are running in parallel and the left-side compressor is considered to obtain the simulation results, as an actual simulation environment. For the propagation delay, we have taken the time from input signal reaching 50% to the output signal reaching 50% of the supply voltage. Also, the average power consumption of left-side compressor is considered, by excluding the power consumption of the buffers. The overall latency and the average power consumption are obtained as 470ps and 670 w, respectively. The results are extracted and are tested by 0.18 m CMOS technology by 1.8V supply voltage.

V.CONCLUSION

We presented the design methodologies of a new 7-2 compressor which is developed to be utilized in high speed systems. This architecture is constructed based on a newly designed truth table and based on a sensible combination of pass transistor and static logics. Due to the simple structure and also reduced capacitances of middle stages, the overall delay of proposed design and its power dissipation are decreased. Also utilizing logic circuits with full swing voltages enhances the speed of cascaded operations. According to the critical path of proposed structure, it includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors in its critical path. Utilizing only 14 gates including 124 transistors to implement this circuit admits the proposed design's great area-efficiency in comparison with previous works. Some glitches are observed in the simulation results which consume extra power. This also can be reduced by considering extra circuitry.

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