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Variable Voltage Modular Multilevel DC/DC Converter with Closed Loop Control Technique

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Abstract:

Dc-based distributions and dc-based micro grids are recognized as the promising solutions for future smart-grid systems due to their clear advantages of flexibility for photovoltaic and fuel cells interface, without frequency stability, high conversion efficiency, and easy system control. The Modular Multilevel Converter (MMC) represents an emerging topology with a scalable technology making high voltage and power capability possible. The MMC is built up by identical, but individually controllable sub modules.

The Modular Multilevel Converter (MMC) is a new topology for multilevel converters with potential for medium voltage and high voltage applications. Equivalent Circuit models and dynamic models for the MMC that provide a faithful representation of system behavior are quite complex given the large number of energy states and control variables. They are not particularly useful in studying the terminal behavior of the converter and for the development of an intuitive control approach to regulate power transfer.

A control scheme with a new sub module capacitor voltage balancing method is also proposed in this paper. Modular multilevel converters, based on cascading of half bridge converter cells, can combine low switching frequency with low harmonic interference. They can be designed for high operating voltages without direct series connection of semiconductor element. The high switch voltage stress in the primary side is effectively reduced by the full bridge modules in series. In this project by investigating by investigating the topology derivation principle of the phase-shift-controlled three-level dc/dc converters, the modular multilevel dc/dc converters, by integrating the full bridge converters and three-level flying capacitor circuit, are proposed for the high step-down and high power dc-based systems by using MAT Lab/Simulink.

Index Terms:

Input voltage auto balance, voltage source inverter (VSI), Permanent Magnet Synchronous Generator (PMSG), modular multilevel dc/dc converter, phase-shift control scheme, zero-voltage switching (ZVS).DC motor.

I. INTRODUCTION:

The modular multilevel converters (MMC)-based high voltage direct current (HVDC) system is a new type of voltage source converter (VSC) for medium or high voltage direct current power transmission. Recently, it has become more competitive because it has advantages over normal VSC-HVDC system such as low total harmonic distortion, high efficiency, and high capacity [1, 2]. The operation of the MMC-HVDC system has been investigated by many authors over the world. In [3-5], the authors presented the control strategies for eliminating the circulating currents and maintaining the capacitor voltage balancing of the MMC. The dynamic performances of the MMC-HVDC system have been analyzed in [6]. Similar to other HVDC systems, the stable and reliable operation of the system must be researched carefully, especially when the system operates under fault conditions.

In [6-8], the authors showed out the control methods of the MMC-HVDC system under the unbalanced voltage conditions. Almost all of them only focus on the use of proportional-integral (PI) current controllers in the synchronous rotating reference frame (dq-frame) for enforcing steady-state error to zero. However, the use of these PI current controllers will be difficult under the unbalanced voltage conditions because of the complex control of the positive and negative sequence components of the currents [6-8].Recently, the simple proportional-resonant (PR) current controllers in the stationary reference frame (αβ-frame) have been developed to overcome this problem [10].

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The most important performance of the PR current controllers is that the currents are controlled directly in the αβ-frame. Therefore, the complicated analysis of the positive and negative sequence components of the currents is ignored.In this paper, the flying capacitor and full-bridge converters are combined and integrated to derive the advanced modular multilevel dc/dc converters for the high step-down and high power dc-based conversion applications. Due to the charging and discharging balance of the built-in flying capacitor, the input voltage auto balance ability is naturally realized, which halves the switch voltage stress and overcomes the input voltage imbalance. Furthermore, the phase-shift control strategy can be adopted to achieve the soft-switching operation and reduce the switching losses. The concept of modular multilevel dc/dc converters may provide a clear picture on high-voltage dc/dc topologies for the dc-based distribution and micro grid systems.

II.DERIVATION LAW OF MODULAR MULTILEVEL CONVERTERS:

The derivation process of the proposed modular multilevel dc/dc converters is discussed in this section. It is well known that the neutral-point-clamped (NPC) converters and flying capacitor-based converters are the major multilevel topologies for the high-voltage and high-power applications. For the conventional NPC converters with pulse width modulation control, the abnormal operation condition, such as the mismatch in the gate signals, may cause the voltage imbalance of the input capacitors. Therefore, the converter reliability is impacted. Furthermore, the phase-shift control scheme is not suitable for the conventional NPC converters, which leads to large switching losses. Fortunately, by inserting a small flying capacitor parallel connected with the clamping diodes, the input capacitor voltages are automatically shared because the flying capacitor can be directly parallel with the series input capacitors alternatively.More importantly, the phase-shift control strategy can be easily applied to achieve zero-voltage-switching (ZVS) operation without adding any other power components. The phase-shift controlled three-level dc/dc converter is plotted in Fig. 1(c). From another point of view, the phase-shift-controlled TLC can be regarded as the combination and integration of the three-level NPC converter as given in Fig. 1(a) and the three-level flying capacitor-based circuit as shown in Fig. 1(b), where the input capacitors and active power switches are reused and shared to reduce the circuit complexity.

As a result, the advantages of the NPC converter and flying capacitor-based circuit are kept whereas their inherent disadvantages are effectively avoided. Many further improvements are made for the combined phase shift-controlled TLC by adding some active or passive components to extend the soft-switching operation range.

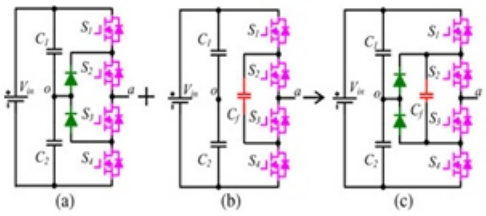

Fig. 1. Derivation of novel TLC: (a) NPC TLC, (b) flying capacitor-based TLC, and (c) phase-shift-controlled combined TLC.

Based on the previously summarized combined multilevel derivation principle, it is innovative and attractive to consider the possibility of combination of the other fundamental multilevel topologies. For example, the cascaded full-bridge converter, or the ISOP full-bridge converter, and the three-level flying capacitor-based converter are combined and integrated to derive the advanced modular multilevel dc/dc converters, which is detailed illustrated in Fig. 2. The time sequence of the leading leg in the phase-shift-controlled full-bridge converters is kept constant and only the phase of the lagging leg is shifted to regulate the output voltage. This indicates that the leading legs of the cascaded full-bridge converter can be assembled with the three-level flying capacitor-based converter to achieve the input voltage auto balance. And the lagging legs of the cascaded full bridge converter are still kept unchanged to provide adequate control freedom to achieve fast and accurate output voltage regulation.

Consequently, for the proposed modular multilevel dc/dc converters, the big concern of the input-voltage imbalance existed in the ISOP converters is completely overcome due to the built-in flying capacitor. More importantly, the derived modular multilevel dc/dc concept can be easily put forward to N-stage converters by stacking the full-bridge power modules in series in the primary side to satisfy the growing bus voltage in the dc-based distribution and micro grid systems. In view of the phase-shift-controlled topologies, the aforementioned optimized strategies for the phase-shifted-controlled TLCs can be directly transferred to the derived modular multilevel dc/dc converters to generate a family of high

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performance topologies for the high-voltage and high-power applications. It can be concluded that this modular multilevel converter concept is one of the general solutions for the high-voltage and high-power dc/dc topology origination.

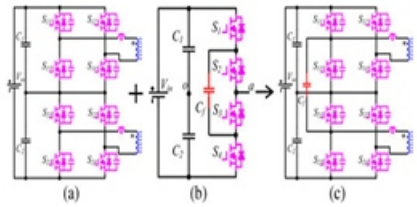

Fig. 2. Derivation of the proposed modular multilevel dc/dc converter: (a) cascaded full-bridge converter, (b) flying capacitor-based TLC, and (c) proposed modular multilevel dc/dc topology.

III.OPERATIONPRINCIPLE AND INPUT-VOLTAGE AUTOBALANCE MECHANISM:

For the secondary side of the derived modular multilevel dc/dc converters, the current-type full-wave rectifier, full-bridge rectifier, current doubler rectifier, and other advanced current-type rectifiers can be employed. In this section, the widely adopted current-type full-wave rectifier is applied as an example to explore the circuit performance of the proposed modular multilevel configuration, which is illustrated in Fig. 3. In the primary side, the capacitors C1and C2are used to split the high input voltage, S11−S14are the power switches of the top full-bridge module, S21−S24form the bottom full-bridge module,Cs11−Cs24are the parasitic capacitors of the power switches, and Llk1and Llk2 are the leakage inductors of the transformersT1andT2, respectively. In the secondary side, Do11,Do12,Lf1, and Co1 are for the top full-bridge module and Do21,Do22,Lf2, and Co2 are for the bottom full-bridge module. ip1,ip2,iDo11,iDo12,iDo21, and iDo22are the primary and secondary currents through the windings of the transformers with the defined direction in Fig. 3. And is1and is2 are the filter inductors currents.

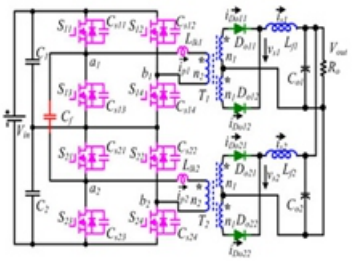

Fig. 3. Proposed modular multilevel dc/dc converter with input voltage auto balance ability.

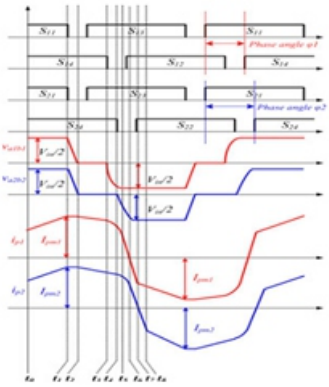

Fig. 4. Key waveforms of the proposed converter

A. Operation Analysis:

The phase-shift control scheme is employed in the proposed converter to realize the ZVS performance of all the power switches, where S11,S13,S21, and S23 are the leading-leg switches and S12,S14,S22, and S24 are the lagging-leg switches. The key waveforms of the proposed converter are shown in Fig. 4. For the top full-bridge module,S11 andS13 act with 0.5 duty cycle complementarily with proper dead time td, so as for the switches S12 andS14. The phase-shift angle between the leading and lagging switch pairs is defined as ϕ1.The gate signal pattern of the bottom full-bridge module is similar to that of the top full-bridge module with the phase-shift angle ϕ2. Meanwhile, the leading switches pair S11 andS13 turns ON and OFF simultaneously with the switch pair S21 andS23, while the phase-shift angles ϕ1 and ϕ2 are decoupled control freedoms for the output voltage regulation. The mode 0 <ϕ1−ϕ2 <td is taken into consideration when analyzing the operation of the converter, and the equivalent operation circuits are depicted in Fig. 5. In order to simplify the analysis, the following assumptions are made: 1) all the power switches and diodes are ideal; 2) the parasitic capacitorsCs11−Cs24of the switches have the same value as Cs; 3) the voltage ripples on the divided input capacitorsC1,C2 and flying capacitors Cf are small due to their large capacitance; 4) the turns ratio of both transformers is N= n2:n1; and 5) the input voltage is balanced and the auto balance mechanism will be depicted later. There are 15 operation stages in one switching period. Due to the symmetrical circuit structure and operation, only the first eight stages are analyzed as follows.

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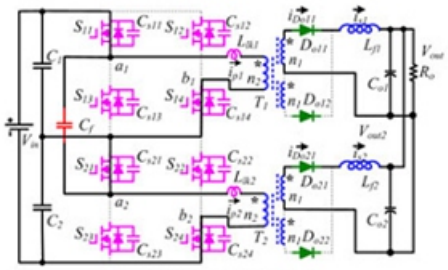
Stage 1 [t0,t1]:Before t1, the switches S11,S14,S21, and S24are in the turn-on state to deliver the power to the secondary side. The output diodesDo11 andDo21 are conducted and the output diodesDo12 andDo22 are reverse biased. The flying capacitor Cf is in parallel with the input divided capacitor C1 to make VCf equal toVC1.

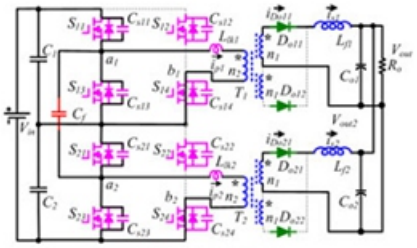
$$i_{p1}(t) = i_{p1}(t_0) + \frac{V_{in}/2 - NV_{out}}{L_{lk1} + N^2 L_{f1}}(t - t_0) \quad (1)$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{V_{in}/2 - NV_{out}}{L_{lk2} + N^2 L_{f2}}(t - t_0) \quad (2)$$



(Stage 1) [t_0-t_1]

Stage 2 [t1,t2]:At t1, the turn-off signals of the switches S11and S21are given. ZVS turn off for these two switches are achieved due to the capacitors Cs11 andCs21. Cs11 andCs21 are charged andCs13 andCs23 are discharged by the primary currents.

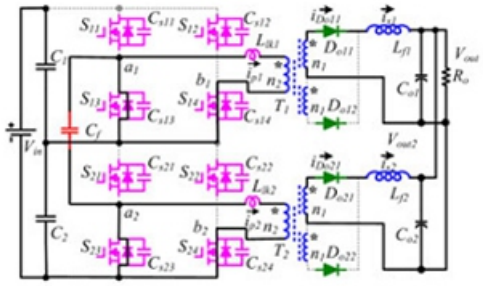


(Stage 2) [t_1-t_2]

Stage3[t2,t3]:At t2, the voltages of Cs13 andCs23 reach 0 and the body diodes ofS13andS23are conducted, providing the ZVS turn-on condition forS13andS23. The flying capacitor Cf is changed to be in parallel with the input divided capacitor C2. The primary currents are derived by

$$i_{p1}(t) = \frac{i_{s1}(t)}{N} \quad (3)$$

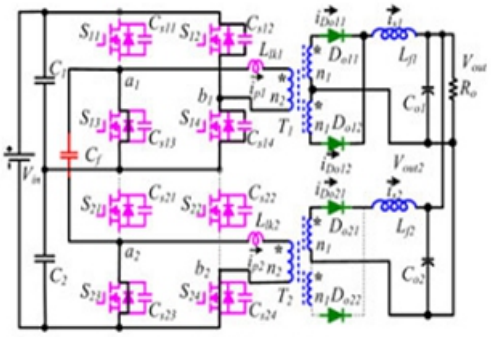
$$i_{p2}(t) = \frac{i_{s2}(t)}{N} \quad (4)$$



(Stage 3) [t_2-t_3]

Stage4 [t3,t4]:At t3,S14turns off with ZVS.Cs14is charged andCs12 is discharged, leading to the forward bias of Do12; hence, the secondary currentis1 circulates freely through both Do11andDo12. ip1is regulated by

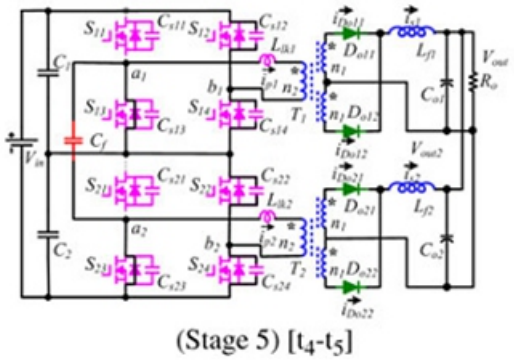
$$i_{p1}(t) = i_{p1}(t_3)\cos\omega(t - t_3) \quad (5)$$



(Stage 4) [t_3-t_4]

Stage 5 [t4,t5]:At t4, the turn-off signal ofS24comes. ZVS turn-off performance is achieved forS24. Similar to the previous time interval, Do21 and Do22 conduct simultaneously, thus leading to the transformer T2 short-circuit. ip2is regulated by

$$i_{p2}(t) = i_{p2}(t_4)\cos\omega(t - t_4) \quad (6)$$



(Stage 5) [t_4-t_5]

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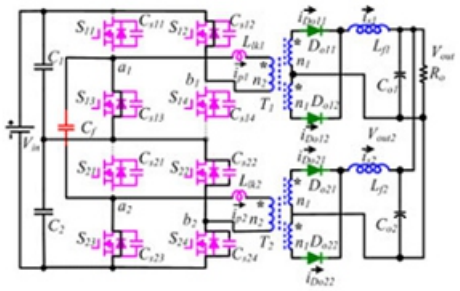
Stage 6 [t5,t6]:Att5,Cs12is discharged completely and the anti parallel diode of S12 conducts, getting ready for the ZVS Turn-on ofS12. During this time interval, ip1 declines steeply duo to half-input voltage across the leakage inductorLlk1. ip1 is given by

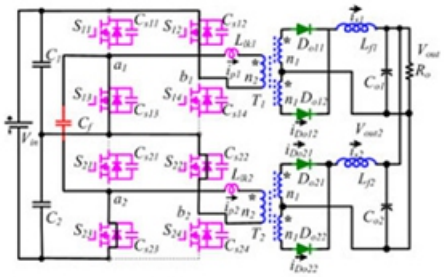
$$i_{p1}(t) = i_{p1}(t_5) - \frac{V_{in}/2}{L_{lk1}}(t - t_5) \quad (7)$$



(Stage 6) [t_5-t_6]

Stage 7 [t6,t7]:At t6,ip1 decreases to 0 and increases reversely with the same slope throughS12 andS13. Cs22 is discharged completely and the anti parallel diode ofS22conducts. ip2 declines rapidly duo to half-input voltage across the leakage inductor Llk2.ip2is given by

$$i_{p2}(t) = i_{p2}(t_6) - \frac{V_{in}/2}{L_{lk2}}(t - t_6) \quad (8)$$



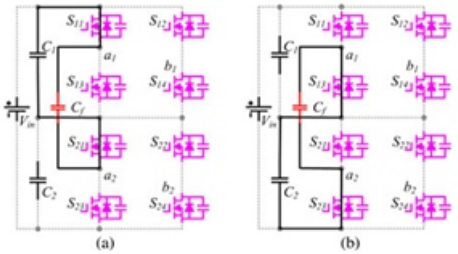
(Stage 7) [t_6-t_7]

Stage 8 [t7,t8]:At t7,ip2 decreases to 0 and increases reversely throughS22 andS23. The current through the output diodeDo11 decreases to 0 and turns off. The output diodeDo21 turns off aftert8, and then a similar operation works in the rest stages.

B. Input Voltage Autobalance Mechanism:

The input voltage imbalance is one of the major drawbacks for most multilevel converters and ISOP converters, which is mainly caused by the asymmetry of the component parameter difference and the mismatch of control signals.

It has been carried out that the transformer turns ratio difference(N), leakage inductance distinction (Llk), and phase-shift angle mismatch (ϕ)are the main reasons for the input voltage imbalance in the steady state for the ISOP phase-shift-controlled converters [18]. The effect of these factors is summarized in Table I, which shows that N1 >N2 orLlk1 >Llk2 orϕ1 >ϕ2 leads to the voltage VC1on the top input capacitorC1higher than the voltageVC2on the bottom capacitorC2and vice versa. As the parameter difference increases, the voltage gap betweenVC1andVC2increases correspondingly.The input voltage auto balance mechanism of the proposed modular multilevel dc/dc converter is displayed in Fig. 6 and detailed elaborated as follows. According to the steady operation of the proposed converter, for the leading-leg switches, the switchesS11andS21have the same time sequence and the switchesS13 andS23 are operated synchronously. WhenS11 andS21 are turned ON,S13 andS23 are turned OFF accordingly, and the flying capacitor Cf is connected in parallel with the top input capacitor C1 as plotted in Fig. 5(a). This makes VCf equal toVc1. In the same way, as given in Fig. 5(b), the flying capacitor Cf is in parallel with the bottom input capacitor C2, whenS13and S23are in turn-on state. This denotes that VCf andVc2 are the same. The connection of Cf with C1 or C2 alternates with high switching frequency, which leads to the voltages on both the input capacitors automatically shared and balanced.It is important to point out that the flying capacitor does not connect with the lagging-leg switches directly. As a result, the operation of Cf hardly affects the states of the lagging-leg switches. Then, both the two phase-shift anglesϕ1 and ϕ2 can be taken as control freedoms to regulate the output voltage.



(a) (b)

Fig. 6. Input voltage autobalance mechanism: (a)Cf in parallel withC1 and(b)Cf in parallel withC2

IV. CONVERTER PERFORMANCE ANALYSIS:

A. Voltage Stresses of Switches

In the primary side, the voltage stress of the power switches S11−S24is half of the input voltage owing to the series structure and the autobalance mechanism.

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As a result, the low voltage-rated power devices are available in the high input applications to restrict the conduction losses.

B. ZVS Soft-Switching Condition:

1) Leading Legs:

ZVS turn-off is achieved for the leading switches due to their intrinsic capacitors. In order to realize ZVS turn-on, enough energy is needed to charge and discharge the intrinsic capacitors. During the dead time interval [t1−t2],S11 andS21 are turned OFF;Cs11 andCs21 are charged andCs13 andCs23 are discharged as shown in Fig. 6. According to the Kirchhoffs law, the following equations are derived:

$$i_{Cs11} + i_{Cs13} = i_{p1} - i_{Cf} \tag{9}$$

$$i_{Cs21} + i_{Cs23} = i_{p2} + i_{Cf} \tag{10}$$

It is reasonable to assume that ip1and ip2 are nearly constant during this period due to the short dead time. When the sum of VCs13 and VCs21 is not equal to VCf, Cf may be charged or discharged. The currentiCfaffects the ZVS performance of the power switches according to (11) and (12): 1) when Cf is discharged, iCf flows in the positive direction as shown in Fig. 7, and ZVS performance of S21 and S23 is improved but deteriorated for S11 andS13; and 2) when Cf is charged, iCf flows reversely, which improves the ZVS performance of S11 and S13but deteriorates that of S21and S23.

Fortunately, Cf is much larger than Cs, making iCf small. Besides, the output filter inductance is reflected to the primary side and is in series with the resonant inductance. The energy of both the filter inductors and the resonant inductors is sufficient to achieve ZVS for the leading switches. The output filter inductance is so large enough that the leading switches can realize ZVS turn-on even at light loads.

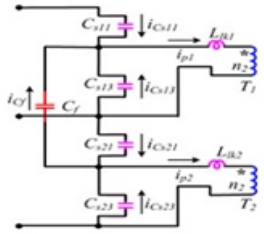

Fig. 6. ZVS equivalent circuit of leading switches during dead time

2) Lagging Legs:

Similar with the leading switches, the lagging switches are able to realize ZVS turn-off by utilizing their intrinsic capacitors. However, only the energies of the resonant inductors are employed to achieve ZVS turn-on for the lagging switches. In order to accomplish ZVS.

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{N}\right)^2 > \frac{1}{2}\cdot 2C_s\left(\frac{1}{2}V_{\text{in}}\right)^2 = \frac{1}{4}C_s V_{\text{in}}^2 \tag{11}$$

As the resonant inductance is quite smaller than the filter inductance, the achievement of the ZVS turn-on for the lagging switches is more difficult than the leading switches at light loads.

C. Duty Cycle Loss:

During interval [t3–t7], Va1b1 is negative, and ip1 transits from the positive direction to the negative reflected filter inductance current. The secondary diodes Do11 andDo12 conduct simultaneously, making the secondary rectified voltage become 0. The duty cycle is lost during this time interval, the expression of which is derived by [31]:

$$D_{\text{loss1}} = \frac{2(t_7 - t_3)}{T_s} \approx \frac{8L_{lk1}I_{o1}}{NV_{\text{in}}}. \tag{12}$$

For the bottom full-bridge module, the duty cycle loss is similar to the top full-bridge module as given by

$$D_{\text{loss2}} = \frac{2(t_8 - t_4)}{T_s} \approx \frac{8L_{lk2}I_{o2}}{NV_{\text{in}}} \tag{13}$$

V. CLOSED LOOP SYSTEM:

Sometimes, we may use the output of the control system to adjust the input signal. This is called feedback. Feedback is a special feature of a closed loop control system. A closed loop control system compares the output with the expected result or command status, and then it takes appropriate control actions to adjust the input signal. Therefore, a closed loop system is always equipped with a sensor, which is used to monitor the output and compare it with the expected result. Fig. 9 shows a simple closed loop system. The output signal is fed back to the input to produce a new output. A well-designed feedback system can often increase the accuracy of the output.

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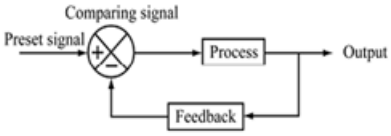

Fig. 9. Block diagram of a closed loop control system

Feedback can be divided into positive feedback and negative feedback. Positive feedback causes the new output to deviate from the present command status. For example, an amplifier is put next to a microphone, so the input volume will keep increasing, resulting in a very high output volume. Negative feedback directs the new output towards the present command status, so as to allow more sophisticated control. For example, a driver has to steer continuously to keep his car on the right track. Most modern appliances and machinery are equipped with closed loop control systems. Examples include air conditioners, refrigerators, automatic rice cookers, automatic ticketing machines, etc. One advantage of using the closed loop control system is that it is able to adjust its output automatically by feeding the output signal back to the input. When the load changes, the error signals generated by the system will adjust the output. However, closed loop control systems are generally more complicated and thus more expensive to make.

Operation of a Closed-Loop Control System:

Most people may not think about control systems in their day to day activities. Control systems are used millions of times a day. Control systems are found in cars, home electronics, power plants, and cities worldwide. The most common type of control system is a closed loop system. The closed loop system consists of five essential processes. The processes are carried out in each basic part of a control system and they are: input transducer, summing junction, controller, plant or process, and the output transducer.

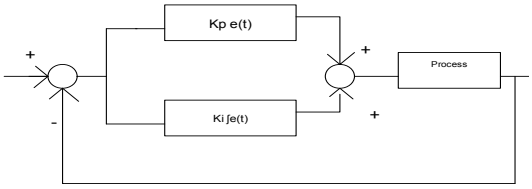

Fig. 10 Diagram of a Closed-loop Control System

The Proportional-Integral (P-I) controller is one of the conventional controllers and it has been widely used. The major features of the P-I controller are its ability to maintain a zero steady-state error to a step change in reference.

A PI Controller (proportional-integral controller) is a special case of the PID controller in which the derivative (D) of the error is not used. The controller output is given by Kp Δ+KI ∫Δdt

The applications of the induction motor are:

Used in Robotics, Billet Shearing Machines, Section Straightening Machines in Rolling mills, Grinding machine, varying load machine, Printing machine, Lathe machine, Drives of fan etc.

VI. SIMULATION RESULTS:

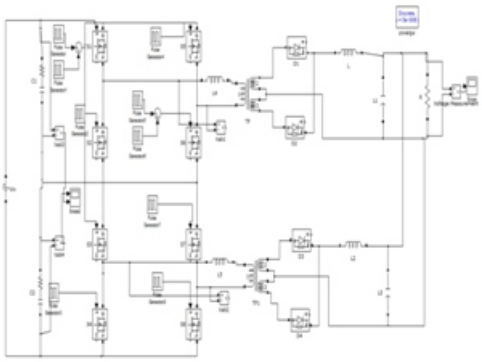

Fig: Matlab/Simulink circuit of proposed system without flying capacitor

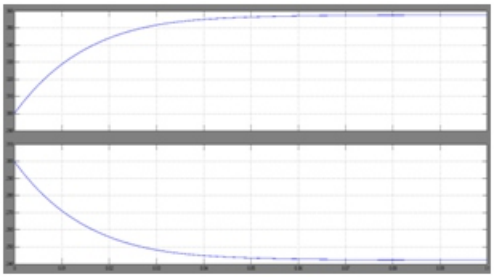

Fig: simulation waveform of proposed system input voltage without flying capacitor

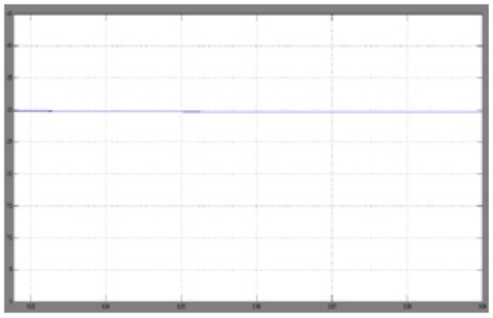

Fig: simulation waveform of proposed system output voltage without flying capacitor

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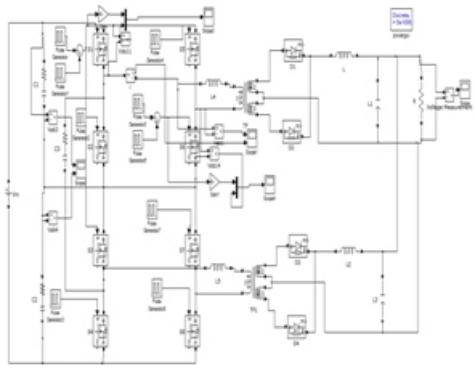

Fig: Matlab/Simulink circuit of proposed system with flying capacitor

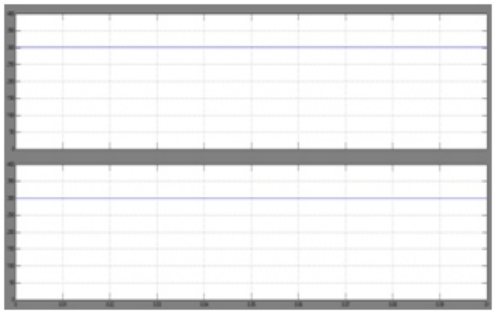

Fig: simulation waveform of proposed system input voltage with flying capacitor

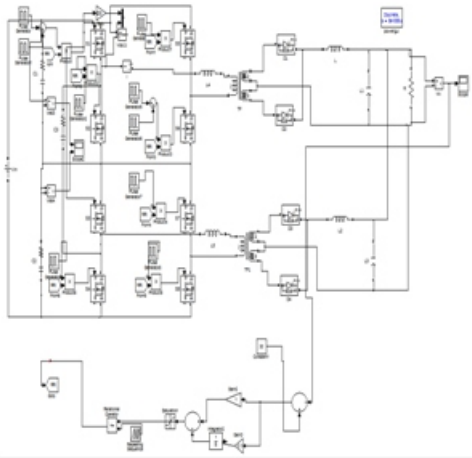

Fig: Matlab/Simulink circuit of closed loop system with flying capacitor

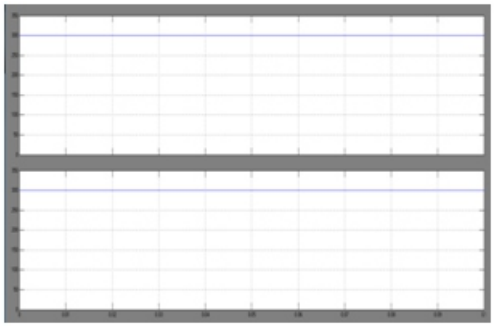

Fig: simulation waveform of input voltage for closed loop system with flying capacitor

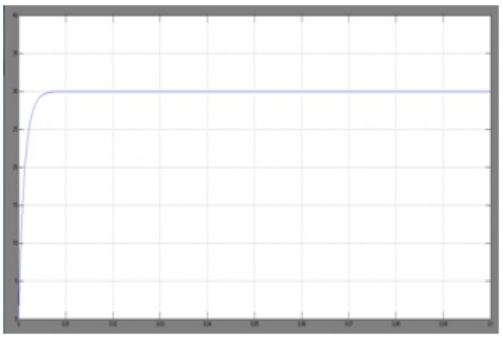

Fig: simulation waveform of output voltage for closed loop system with flying capacitor

VII. CONCLUSION:

In this paper, a novel phase-shift-controlled modular multilevel dc/dc converter is proposed and analyzed for the high input voltage dc-based systems. Due to the inherent flying capacitor, which connects the input divided capacitors alternatively, the input voltage is automatically shared and balanced without any additional power components and control loops. Consequently, the switch voltage stress is reduced and the circuit reliability is enhanced. By adopting the phase-shift control scheme, ZVS soft-switching performance is ensured to reduce the switching losses. The modular multilevel dc/dc converter concept can be easily extended to N-stage converter with stacked full-bridge modules to satisfy extremely high-voltage applications with low-voltage-rated power switches.

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