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Implementation of Crosstalk Elimination Using Digital Patterns Methodology

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Abstract:
In this work, a novel algorithm have been proposed for eliminating opposite transition crosstalk, forbidden pattern crosstalk along with optimized power transition crosstalk. So far in the literature many code books have been discussed based on the Fibonacci series as the code book generated was analyzed a new approach has been proposed for generating the codebook using the correlation graphs. Three methods has been discussed namely Opposite Transition Elimination Crosstalk (OTEE), Slowdown Elimination Crosstalk (SEE), Non Adjacent Crosstalk (NAT) codebook. HDL implementation was done in Xilinx and comparison of bus width vs.lut utilization was plotted in excel.

Keywords ***-Deep Sub-Micron (DSM), crosstalk avoidance code, forbidden transition overlapping codes (FTOCs) and forbidden pattern overlapping codes (FPOCs), 16-level Encoder.***

I. INTRODUCTION

Crosstalk has become a significant problem in deep submicron (DSM) VLSI design. Consider the situation where we scale existing process dimensions by a factor S to obtain a new process. If this scaling is performed in all three dimensions, the cross-sectional area of wires in the design would decrease by a factor .This would result in a quadratic increase in wire resistance, leading to increased wiring delays.

To alleviate this problem, recent processes have avoided scaling the vertical dimension of wires (thus creating “tall “wires). This in turn has led to a situation where the cross-coupling capacitance of adjacent wires on the same layer (CW) is much larger than the capacitance of any wire to the substrate (CS).is much larger than the capacitance of any wire to the substrate (CS). The ratio r = CW/CS was known to be around 10 for a 0.1µm process.

As a result of the large value of r, crosstalk between adjacent wires on the same metal layers manifests in ways that make designs unpredictable. It results in a significant delay variation and possible integrity problems. As a result, crosstalk has become a critical design consideration. The detrimental effects of crosstalk are aggravated in long on chip buses, since bus signals are typically driven at minimum pitch for long distances. The focus of this paper is the selective reduction of the delay variation effect in buses (and therefore the reduction in maximum delay and signal integrity problems in the bus signals as well) due to crosstalk. We do this by developing design techniques that allow the designer to trade-off the degree of crosstalk control desired with the associated area

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overhead has been shown that reducing the cross talk boosts the bus performance significantly [3]. Different approaches have been proposed for cross talk reduction in the context of bus interconnects. Some schemes focus on reducing the energy consumption, some focus on minimizing the delay and other schemes address both. The simplest approach to address the inter-wire cross talk problem is to shield each signal using grounded conductors. Sincetheworstcasecrosstalkisaresultofsimultaneoustransitionofdatabitsinsynchronousbusses,skewingoftransitiontimesofadjacentbitscanalleviate the crosstalk effect. Using the techniquethatintentionallyintroducestransitiontimeskewingcanpreventsimultaneousoppositetransitionsbetweenadjacentwiresandconsequentlyreducetheworstcasebus delay.trade-off the degree of crosstalk control desired with the associated area overhead.

II. BACKGROUND

Crosstalk consists in transmitting unwanted energy from one trace to an adjacent one, whenever the electromagnetic field lines that surround the traces interact. The main detrimental effects caused by crosstalk consist in changing the performances of the transmission lines by modifying the effective characteristic impedances and propagation velocity which is showed in fig 1. On the other hand, through electromagnetic coupling is also induced noise into parallel bus lines, degrading the signal integrity and reducing noise margins. As a result on a parallel data bus line the signals are affected by crosstalk glitch and crosstalk delay. Crosstalk glitch is represented by a voltage overshoot that appears on a trace that should have a steady value, when one or more lines are switching. Crosstalk delay is caused by the parasitic capacitances produced by the electric field lines that close on the bus traces. In order to reduce the closing of electromagnetic field lines on adjacent traces can be used two physical solutions: increase the distance between traces or insert shield traces. The only detrimental effect is consisting in increasing the parallel bus area. Beside the physical methods, another approach is to develop a channel coding algorithms that try to mitigate crosstalkproblems.

Depending on the coding rules, the algorithm can reduce the number of transitions when sending a new symbol, or preventing specific switching patterns. By reducing the number of transitions there is reduced the number of parasitic capacitances charge/discharge when sending new information. As a result reduced the energy needed in sending information. A crosstalk avoidance code (CAC) should not have the goal to reduce bus energy, but instead should try to avoid crosstalk glitch and delay as much as possible. The main goal of the CAC should consist in guaranteeing an error free transmission. The CACs presented in many papers are developed for deep submicron structures, where the values for the parasitic elements are much smaller compared to an off-chip parallel bus structure. Because for on-chip structures the capacitance has a greater impact, usually the coding algorithm are taking into account only the capacitive coupling. The magnetic field lines can manifest their influence on traces placed further apart, modifying the coding rules implemented in the CAC.

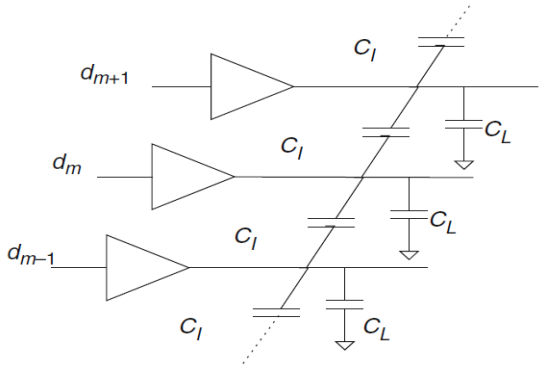

Fig1.BusModelCrosstalk

The rest of the paper is follows section 3 describes the three methods proposed along with a numerical example related to Fibonacci series .section 4 deals with the simulation results and revelent input and output is discussed below the simulation figure. section 5 discuss about the conclusion and future scope of the project

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III. PROPOSED METHOD

1. OTEE CODEC

Opposite transition elimination encoding is the codec does not contain the forbidden pattern in oppositetransition10 & 01.the correlation graph is shown in the fig 2 .the Fibonacci algorithm is drawn at fig 3(a) and fig 3(b).the Xilinx simulation result is shown in fig 7.

Correlation Graph

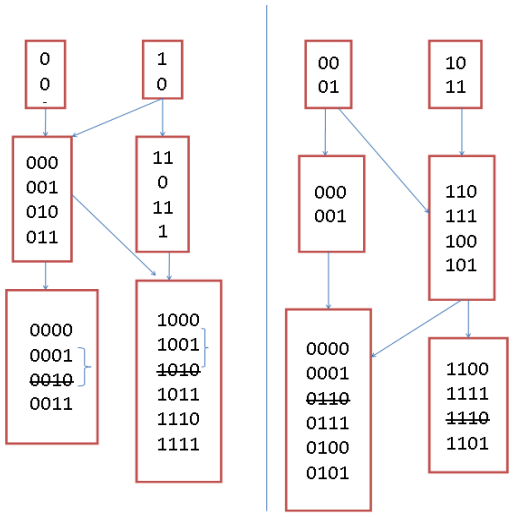

Fig2.correlation graph of OTEE Fibonacci algorithm

OTEE encoder & decoder block is implemented by using fibonaciiseries.Herefibonacii series used is3 2 11.TheXilinx simulation result is shown in fig 8.

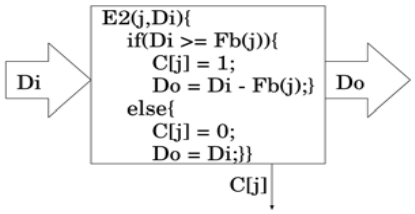

Fig 3(a): encoder of otee

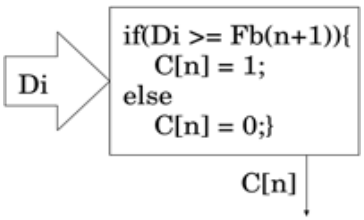

Fig 3(b): decoder of OTEE

Numerical Example

Case(i):
$D_i = 6$
fb(j) = 5
6 >= 5 (yes),then
$C_j = 1$
$D_0 = 6-3 = 3$

Case (ii):
3 >= 3 (YES),then
$C_j = 1$
$D_0 = 3-2 = 1$

Case(iii):
1 >= 2 (No),then
$C_k = 0$

Case (iv):
1 >= 1 (Yes),then
$C_K = 1$

The above numerical example is developed on Fibonacci series .the j is the number of input bits of considered bus width. The j series Fibonacci number is considered for algorithm. Comparison of input data with series is done which results the resultant binary and the other represents the next input for the successive comparison.

2. NAT CODEC

Non adjacent codec minimizes the power of transmission by reducing the number of one's in the transition .the codec correlation graph is shown in fig 4 .as well its Fibonacci algorithm is mentioned in fig5(a) and decoding 5(b).

Correlation Graph

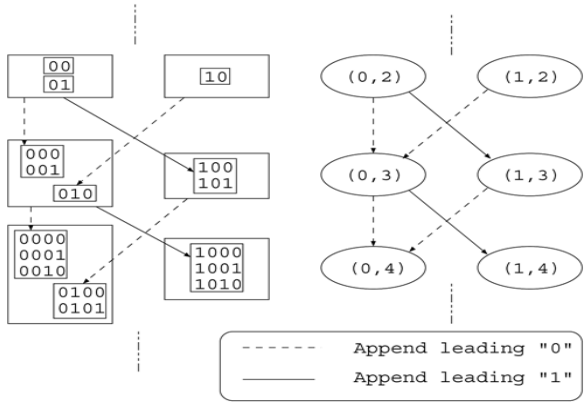

Fig 4.correaltion graph of NAT encoding

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Fibonacci Algorithm

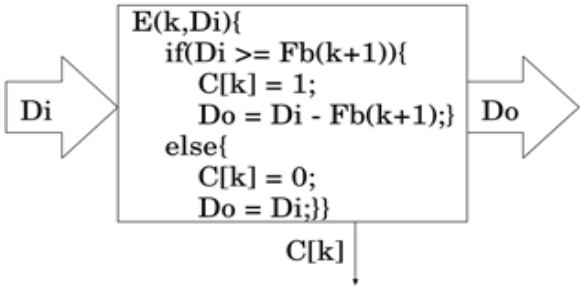

Fig 5(a):Encoder of NAT

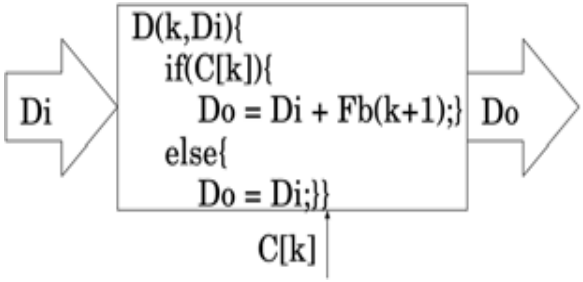

Fig 5(b):Decoder of NAT

Numerical Example

Case(i):

$D_i = 6$

$f_{m+1} = 5$

6 >= 5 (yes),then

$C_k = 1$

$D_0 = 6-5 = 1$

Case (ii):

1 >= 3 (N0),then

$C_k = 0$

Case(iii):

1 >= 2 (No),then

$C_k = 0$

Case (iv):

1 >= 1 (Yes),then

$C_K = 1$

3. SEE CODEC

Slowdown elimination codec is to remove the forbidden pattern containing 101 and 010 .as the crosstalk was discussed in section 2.the corelation graph was mentioned in the fig 6.the code in discussed in the results section. The xilinx simulation result is shown in fig 9.

Correlation Graph

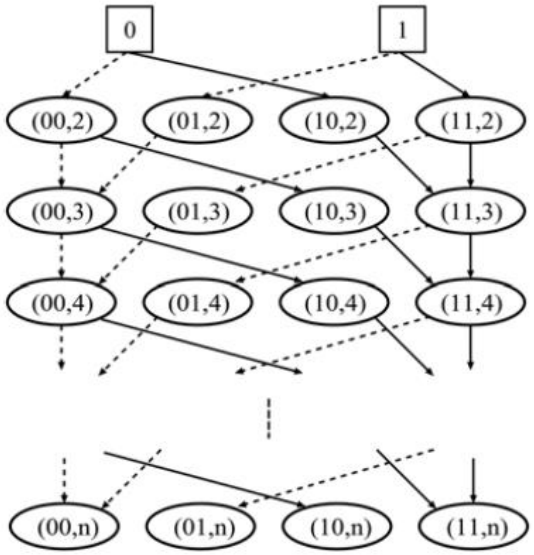

Fig 6 correlation graph of SEE

IV. SIMULATION RESULTS

OTEE Simulation

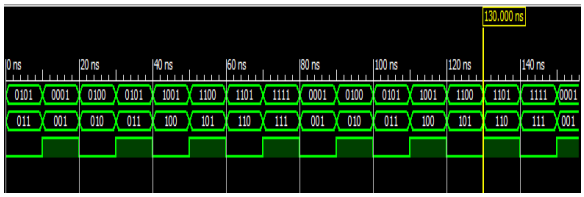

Fig 7. Simulation of OTEE for all the 3input bus inputs

NAT Simulation

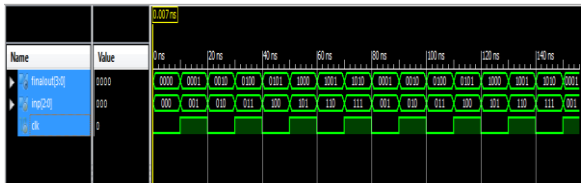

Fig 8. Simulation of the NAT encoding for all the 4 input bus

SEE Simulation

Fig 9 simulation result for the SEE encoding for 6 as given input

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Number of luts	Correlation graph	Fibonacci
OTEE	5	8
NAT	43	90
SEE	8	12

Table 1. LUT report for correlation graph and Fibonacci

V. CONCLUSION AND FUTURE SCOPE

The three methods stated OTEE,NAT,SEE were implemented in xilinxand the synthesized report has been generated .the synthesis was done for 4 input data bus .the lut count increases for certain extent of bus width but later the count remains constant as the Fibonacci series has an exponential increase.

FUTURE SCOPE

Further implementation can be processed to decrease the delay .as the front end process has been accurately designed the backend process i.ecmos design is to be concentrated

REFERENCES :

[1] C. Duan, V. H. C. Calle, and S. P. Khatri, "Efficient on-chip crosstalk avoidance CODEC design," IEEE Trans. Very Large Scale Integr. Syst., vol. 17, no. 4, pp.551–560, Apr. 2009.

[2]M. Ghoneima and Y. Ismail, "Delayed line bus scheme: A low-power bus scheme for coupled on-chip buses," in Proc. ISLPED, Aug. 2004, pp. 66–69.

[3] P. Subrahmanya, R. Manimegalai, V. Kamakoti, and M. Mutyam, "A bus encoding technique for power and crosstalk minimization," in Proc. 17th Int. Conf. VLSI Design, 2004, pp. 443–448.

[4] K.-C. Cheng and J.-Y. Jou, "Crosstalk-avoidance coding for low-power on-chip bus," in Proc. 15th IEEE Int. Conf. Electron. Circuits Syst., Aug.–Sep. 2008, pp.1051–1054.

[5] Inter-Wire Coupling Reduction Analysis of Bus-Invert Coding Rung-Bin Lin, Member,IEEE Int. conf. Electron. Circuits Syst., ..2008.

[6] C. Duan, C. Zhu, and S. Khatri, "Forbidden transition free crosstalk avoidance codec design," in Proc. Design Autom. Conf., 2008, pp.986–991.

[7] M. Mutyam, "Preventing crosstalk delay using Fibonacci representation," inProc. IEEE Int. Conf. VLSI Design, 2004, pp. 685–688.

[8]C. Duan, A. Tirumala, and S. Khatri, "Analysis and avoidance of crosstalk in on-chip buses," in Proc. Hot Interconnects, 2001, pp.133–138.

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