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Sharing the Information of the Wireless Scanner Network among Different Embedded Systems


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ABSTRACT:

Technological advancements in the silicon industry, as predicted by Moore's law, have enabled integration of billions of transistors on a single chip. To exploit this high transistor density for high performance, embedded systems are undergoing a transition from single-core to multi-core. Although a majority of embedded wireless sensor networks (EWSNs) consist of single-core embedded sensor nodes, multi-core embedded sensor nodes are envisioned to burgeon in selected application domains that require complex in-network processing of the sensed data. In this paper, we propose an architecture for heterogeneous hierarchical multi-core embedded wireless sensor networks (MCEWSNs) as well as an architecture for multi-core embedded sensor nodes used in MCEWSNs.

We elaborate several compute-intensive tasks performed by sensor networks and application domains that would especially benefit from multi-core embedded sensor nodes. This paper also investigates the feasibility of two multi-core architectural paradigms Symmetric multiprocessors (SMPs) and tiled many-core architectures (TMAs)V for MCEWSNs. We compare and analyze the performance of an SMP (an Intel-based SMP) and a TMA (Tilera's TILEPro64) based on a parallelized information fusion application for various performance metrics (e.g., runtime, speedup, efficiency, cost, and performance per watt). Results reveal that TMAs exploit data locality effectively and are more suitable for MCEWSN applications that require integer manipulation of sensor data, such as information fusion, and have little or no communication between the parallelized tasks. To demonstrate the practical relevance of MCEWSNs, this paper also discusses several state-of-the-art multi-core embedded sensor node prototypes developed in academia and industry. We further discuss research challenges and future research directions for MCEWSNs.

Index-terms:

Processor, sensors, zigbee module, LCD display embedded technology.

I. PROJECT RELATED WORK:
1.1 BLOCK DIAGRAM:
1.1.1 BLOCK DIAGRAM OF TRANSMITTER SECTION:

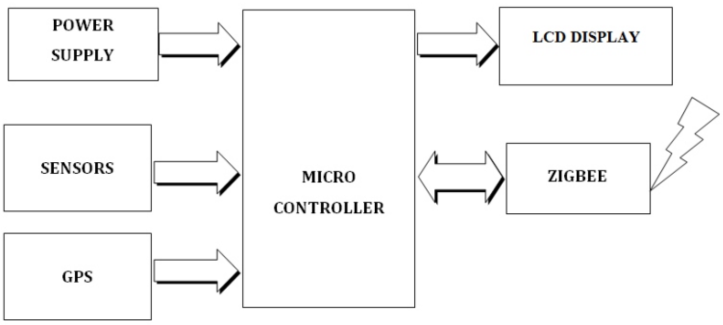

Fig 1. Block Diagram of transmitter section

1.1.2 Block Diagram of Receiver Section

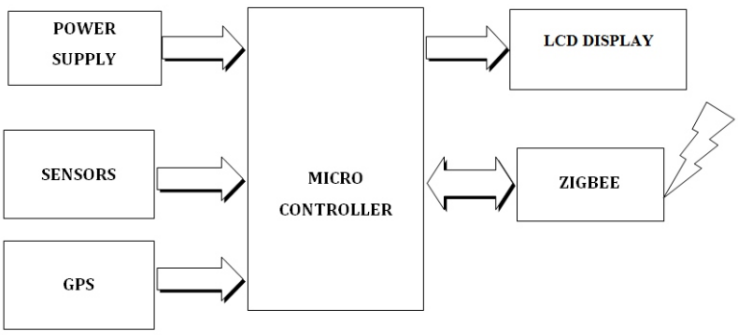

Fig 2. Block Diagram for Receiver Section

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1.1.3 MONITORING SECTION:

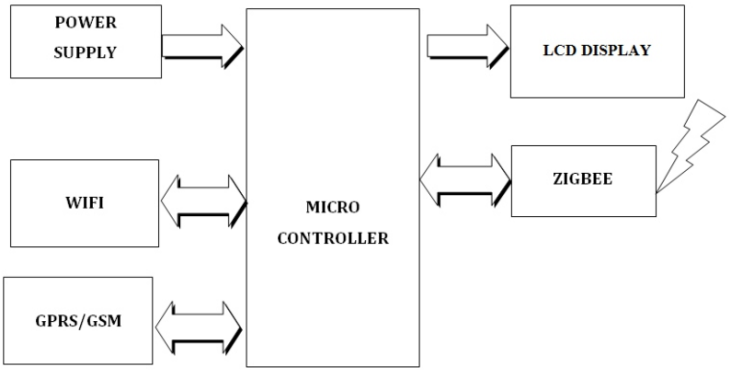

Fig 3. Monitoring Section

1.2 ARM PROCESSOR:

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the in¬struction set and related decode mechanism are much simpler than those of micro programmed Complex Instruc¬tion Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time inter¬rupt response from a small and cost-effective processor core. Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory. The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume ap-plications with memory restrictions, or applications where code density is an issue. The key idea behind Thumb is that of a super-reduced instruction set.

II. HARDWARE COMPONENTS:

2.1 ZIGBEE Technology:

ZIGBEE is the only wireless standards-based technology that addresses the unique needs of remote Sensors and controls don't need high bandwidth but they do need low latency and very low energy consumption for long battery lives and for large device arrays. There are a multitude of standards that address mid to high data rates for voice, PC LANs, video, etc. monitoring and control, sensory network applications.

However, up till now there hasn't been a wireless network standard that meets the unique needs of sensors and control devices. There are a multitude of proprietary wireless systems manufactured today to solve a multitude of problems that also don't require high data rates but do require low cost and very low current drain. These proprietary systems were designed because there were no standards that met their requirements. These legacy systems are creating significant interoperability problems with each other and with newer technologies.

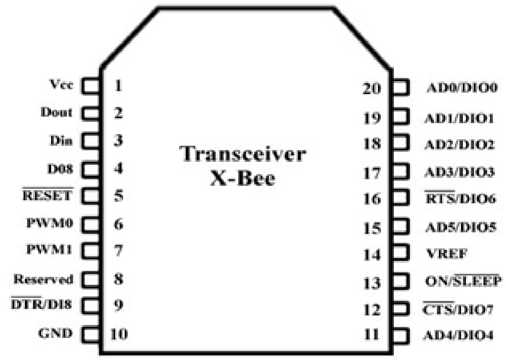

Fig: 4 Pin diagram of X-Bee Transceiver

2.2 GPS TECHNOLOGY:

The Global Positioning System (GPS) is a U.S. space-based global navigation satellite system. It provides reliable positioning, navigation, and timing services to worldwide users on a continuous basis in all weather, day and night, anywhere on or near the Earth. GPS is made up of three segments: Space, Control and User. The Space Segment is composed of 24 to 32 satellites in Medium Earth Orbit and also includes the boosters required to launch them into orbit.

The Control Segment is composed of a Master Control Station, an Alternate Master Control Station, and a host of dedicated and shared Ground Antennas and Monitor Stations. The User Segment is composed of hundreds of thousands of U.S. and allied military users of the secure GPS Precise Positioning Service, and tens of millions of civil, commercial and scientific users of the Standard Positioning Service (see GPS navigation devices). GPS satellites broadcast signals from space that GPS receivers use to provide three-dimensional location (latitude, longitude, and altitude) plus precise time.

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2.3 LIQUID CRYSTAL DISPLAY:

Fig 5: Liquid crystal display

A model described here is for its low price and great possibilities most frequently used in practice. It is based on the HD44780 microcontroller (Hitachi) and can display messages in two lines with 16 characters each. It displays all the alphabets, Greek letters, punctuation marks, mathematical symbols etc. In addition, it is possible to display symbols that user makes up on its own. Automatic shifting message on display (shift left and right), appearance of the pointer, backlight etc. are considered as useful characteristics.

III. OUTPUT:

In this section, we present performance and performance per watt results for the two multi-core architectures (SMPs and TMAs) that can be used in MCEWSNs. For the SMP architecture, we evaluate an eight-core Intel-based SMP consisting of two Intel Xeon E5430 quad-core processors fabricated at 45 nm CMOS lithography with a maximum clock frequency of 2.66 GHz . For conciseness, we will refer to this SMP as SMP2_QuadXeon in the remainder of this paper. Results in this paper focus only on parallelization to demonstrate the performance and performance per watt advantages that can be attained by leveraging multi-core embedded sensor nodes. Implementation of a complete MCEWSN architecture (Fig. 1) for real world applications, such as video surveillance, is a focus of our future research work.

Considering the significance of information fusion for EWSNs, we parallelize an information fusion application both for SMPs and TMAs to investigate the suitability of the two architectures for MCEWSNs. We analyze an information fusion application as an example to demonstrate the performance and performance per watt advantages of multi-core embedded sensor nodes as compared to single-core embedded sensor nodes, although other sensor applications can be parallelized to demonstrate similar advantages.

IV. FUTURESCOPE:

•By adding GRS and WIFI we can check the water flow in paddy fields
•By using GPS we can check weather in wells
•And also we can add Zigbee

V. CONCLUSION:

The project "SHARING THE INFORMATION OF THE WIRELESS SCANNER NETWORK AMONG DIFFERENT EMBEDDED SYSTEMS" has been successfully designed and tested. Integrating features of all the hardware components used have developed it. Presence of every module has been reasoned out and placed carefully thus contributing to the best working of the unit. Secondly, using highly advanced IC's and with the help of growing technology the project has been successfully implemented.

VI. REFERENCES:

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