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Renewable Energy Based Three Level Diode Clamped Inverter with Minimum Losses for Induction Motor Control Application

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ABSTRACT:

To minimize the power demand and scarcity we have to improve the power extracting methods. Multilevel inverter is used to extract power from solar cells, fuel cells and batteries. It synthesizes the desired ac output waveform from several dc sources. This paper presents a three phase multilevel inverter topology that uses for IM control with minimum total harmonic distortion. To achieve a better voltage utilization and harmonics reduction, Multicarrier Phase Shift Pulse Width Modulation control technology is used inverter provides higher output quality with relatively less harmonics losses and THD as compared to the other conventional inverters. Working of the present topology is explained and finally results are analyzed by MATLAB/SIMULINK software.

I. INTRODUCTION:

I N RECENT years, there has been an increasing interest in electrical power generation from renewable-energy sources, such as photovoltaic (PV) or wind-power systems [1], [2]. The benefits of power generation from these sources are widely accepted. They are essentially inexhaustible and environmentally friendly. Among the different renewable-energy sources possible to obtain electricity, solar energy has been one of the most active research areas in the past decades, both for grid-connected and stand-alone applications [3]–[9]. Carrier-based NPP regulator for a three-level diode clamped inverter in conjunction with a closed-loop controller can be operated with an input DC from PV system.

This NPP regulator has good performance in terms of
•Reduced THD
•Improved NPP harmonic profile,
•Balanced dc link with almost zero average NPP
Large utility-scale solar parks or farms are power stations and capable of providing an energy supply to large numbers of consumers.

Generated electricity is fed into the transmission grid powered by central generation plants (grid-connected or grid-tied plant), or combined with one, or many, domestic electricity generators to feed into a small electrical grid (hybrid plant). In rare cases generated electricity is stored or used directly by island/standalone plant. PV systems are generally designed in order to ensure the highest energy yield for a given investment.

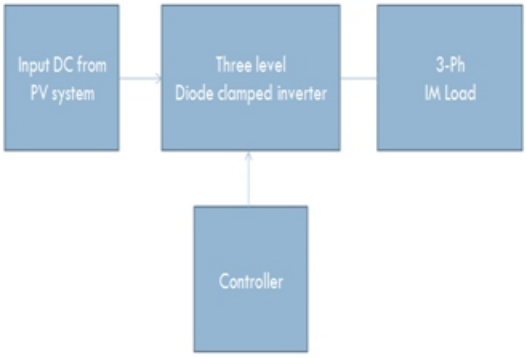

Fig1.Proposed System Block Diagram

SOLAR SYSTEM:

The installed PV power has been increasing in the past, and a more significant increase is expected in the near future, owing to the potential advances in the PV conversion technology and the reduction in cost-per watt that a large-scale production will bring about [10]. The exponential rate of growth in the worldwide cumulative PV capacity since 1992 is mainly due to grid-connected applications. A solar cell basically is a p-n semiconductor junction. When exposed to light, a current proportional to solar irradiance is generated. Standard simulation tools utilize the approximate diode equivalent circuit shown in Fig. 1 in order to simulate all electric circuits that contain diode. The circuit consists of Ron in series with voltage source Von. PVs generate electric power when illuminated by sunlight or artificial light, the absorption of photons of energy greater than the band-gap energy of the semiconductor promotes electrons from the valence band to

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the conduction band, creating hole-electron pairs throughout the illuminated part of the semiconductor. These electrons and holes pairs will flow in opposite directions across the junction thereby creating DC power. Figure 1: circuit model of PV cell.

2.1 Mathematical Model:

The equation [1] & [2] that are used to solve the mathematical model of the solar cell based on simple equivalent circuit shown in Fig. 1, are given below;

$$I_D = I_O\left[e^{\frac{q(V+IR_s)}{KT}} - 1\right] \quad (1)$$

$$I = I_L - I_O\left[e^{\frac{q(V+IR_s)}{KT}} - 1\right] - \frac{(V+IR_s)}{R_{sh}} \quad (2)$$

Where:
I is the cell current in (A).
q is the charge of electron = 1.6x10-19 (coul).
K is the Boltzmann constant (j/K).
T is the cell temperature (K).
IL is the light generated current (A).
I0 is the diode saturation current. ,
Rs, Rsh are cell series and shunt resistance (ohms).
V is the cell output voltage (V).

Diode clasped/Neutral point clipped multilevel inverter innovation has risen as of late as an essential option in the range of high-power medium voltage vitality control. The structure of diode braced inverters permits them to achieve high voltages and consequently lower voltage rating gadgets can be utilized. As the quantity of levels builds the orchestrated yield waveform has more steps creating a fine stair case wave and drawing nearer nearly to the sought sinusoidal wave.

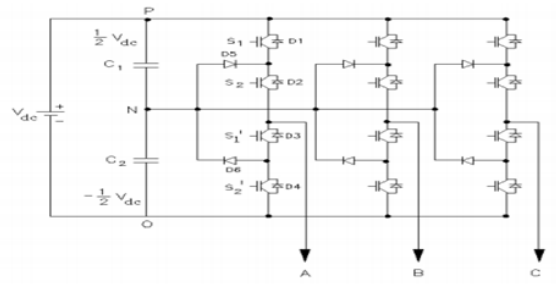

Figure 1. Three Level Diode Clamped Inverter

Thus diode braced multilevel inverters offer a superior decision at a powerful end in light of the fact that the high volt-ampere evaluations are conceivable with these inverters without the issues of high dv/dt and the other related ones. NPC inverter has an inborn issue of uneven voltages crosswise over dc-join capacitors because of burden unbalancing, non uniform conveyance of charges, and non-indistinguishable properties of dc-connection capacitors gave from the producer [1], [2]. A few open circle procedures have been proposed for the lessening of the symphonious substance [3], [4]. The creators have proposed two methods for mid-point voltage adjusting in NPC three level inverters. Restricted of voltage adjusting based upon the expansion or change of equipment hardware to the inverter [5]-[10] which alter the charging and releasing streams of DC-connection capacitorsSecond method for voltage adjusting is based upon change in inverter control methodology in view of PWM plans. Numerous bearer and SVPWM based methodologies have been proposed for the adjustment of propositions inverters [11]-[15].

S. No	Switching States				Switching States	Output Phase Voltage (Vao)
	Sa1	Sa2	S'a1	S'a2		
1	1	1	0	0	+	+(V/2)
2	0	1	1	0	0	0
3	0	0	1	1	-	-(V/2)

Table 1: Switching states of three level NPC inverter

A shut circle control method, which diminishes the consonant substance and additionally keeps up voltage soundness in the impartial point, is displayed in this paper. Shut circle controller is in view of infusing balance extent to the tweaking flag as an element of a control enter that amends any current unevenness. In this paper primary contemplations given to manage the voltage irregularity of NPC inverter utilizing sine triangle modulator in conjunction with a shut circle controller, which significantly diminishes the symphonious contortions in the yield voltage waveform, bringing about decrease of the obliged dc transport capacitance.

II. NEED OF NEUTRAL POINT BALANCING:

The Neutral point braced inverter is indicated in Fig.1 and Table I give the changing states to produce the three level yield voltage for stage U.

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Because of unequal voltages over two dc-join capacitors PWM inverter yield voltage and yield current waveforms get bended. Unbalance DC connection makes expanded voltage weight on exchanging gadgets. Expanded voltage irregularity crosswise over dc-join capacitors may bring about disappointment of gadgets. Thusly, Neutral point voltage adjusting control is essential without relinquishing the consonant execution of the inverter. Fig. 2 demonstrates the waveforms and symphonious ranges of stage voltage and line voltage under burst state of huge awkwardness at dc join with Vdc1 = 200 V and Vdc2 = 400 V. Under this condition, the dc segment and even-arrange music are more huge which are risky for drive and different applications.

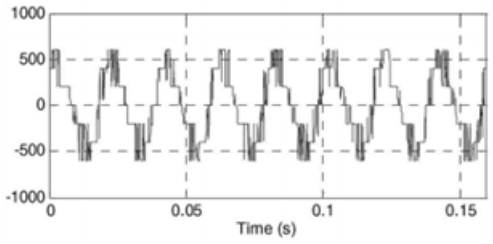

Fig. 2 Output line voltage distortions due to unbalanced DC-link voltage

For this study, the dc connection was deliberately made lopsided. It is clear that the line voltage THD will have the base quality for adjusted dc connection and they are expanding with expanded unbalancing.

III. DESIGN OF CLOSED LOOP NPC INVERTER:

Planning of shut circle NPC inverter consider the accompanying imperative perspectives,

i) guaranteeing dc-join capacitor, voltage adjusting and controlling dc-join voltage

ii) minimization of inverter voltage and current music;

iii) guaranteeing less and uniform exchanging weight on exchanging gadgets, bringing about lessened exchanging misfortunes. Fig.3 NPC offset addition PWM block diagram.

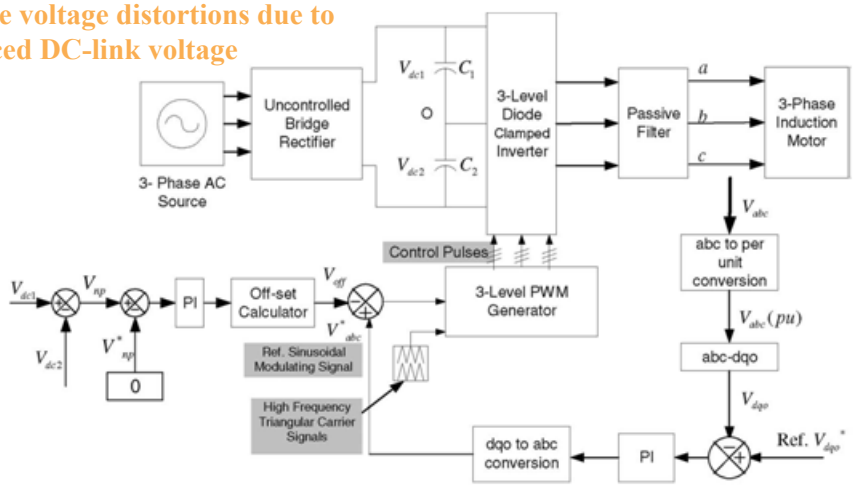

Fig. 3 shows the complete block diagram of the NPC offset addition PWM.

It comprises of both a dc-join voltage control circle and a heap voltage control circle. Three stage load voltages are detected and changed over into a for each unit framework. These per-unit voltages are changed over into dqoaxis. In the wake of contrasting and preset qualities (Vd=1,Vq=0) again changed over to abc-signal. This Vabc sign is included with the dc-join voltage control circle created counterbalance signal. This sign is going about as regulating sign. It is contrasted and bearer PWM by utilizing level movement PWM and the beats are given to fitting switches. Fig.4 abc to dqo change reference examination and dqo to abc transformation Fig demonstrates the deliberate voltage Vabc is changed over by utilizing the abc to dqo conversation strategy utilizing the accompanying three-stage to two-stage change:

Vd = 2/3[Va sin (ωt) +Vb sin (ωt − 120o) + Vc sin (ωt − 240o)]

Vq= 2/3[Va cos(ωt)+Vb cos(ωt − 120o)+Vc cos(ωt − 240o)]

Vo= Va+ Vb +Vc

These dqo voltages Vdqo are contrasted and preset estimations of dqo voltages. It brings about voltage lapse which is handled through a PI controller to create two hub charge signals V*dqo. At that point, three-stage reference voltage signs are combined utilizing the accompanying two phase to three-stage change:

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Va= Vd sin (ωt) + Vq cos(ωt) + Vo)
Vb = Vd sin (ωt − 1200) + Vq cos(ωt − 1200) + Vo)
Vc = Vd sin (ωt − 2400) + Vq cos(ωt − 2400) + Vo)
These are the reference sinusoidal tweaking sign Vabc. The plentifulness tweak file m is characterized as m = √Vd 2 + Vq 2
balance expansion system is indicated in Fig. to the reference sinusoidal sign. The contrasted sign is given with switches.

INDUCTION MOTOR:

In recent years the control of high performance induction motor drives for general industry applications and production automation has received widespread research interests. Induction machine modeling has continuously attracted the attention of researchers not only because such machines are made and used in largest numbers but also due to their varied modes of operation both under steady and dynamic states. Three phase induction motors are commonly used in many industries and they have three phase stator and rotor windings.

The stator windings are supplied with balanced three phase ac voltages, which produce induced voltages in the rotor windings due to transformer action. It is possible to arrange the distribution of stator windings so that there is an effect of multiple poles, producing several cycles of magneto motive force (mmf) around the air gap. This field establishes a spatially distributed sinusoidal flux density in the air gap. In this paper three phase induction motor as a load. The equivalent circuit for one phase of the rotor is shown in figure. 12.

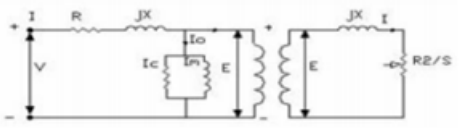


Figure 12: Steady state equivalent circuit of induction motor.

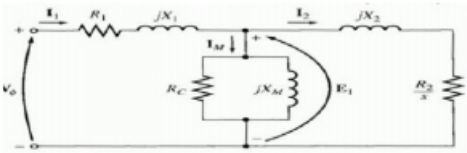


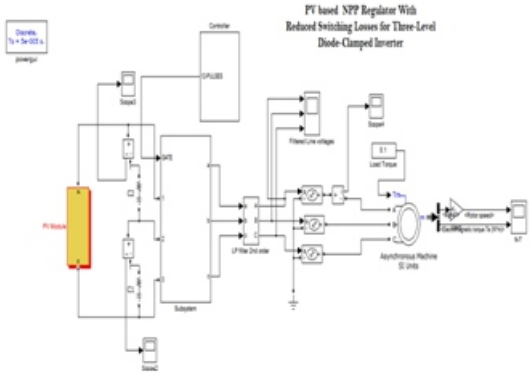
Figure 13: Equivalent circuit refers to stator side.

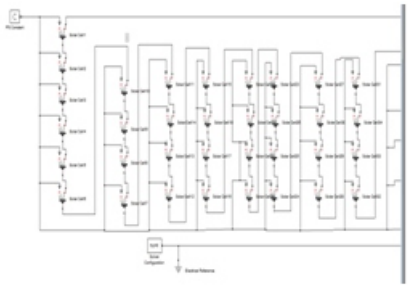
The rotor current is

$$I_r = \frac{sE_r}{R_r + jX_r} = \frac{E_r}{\frac{R_r}{s} + jX_r}$$

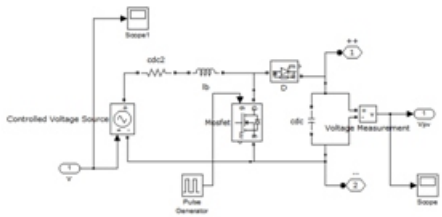
The complete circuit model with all parameters referred to the stator is in figure. 13. Where Rs and Xs are per phase resistance and leakage reactance of the stator winding. Xm represents the magnetizing reactance. R'r and X'r are the rotor resistance and reactance referred to the stator. I'r is the rotor current referred to the stator. There will be stator core loss, when the supply is connected and the rotor core loss depends on the slip.

SIMULATION:

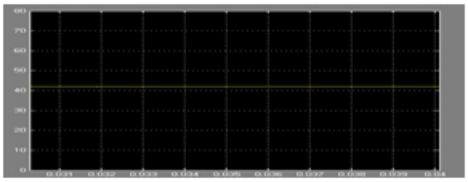




Solar system



Boost converter



Solar DC voltage

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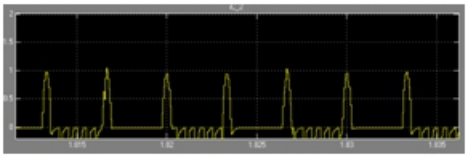
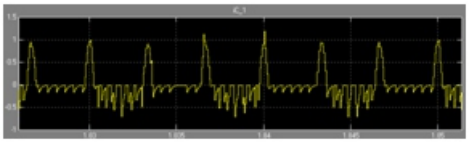
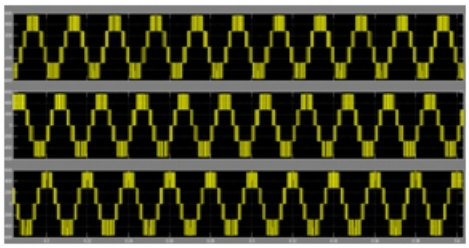


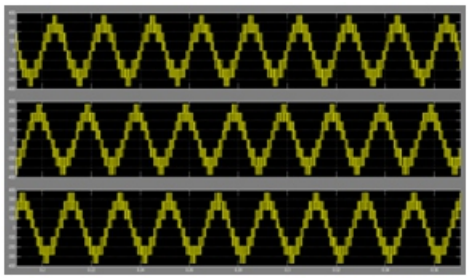
Capacitor current –iC1



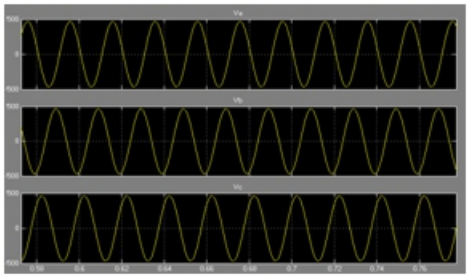
Capacitor current –iC2



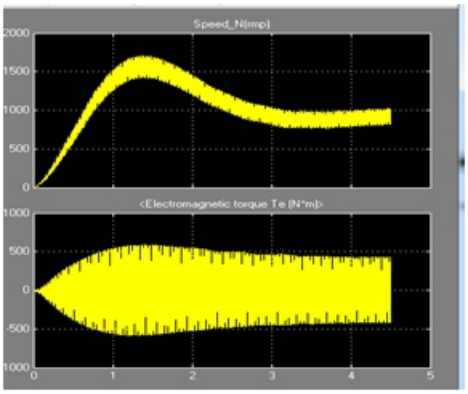
Line voltages of Inverter terminals



Line –Neutral voltages of Inverter terminals



Line voltages after filtering



Motor output

CONCLUSION:

This paper presents a new three phase multi level inverter with reduced switches.Multilevel inverters offer improved output waveforms and lower THD. In this topology less THD in the nine-level inverter compared with that in the seven-level inverters is connected PV inverters. This inverter provided to induction motor with smooth output and better voltage. Switching loss reduce in this topology than the common three phase multi-level-inverter.

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