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Comparative Analysis of 5 level and 3 level AC/DC Converter with Unity Power Factor at Input and Variable DC at Output

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Abstract:
Excessive use of non-linear loads, such as variable speed drives (VSDs), power factor improvement has become more difficult. The presence of harmonic currents cause power capacitors to absorb them, as capacitor impedance is inversely proportional to frequency. The effects are overheating and increased dielectric stress of power capacitors, which result in their premature failure. These traditional approaches can also interact with harmonics, leading to harmonic amplifications at resonant frequency, which can damage the capacitors or components of the system. A new integrated three-level ac–dc converter is presented. The proposed converter integrates the operation of the boost power factor correction and the three-level dc–dc converter. The converter is made to operate with two independent controllers—an input controller that performs power factor correction and regulates the dc bus and an output controller that regulates the output voltage. The input controller prevents the dc-bus voltage from becoming excessive while still allowing a single-stage converter topology to be used. The paper explains the operation of the three level and five level converter in detail for power factor correction and discusses its features and a procedure for its proper design.

Index Terms—AC–DC power conversion, single-stage power factor correction (PFC).

I. INTRODUCTION

Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Pulse Width Modulation variable speed drives are increasingly applied in many new industrial applications that require superior performance. Hence, different circuit configurations namely inverters have become popular and considerable interest by researcher are given on them. Variable voltage and frequency supply to A.C drives is invariably obtained from a three-phase voltage source inverter. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. THE ac–dc power supplies with transformer isolation are typically implemented with some sort of input power factor correction (PFC) to comply with harmonic standards such as IEC 1000-3-2 [1]. With the rapid rise in the use of electrical equipment in recent years, power converter manufactures are being pressed by regulatory to implement some form of PFC in their products. High power factor and low input current harmonics are more and more becoming mandatory performance criteria for power converters. Although it is possible to satisfy by adding passive filter elements to the traditional passive diode rectifiers/LC filter input combination. The result of this converter is very bulky and heavy due to the size of the low frequency inductors and capacitors. Active power factor correction techniques have been used in AC-DC converter to improve power factor and reduce the

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harmonics. Active power factor correction can be classified into two stage scheme. Two stages PFC contain two independent power stages in cascade with PFC stage and DC-DC regulator. The total efficiency of the two stages is lower because the total power has to be processed twice with two cascade power stage. Cost of the circuit is increase several schemes have developed to combine stage into one stage [13]. This paper introduces the new converter is interfaced to induction machine drive to check the performance of the drive characteristics, explains its basic operating principles and its modes of operation, and discusses its features and its design.

II. CONVERTER OPERATION

The proposed converter and its key waveforms are shown in Figs. 1 and 2, respectively. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, auxiliary winding 1 (Naux1/$N$1 = 2) cancels out the dc bus voltage so that the output voltage of diode bridge 1 (DB1) is zero and the currents in input inductors La1, Lb1, and Lc1 rise. When the primary voltage of the main transformer is negative, auxiliary winding 2 (Naux2/$N$1 = 2) cancels out the dc bus voltage so that the output voltage of diode bridge 2 (DB2) is zero and the currents in input inductors La2, Lb2, and Lc2 rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents fall since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages. The converter modes of operation are explained in this section. The typical converter waveforms are shown in Fig. 2. The equivalent circuit in each stage is shown in Fig. 3. The converter goes through the following modes of operation.

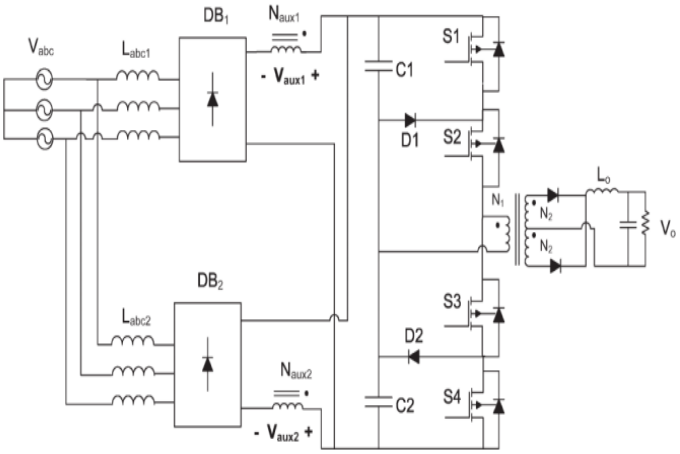

Fig.1. Proposed interleaved three-phase three-level converter.

Mode 1 ($t0 < t < t1$) [Fig. 3(a)]: During this interval, switches $S1$ and $S2$ are ON. In this mode, the energy from dc bus capacitor $C1$ flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 1 which is equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in $La1$, $Lb1$, and $Lc1$ rise.

Mode 2 ($t1 < t < t2$) [Fig. 3(b)]: In this mode, $S1$ is OFF, and $S2$ remains ON. The energy stored in $L1$($L1$ = Labc1) during the previous mode starts to transfer into the dc bus capacitors. The voltage that appears across auxiliary winding 1 is zero. The primary current of the main transformer circulates through $D1$ and $S2$. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-VL$.

Mode 3 ($t2 < t < t3$) [Fig. 3(c)]: In this mode, $S1$ and $S2$ are OFF. The energy stored in $L1$ still is transferring into the dc bus capacitor. The primary current of the transformer charges $C2$ through the body diodes of $S3$ and $S4$. Switches $S3$ and $S4$ are switched ON at the end of this mode.

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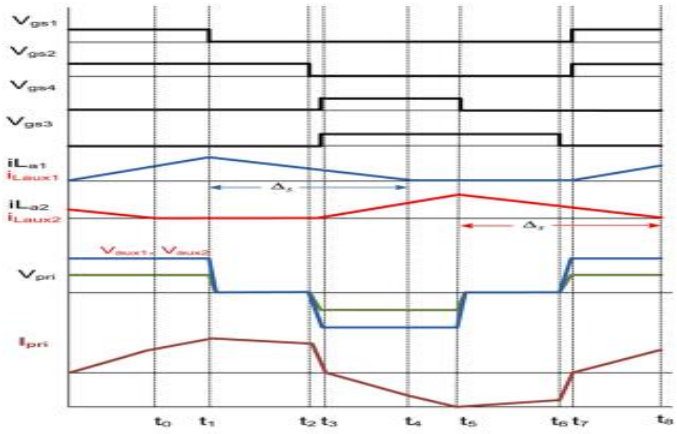


Fig.2.Typical waveforms describing the modes of operation.

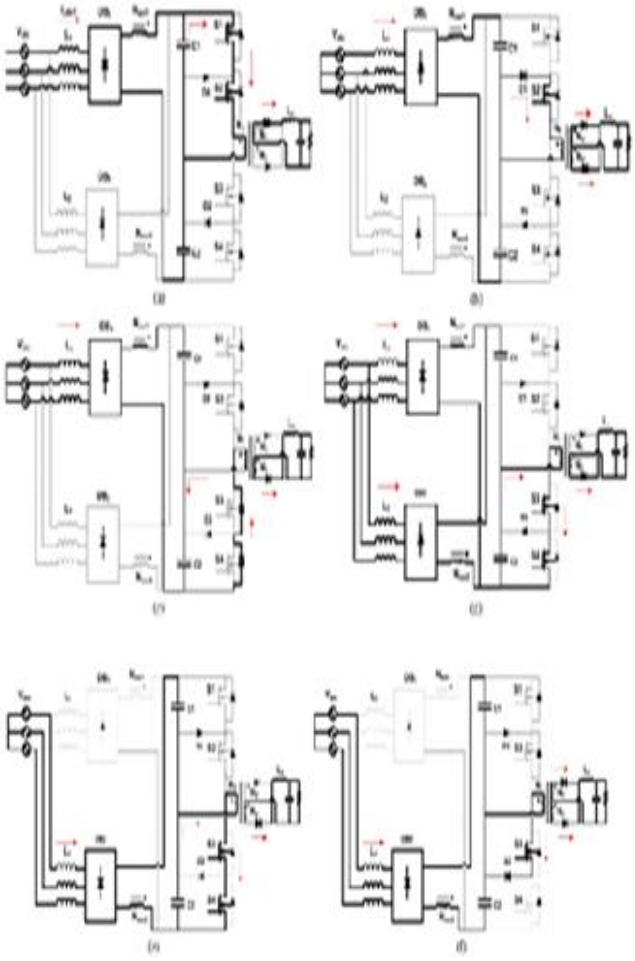
Mode 4 ($t3 < t < t4$) [Fig. 3(d)]: In this mode, $S3$ and $S4$ are ON, and the energy flows from capacitor $C2$ into the load. The voltage appears across auxiliary winding 2 which is equal to the dc bus voltage but acts like a magnetic switch and cancels out the dc bus voltage. The voltage across the boost inductors $L2$ ($L2 = L\text{abc}2$) becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases. This mode ends when the energy stored in $L1$ completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through modes 1–4 but with $S3$ and $S4$ ON instead of $S1$ and $S2$ and with DB2 instead of DB1.

Mode 5 ($t4 < t < t5$) [Fig. 3(e)]: In this mode, $S3$ and $S4$ are ON, and a symmetrical period begins. In this mode, the energy flows from capacitor $C2$ into the load. The voltage across the boost inductors $L2$ becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases.

Mode 6 ($t5 < t < t6$) [Fig. 3(f)]: In this mode, $S3$ is ON and $S4$ is OFF, and the primary current of the main transformer circulates through diode $D2$ and $S3$. The energy stored in the boost inductors $L2$ during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 7 ($t6 < t < t7$) [Fig. 3(g)]: In this mode, $S3$ and $S4$ are OFF, and the primary current of the transformer charges capacitor $C1$ through the body diodes of $S1$ and $S2$. The energy stored in the boost inductors $L2$ transfers into the dc bus capacitor.

Mode 8 ($t7 < t < t8$) [Fig. 3(h)]: In this mode, $S1$ and $S2$ are ON. In this mode, the energy from dc bus capacitor $C1$ flows to the output load. This mode ends when the energy in the inductors $L2$ completely transfers into the dc bus capacitors. Time $t8$ is the end of the switching cycle, and another switching cycle begins with the same modes.



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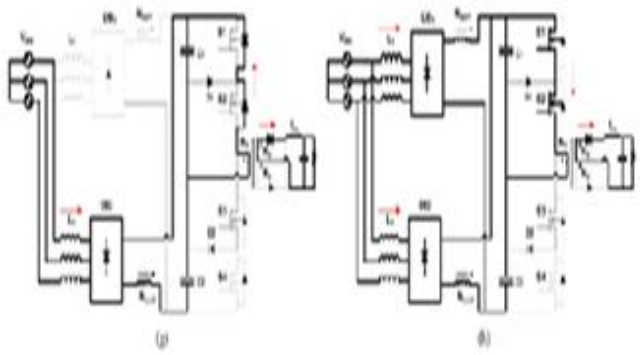

Fig.3. Modes of operation. (a) Mode 1 (t0 < t < t1). (b) Mode 2 (t1 < t < t2). (c) Mode 3 (t2 < t < t3). (d) Mode 4 (t3 < t < t4). (e) Mode 5 (t4 <t < t5). (f) Mode 6 (t5 < t < t6). (g) Mode 7 (t6 < t < t7). (h) Mode 8 (t7 < t < t8).

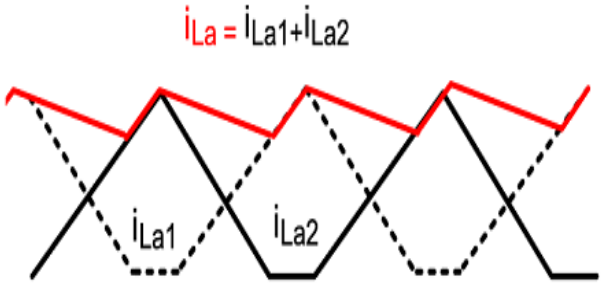

Fig. 4. Interleaving between two input inductor currents.

It should be noted that the input current is the summation of inductor currents *iL*1 and *iL*2 which are both discontinuous. However, by selecting appropriate values for *L*1 (= *La*1 =*Lb*1 = *Lc*1) and *L*2 (= *La*2 = *Lb*2 = *Lc*2) in such a way that two inductor currents such as *i*La1 and *i*La2 have to overlap each other, the input current can be made continuous as shown in Fig. 5, thus reducing the size of the input filter significantly. There is a natural 180◦ phase difference between the currents in *L*1 and the currents in *L*2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage—these two events occur 180◦ apart during a switching cycle.

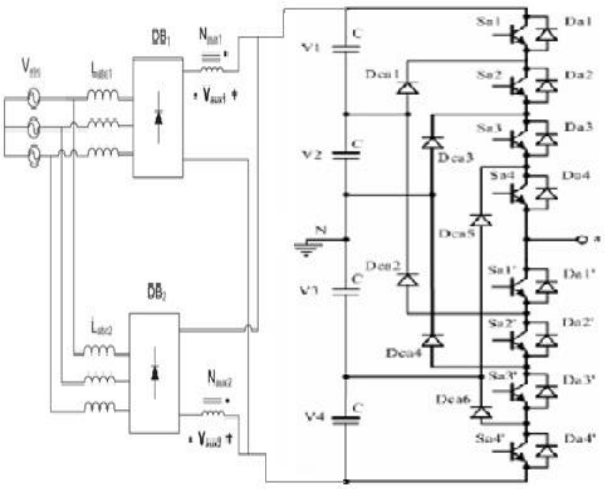

Fig.5. Proposed interleaved three-phase Five-level converter.

The 5 level converter reduces the harmonics, when it was first used in a three-level converter in which the mid-voltage level was defined as the neutral point. The 5 level converter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level converter needs m-1 capacitors on the dc bus. A three-phase five-level converter is shown in Fig.6. The dc bus consists of four capacitors, i.e., C1, C2, C3 and C4. For a dc bus voltage *Vdc*, the voltage across each capacitor is *Vdc*/4 and each device voltage stress will be limited to one capacitor voltage level, *Vdc*/4 through clamping diodes.

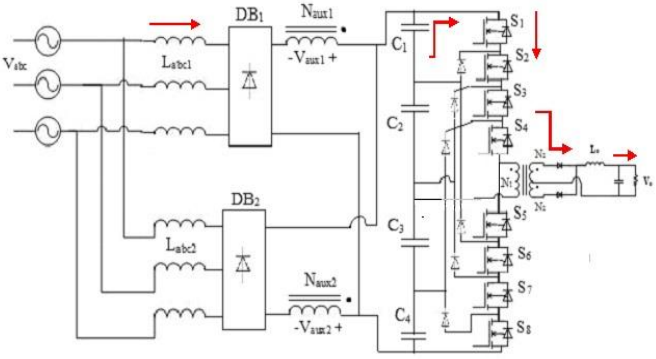

Fig.6. Mode 1 for the voltage level +Vdc/2.

During this interval, switches *S*1, *S*2, S3 and S4 switches are ON. In this mode, the energy from dc bus

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capacitor *C*1 and C2 flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 1 which is equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in *La*1, *Lb*1, and *Lc*1 rise.

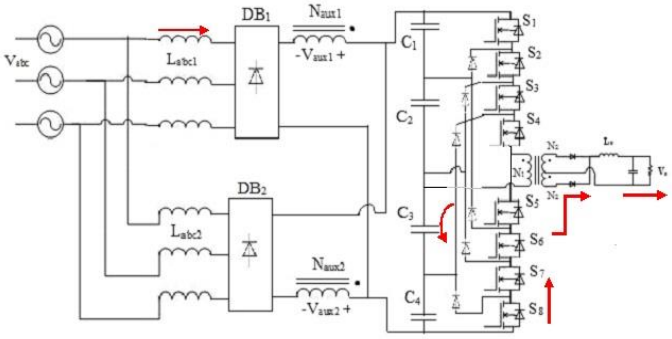

Fig.7. Mode 2 for the voltage level -Vdc/2.

During this interval, switches *S*5, *S*6, S7 and S8 switches are ON. In this mode, the energy from dc bus capacitor *C3* and C4 flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 2 which is equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in *La*2, *Lb*2, and *Lc*2 rise.

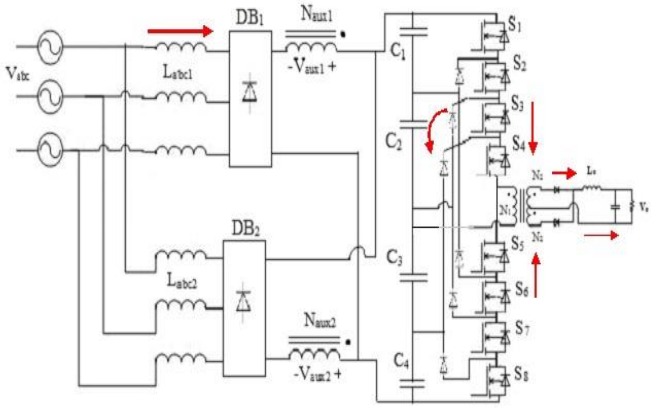

Fig.8. Mode 3 for the voltage level zero volts.

In this mode, *S*1, S2, S7 and S8 is OFF, and *S*3, S4, S5 and S6 remains ON. The energy stored in *L*1 and L2 during the previous mode starts to transfer into the dc bus capacitors. The voltage that appears across auxiliary winding 1 is zero.

III. CONVERTER ANALYSIS AND DESIGN

The analysis and the design of the proposed interleaved converter are almost identical to that presented and therefore are not presented here. Readers are referred to for details. In this paper, only differences in the analysis and the design are presented.

With respect to analysis, steady-state operating points are identified using a computer program such as the one presented. The only difference between the analysis of the proposed converter and the one is the analysis and design of the input inductors. In the proposed interleaved converter, there are two sets of inductors (*L*1 and *L*2) at the input side, with each set conducting half the current. The analysis needs to consider the current in both these sets instead of just one.

The values for *L*1 and *L*2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions but not so low as to result in excessively high peak currents. The worst case to be considered is the case when the converter operates with minimum input voltage and maximum load since, if the input current in each set of inductors is discontinuous under these conditions, it will be discontinuous for all other operating conditions, and thus, an excellent power factor will be achieved.

IV.MATLAB/SIMULINK RESULTS

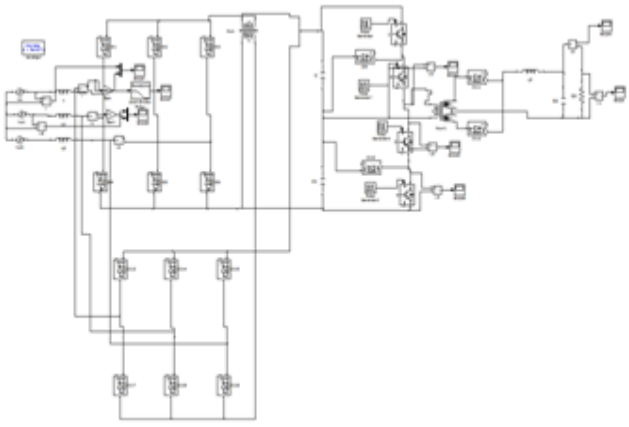

Fig.9. Matlab/Simulink model of proposed converter with half load.

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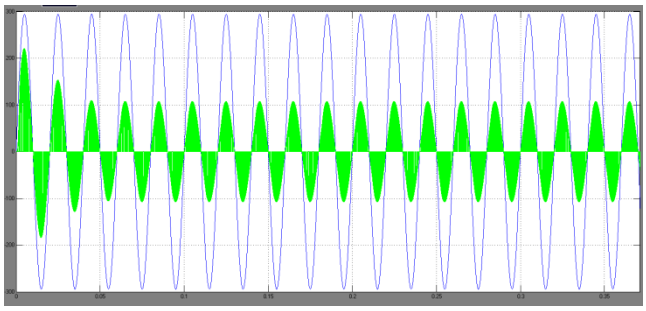

Fig.10. Simulated input wave form of the Voltage and current of the proposed converter with half load.

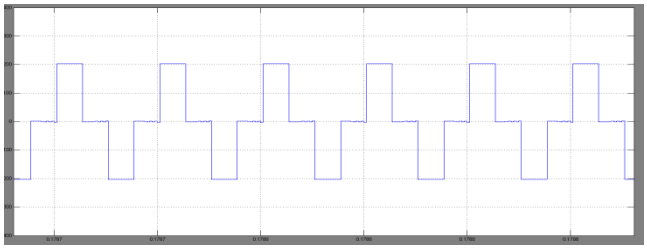

Fig.11. Simulated output wave form of the voltage at primary winding of the transformer of the proposed converter with half load.

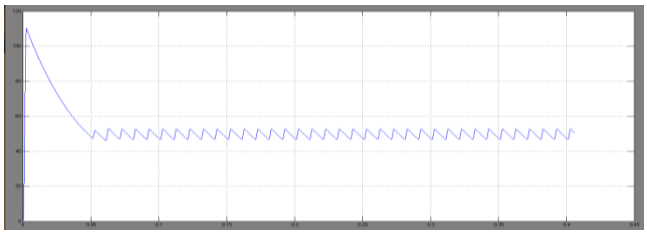

Fig.12. Simulated output wave form of the converter of the proposed converter with half load.

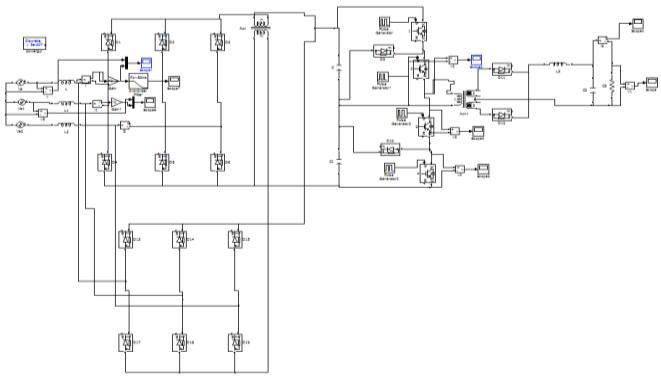

Fig 13. Matlab/Simulink model of the proposed converter with full load.

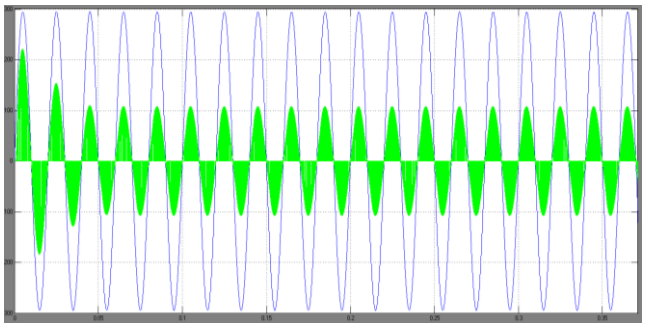

Fig.14.Simulated input wave form of the Voltage and current of the proposed converter with full load.

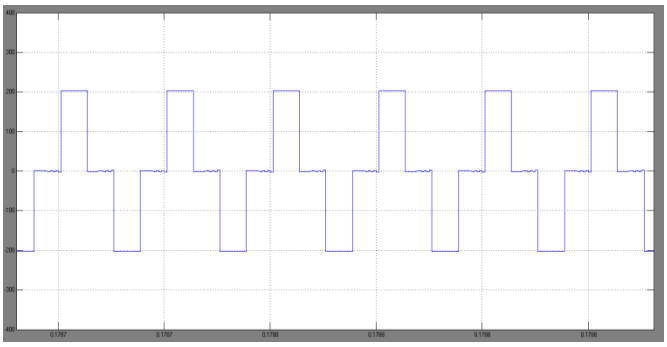

Fig.15. Simulated output wave form of the voltage at primary winding of the transformer of the proposed converter with full load.

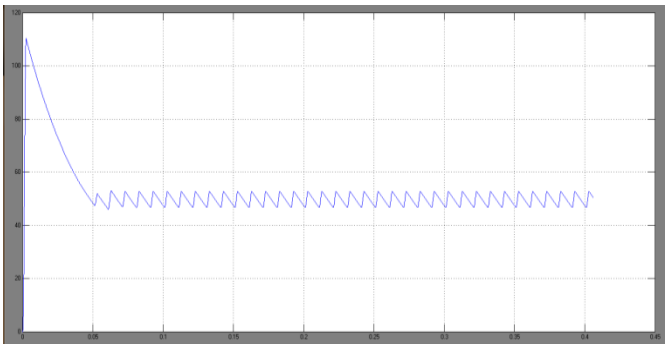

Fig.16. Simulated output wave form of the converter of the proposed converter with full load.

Case ii) Single phase single stage power factor corrected converter for five level

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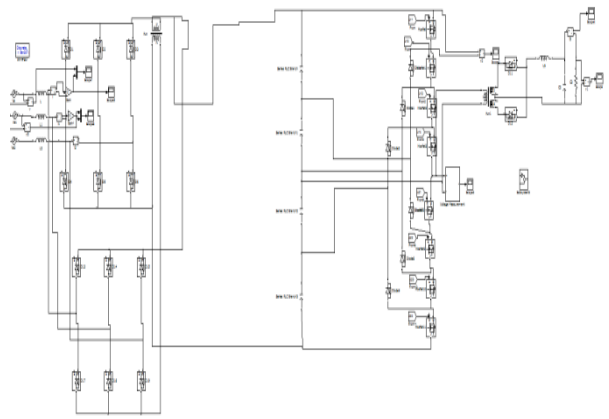

Fig.17. Simulink circuit for five level for PFC

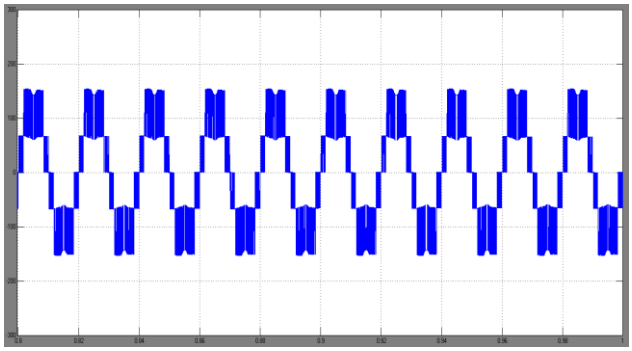

Fig.18. five level output at primary side of transformer

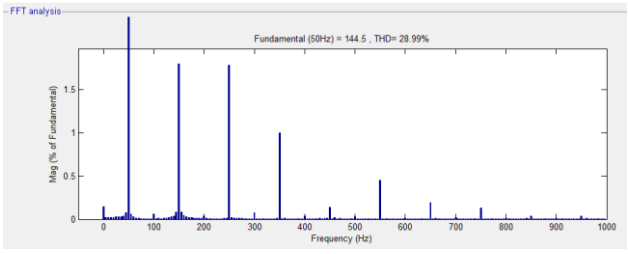

Fig.19.FFT window for five level output at primary side of transformer

V.CONCLUSION

In this paper, a new converter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. A new multilevel single-stage ac–dc converter is proposed in the paper. This converter is operated with two controllers, one controller that performs input PFC and a second controller that regulates the output voltage. The outstanding feature of this converter is that it combines the performance of two-stage converters with the reduction of cost of single-stage converters. The paper introduces the proposed five level converter reduces the harmonics compared to three level converter, explains its basic operating principles and modes of operation, and discusses its design with respect to different dc-bus voltages.

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