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Minimum rating 5 level D-STATCOM for Improvement of Power Quality

Maradana Udaykumar
M-Tech Student PG Scholar,
Department of Electrical & Electronics Engineering,
Sankethika Vidya Parishad Engineering College,
Vishakapatnam, Vishakapatnam (Dt), A.P, India.

P.Murari
Assistant Professor,
Department of Electrical & Electronics Engineering,
Sankethika Vidya Parishad Engineering College,
Vishakapatnam, Vishakapatnam (Dt), A.P, India.

Abstract:

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A new DSTATCOM topology with reduced dc link voltage and filter size is proposed using 5 level DSTATCOM logic controller. The distribution static compensator (DSTATCOM) is used for load compensation in power distribution network. In the presence of feeder impedance, the inverter switching distorts both the PCC voltage and the source currents. In this paper, a new topology for DSTATCOM applications with non stiff source is proposed. The compensation performance of any active filter depends on the voltage rating of dc-link capacitor. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. A new DSTATCOM topology with reduced dc link voltage is proposed. The topology consists of two capacitors: one is in series with the interfacing inductor of the active filter and the other is in shunt with the active filter. The series capacitor enables reduction in dc-link voltage while simultaneously compensating the reactive power required by the load, so as to maintain unity power factor without compromising DSTATCOM performance. The shunt capacitor, along with the state feedback control algorithm, maintains the terminal voltage to the desired value in the presence of feeder impedance with the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced. Detailed design aspects of the series and shunt capacitors are discussed in this paper. A simulation study of the proposed topology has been carried out using MATLAB/SIMULINK. Finally a 5level DSTATCOM controller is applied for further reduction of harmonics on source side.

Keywords:

DSTATCOM, PCC, Power factor, STATCOM and UPQC.

I.INTRODUCTION:

5 level DSTATCOM based D-STATCOM can provide fast and efficient reactive power support to maintain power system voltage stability. Rating of voltage source inverter (VSI) and size of the interfacing filter are two important issues while implementing DSTATCOM. In this paper, a new DSTATCOM topology has been proposed which simultaneously reduces the rating of VSI as well as size of interfacing filter with enhanced current compensation capabilities. Power quality in distribution systems affects all the connected electrical and electronics equipments. It is a measure of deviations in voltage, current, frequency of a particular system and associated components. In recent years, use of power converters in adjustable speed drives, power supplies etc. is continuously increasing. This equipment draws harmonics currents from AC mains and increases the supply demands. These loads can be grouped as linear (lagging power factor loads), nonlinear (current or voltage source type of harmonic generating loads), unbalanced and mixed types of loads. Some of power quality problems associated with these loads include harmonics, high reactive power burden, load unbalancing, voltage variation etc.

A survey on power quality problems is discussed for classification, suitable corrective and preventive actions to identify these problems. A variety of custom power devices are developed and successfully implemented to compensate various power quality problems in a distribution system. These custom power devices are classified as the DSTATCOM (Distribution Static Compensator), DVR (Dynamic Voltage Restorer) and UPQC (Unified Power Quality Conditioner). The DSTATCOM is a shunt-connected device, which can mitigate the current related power quality problems 5 level DSTATCOM logic can model or control non-linear systems that are difficult to model mathematically. The 5 level DSTATCOM logic is chosen for DSTATCOM as it gives appropriate performance for varying dynamics, higher convergence speed,

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robust and simple to design compared to conventional methods. Therefore, proposed topology will reduce weight, cost, rating, and size of the DSTATCOM with enhanced current compensation capability compared to conventional topology. Generally, a DSTATCOM suffers from high power rating requirement compared to load power and size while implemented in real time. Power rating of the SAPF is directly proportional to the load current to be compensated and dc link voltage. In traditional topology, the dc link voltage has much higher value than the maximum value of phase voltage to achieve satisfactory compensation performance. A higher dc link voltage increases the rating of VSI, makes VSI more bulky; IGBT switches must be rated for higher value of voltage and current. Ultimately the cost, size, weight, and power rating of VSI increases In traditional DSTATCOM topology, an L filter is used at front of VSI for shaping of the injected currents. L filter uses a bulky inductor, has a low slew rate for tracking the reference currents, produces large voltage drop across it, which in turn requires higher value of dc link voltage for proper compensation.

Therefore, L filter adds in cost, size, and power rating further. To reduce the size and power rating of the SAPF, several hybrid topologies have been proposed where an active filter is used with passive components [10]–[12]. In [11], authors have used a hybrid filter tuned at seventh harmonics and design is specific to motor drive applications only. In [12], authors have used a capacitor in series with interfacing filter to reduce the dc link voltage. However, reduction in dc link voltage is limited due to large drop in L type interfacing filter. Also, use of L filter makes filter bulky, bigger in size, and has a low slew rate for tracking the reference currents. In literature, LCL filter has been used as front end of VSI instead of L filter.

This scheme provides better reference tracking performance while using much lower value of passive components. Also, lower value of passive components ensures that the voltage drop across them is much less. Consequently, the dc link voltage will also be lesser while using LCL filter. In this paper, a new DSTATCOM topology has been proposed which combines the advantages of both series capacitor and LCL filter. LCL filter is used at the front end of the VSI, which is followed by the series capacitor. Proposed topology reduces the size of the passive components, the rating of the dc link voltage, and provides excellent reference current tracking performance simultaneously.

Therefore, the cost, size, weight, and power rating of the DSTATCOM will greatly reduce. Performances of proposed DSTATCOM with conventional & 5 level DSTATCOM controller based topologies are verified through extensive simulation using MATLAB/SIMULINK and results are also presented.

II.THREE-PHASE TRADITIONAL AND PROPOSED DSTATCOM TOPOLOGY:

Three-phase traditional and proposed DSTATCOM topology employed in distribution system. Fig. 1 is considered as traditional topology throughout this paper. It contains a three-phase, four-wire, two-level, neutral-point-clamped voltage source inverter. It requires two dc storage capacitors but each leg of the VSI can be controlled independently [8]. Vsabc and Isabc are source voltages and source currents of phases a, b, and c respectively. Feeder impedance in each phase is composed of resistance Rs and inductance Ls. Vt abc and Ilabc are the load terminal voltages and load currents in phases a, b, and c respectively. Loads used here have both linear and non-linear elements which may be balanced or unbalanced. Interfacing inductance and resistance of VSI in each phase are Lf and Rf respectively. DSTATCOM injected currents are if abc in respective phases.

The dc link capacitors are represented by Cdc1 =Cdc2 =Cdc, whereas voltages maintained across them areVdc1 = Vdc2 = Vdc = Vdcref respectively. Proposed topology, shown in Fig. 2, integrates DSTATCOM conventional topology with front end L filter replaced by LCL filter, followed by a series capacitor Cse. Introduction of LCL filter significantly reduces the size of the passive component of the VSI and improves the reference tracking performance. Addition of series capacitor to interfacing filter significantly reduces the dc link voltage and therefore the rating of the VSI. Here,R1andL1represent the resistance and inductance respectively at the filter side, R2and L2 represent the resistance and inductance respectively at the grid side, and C is the filter capacitance forming LCL filter part in all three phases.if1abc andif2abc are currents at filter and grid side in phase a, b, and c respectively. A damping resistance Rd is used in series with C to damp out resonance and to provide passive damping to the overall system, Vcabc and Icabc are voltages across and currents through the branch containing series C and Rd in three phases respectively.

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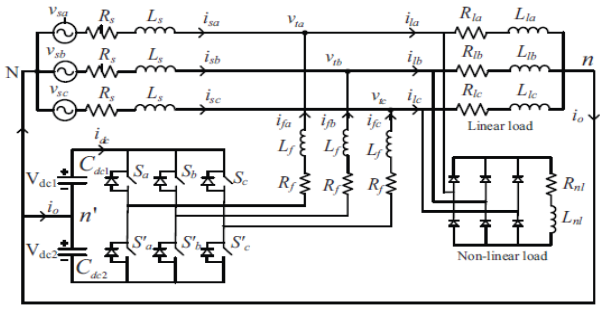

Fig. 1 Traditional DSTATCOM topology in distribution system.

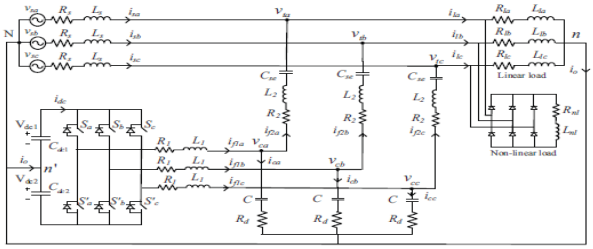

Fig. 2 Proposed DSTATCOM topology in distribution system.

III.REFERENCE CURRENT GENERATION:

DSTATCOM is operated in such a way that the source currents are balanced, sinusoidal, and in phase with respective terminal voltages. Also, average load power and losses in the VSI are supplied by the source. Since, source considered here is non-stiff in nature, direct use of terminal voltages to calculate reference currents will not provide satisfactory compensation.

Here, three phase reference currents (, , and) are generated using instantaneous symmetrical component theory [9] to satisfy all afore mentioned load compensation conditions simultaneously and are given as follows:

$$i^*_{f2a} = i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2b} = i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2c} = i_{lc} - i^*_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \quad (1)$$

where, V^+_{ta1}, V^+_{tb1}, and V^+_{tc1} are fundamental positive sequence voltages at the respective phase load terminal and $\Delta+1 = (V^+_{ta1})^2+(V^+_{tb1})^2+(V^+_{tc1})^2$. Here, Plavg represents average load power and Ploss represents the total looses in the inverter. Average load power is calculated using a moving average filter for better performance during transients and can have a window width of half cycle or full cycle depending upon the type of harmonics present in the load currents. Total losses in the inverter P_{loss}, computed using a proportional integral (PI) controller, helps in maintaining the dc link voltage ($v_{dc1}+v_{dc2}$) at a predefined reference value ($2V_{dcref}$) by drawing a set of balanced currents from the source and is given as follows:

$$P_{loss} = K_p e + K_i \int e\,dt \quad (2)$$

where, Kp, Ki, and e=2Vdcref - (vdc1+vdc2)are proportional gain, integral gain, and voltage error of the PI controller & 5 level DSTATCOM controller respectively. An error current control signal, u(t), is obtained by subtracting actual filter injected currents at grid side from the reference filter currents. u(t) is regulated around a predefined hysteresis band h using hysteresis current controller (HCC) and IGBT switching pulses are generated according to relationship given below: if u(t)≥h, then upper switch of a leg is TURN ON and lower switch is TURN OFF, else If u(t)≤-h, then upper switch of a leg is TURN OFF and lower switch is TURN ON.

IV. MATLAB/SIMULINK RESULTS:

Here simulation is carried out, 1). Conventional DSTATCOM for PQ Improvement Features using PI Controller 2).Modified DSTATCOM for PQ Improvement Features using PI Controller 3). Modified DSTATCOM for PQ Improvement Features using Intelligence based 5 level DSTATCOM Controller

Case 1: Conventional DSTATCOM for PQ Improvement Features using PI Controller

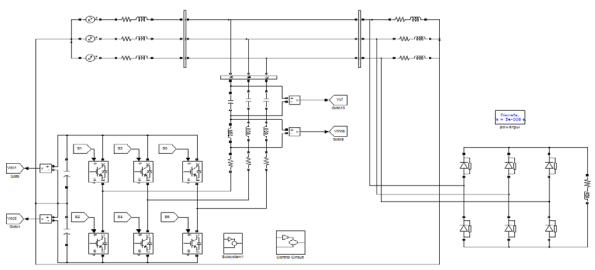

Fig.5 Matlab/Simulink Model of Conventional DSTATCOM for PQ Improvement Features using PI Controller

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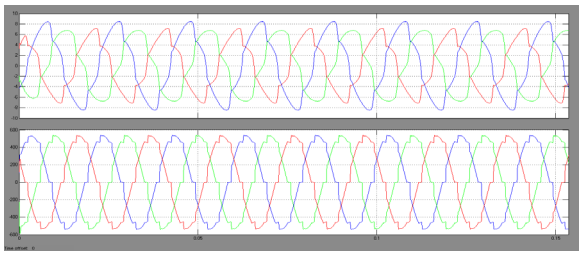

Fig.6 Simulated output wave form of the Source Current and Voltage of the Power system Network with Linear and Non-Linear load before Compensation.

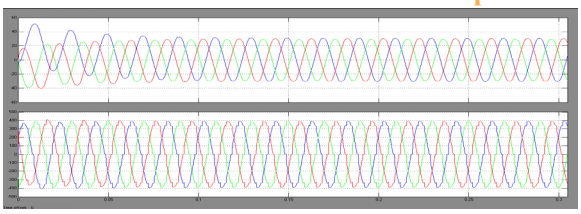

Fig.7 Simulated output wave forms of the Terminal current and voltage of Conventional method.

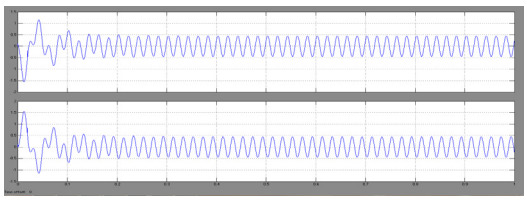

Fig.8 Simulated output wave forms of the Dc Capacitor voltages of Conventional method.

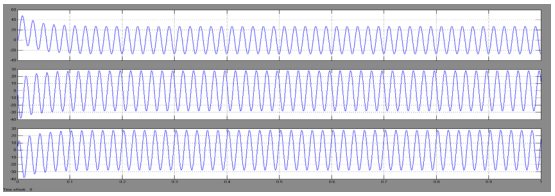

Fig.9 Simulated output wave forms of the Filter currents of Conventional method.

Case-2 Modified DSTATCOM for PQ Improvement Features using PI Controller

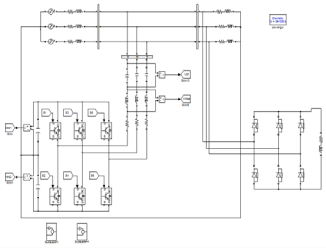

Fig.10Matlab/Simulink model of proposed neutral clamped VSI topology-based DSTATCOM (hybrid filter)

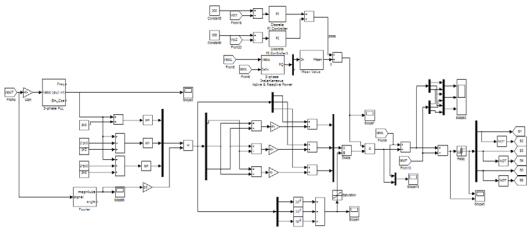

Fig.11 Matlab/Simulink model of Control circuit of proposed neutral clamped VSI topology-based DSTATCOM (hybrid filter).

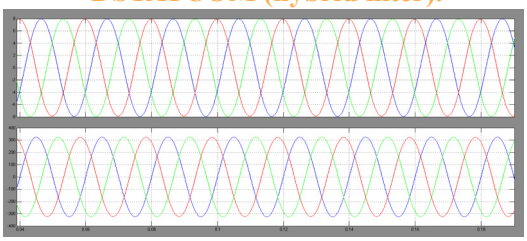

Fig.12 Simulated output wave forms of the Terminal current and voltage.

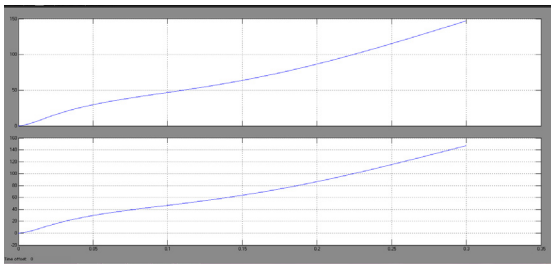

Fig.13 Simulated output wave forms of the Dc Capacitor voltages of the proposed concept.

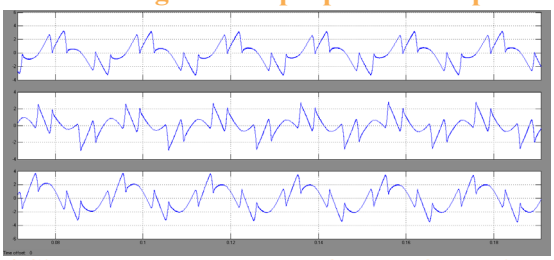

Fig.14 Simulated output wave forms of the Filter currents of the proposed concept.

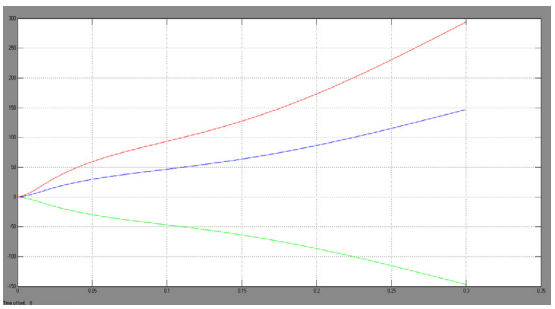

Fig.15 Simulated output wave forms of dc-link voltage (Vdc1 + Vdc2) of the proposed concept

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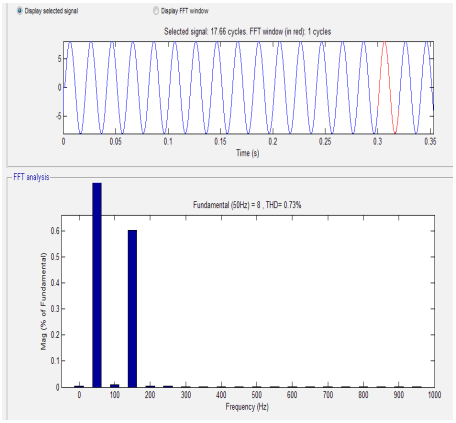

Fig.16 FFT analysis of source current

Fig.16 FFT analysis of source current of Modified DSTATCOM for PQ Improvement Features using PI Controller, get 0.73%.

Case-3 Modified DSTATCOM for PQ Improvement Features using Intelligence based 5

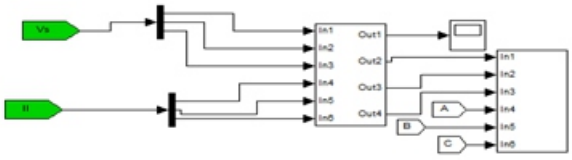

Fig.17 Matlab/Simulink model of proposed neutral clamped VSI topology-based With 5 level DSTATCOM

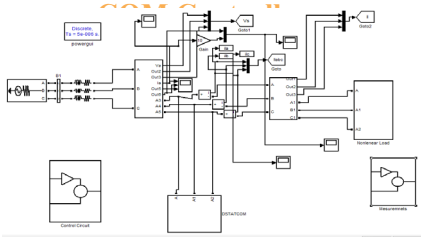

Fig.18 Matlab/Simulink model of Control circuit of proposed neutral clamped VSI topology-based With 5 level DSTATCOM controller.

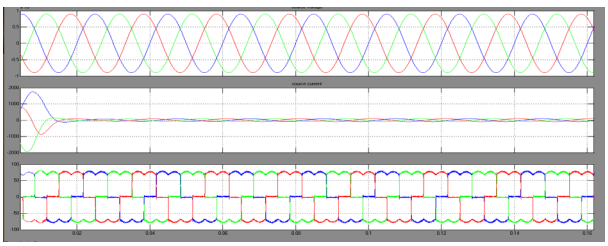

Fig.19 Simulated output wave forms of the Terminal current and voltage with 5 level DSTATCOM Controller

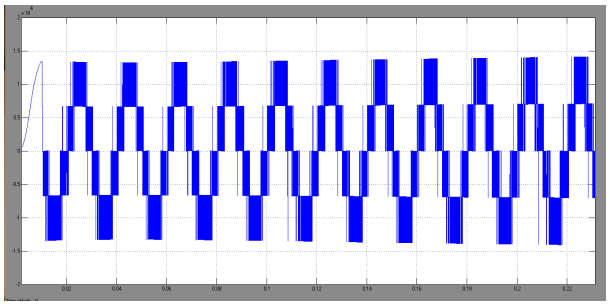

Fig.20 Voltage across top dc capacitor, series filter capacitor, and terminal voltage in phase-a with 5 level DSTATCOM controller.

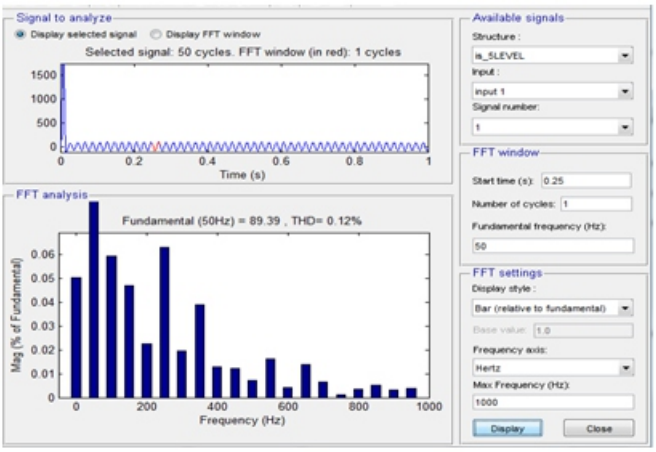

Fig.24 FFT analysis of source current

Fig.21 FFT analysis of source current of Modified DSTATCOM for PQ Improvement Features using 5 level DSTATCOM Controller, get 0.12%.

V.CONCLUSION:

The performance of DSTATCOM has been found satisfactory various control strategies. They are PI and 5 levels DSTATCOM controller by using the PI controller the harmonic percentage is 0.73% and at that same condition but PI replace with 5 levels DSTATCOM controller we get the 0.12%. In this concept PI replace with the 5 level DSTATCOM controller we get the better efficiency. The DC bus voltage of the DSTATCOM has also been regulated without much overshoot to desired value under concern control schemes. The cost, size, weight, and power rating of the DSTATCOM will be significantly reduced compared to traditional topology. A procedure to design LCL filter parameters and series capacitor has been presented. Effectiveness of the proposed DSTATCOM topology over traditional topology is verified through extensive simulation using Matlab/Simulink.

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