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Fuzzy Logic Controller Based Multifunctional D-STATCOM of Power Quality Improvement

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Abstract:

Distribution static compensator (DSTATCOM) is a shunt compensation device that is generally used to solve power quality problems in distribution systems. In an all-electric ship power system, power quality issues arise due to high-energy demand loads such as pulse loads. In this project a new algorithm to generate reference voltage for a distribution static compensator (DSTATCOM) operating in voltage-control mode. Three filter capacitors, one for each phase, are connected in parallel with the DSTATCOM to eliminate high-frequency switching components. The voltage across the filter capacitor is controlled by a dead-beat controller to maintain the AC bus voltage. The magnitude of the bus voltage is chosen as nominal value, i.e., 1.0 p.u., while its phase angle is obtained through a feedback loop that maintains the voltage across the DC storage capacitors.

The proposed scheme ensures that unity power factor (UPF) is achieved at the load terminal during nominal operation, which is not possible in the traditional method. Also, the compensator injects lower currents and, therefore, reduces losses in the feeder and voltage-source inverter. Nearly UPF is maintained, while regulating voltage at the load terminal, during load change. The state-space model of DSTATCOM is incorporated with the deadbeat predictive controller for fast load voltage regulation during voltage disturbances. DSTATCOM to tackle power-quality issues by providing power factor correction, harmonic elimination, load balancing, and voltage regulation based on the load requirement and simulation results are presented by using Matlab/Simulink platform.

Index Terms:

Current control mode, power quality (PQ),voltage-control mode, voltage-source inverter.

I. INTRODUCTION:

Power Quality (PQ) is the key to successful delivery ofquality product and operation of an industry. The increasedapplication of electronic loads and electronic controllerswhich are sensitive to the quality of power makes seriouseconomic consequences and of revenues loss each year. PoorPQ can cause malfunctioning of equipment performance,harmonics, voltage imbalance, sag and flicker problems,standing waves and resonance – are some of the issues thatadversely affect production and its quality leading to huge lossin terms of product, energy and damage to equipment. Thus, itbecomes imperative to be aware of quality of power grid andthe deviation of the quality parameters from the norms /standard such as IEEE-519 standard [1] to avoid breakdownor equipment damage.In present day distribution systems (DS), major powerconsumption has been in reactive loads.

The typical loads maybe computer loads, lighting ballasts, small rating adjustablespeeds drives (ASD) in air conditioners, fans, refrigerators,pumps and other domestic and commercial appliances aregenerally behaved as nonlinear loads. These loads drawlagging power-factor currents and therefore give rise toreactive power burden in the DS. Moreover, situation worsensin the presence of unbalanced and non-linear loads, affect the quality of source currents to a large extent. It affects thevoltage at point of common coupling (PCC) where the facilityis connected. This has adverse effects on the sensitiveequipment connected to PCC and may damage the equipmentappliances. Excessive reactive power demand increases feederlosses and reduces active power flow capability of the DS,whereas unbalancing affects the operation of transformers andgenerators [2-3]. In this paper, a five-level cascade H-bridge inverterbased DSTATCOM configuration has been presented.The adoption of cascade H-bridge inverter forDSTATCOM applications causes to decrease the devicevoltage and the output harmonics by increasing thenumber of output voltage levels.

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Inverter circuit is heartof DSTATCOM and various inverter topologies can beutilized in applications of DSTATCOM such as: cascadedh-bridge, neutral point clamped (NPC) and flyingcapacitor (FC) [4]. In particular, among these topologies,CHB inverters are being widely used because of theirmodularity and simplicity. Various modulation methodscan be applied to CHB inverters. There are variousmodulation methods, but phase shift modulation has usedin this paper. CHB inverters can also increase thenumber of output voltage levels easily by increasingthe number of H-bridges cells [5]. This paper presentsa DSTATCOM with a PI controller based five-levelCHB multilevel inverter for the current harmonic,voltage flicker and reactive power mitigation of thenonlinear load.

II. PROPOSED CONTROL SCHEME:

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Fig.1. It uses a three-phase, four-wire, two-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI [7]. Fig.2 shows the single-phase equivalent representation of Fig.1. Variable uis a switching function, and can be either +1 or -1 depending upon switching state. Filter inductance and resistance areL_fand R_f respectively. Shunt capacitorC_fc eliminates high-switching frequency components. First, discrete modeling of the system is presented to obtain a discrete voltage control law, and it is shown that the PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. Then, a procedure to design VSI parameters is presented. A proportional-integral (PI) controller is used to regulate the dc capacitor voltage at a reference value. Based on instantaneous symmetrical component theory and complex Fourier transform, a reference voltage magnitude generation scheme is proposed that provides the advantages of CCM at nominal load. The overall controller block diagram is shown in Fig. 3 These steps are explained as follows.

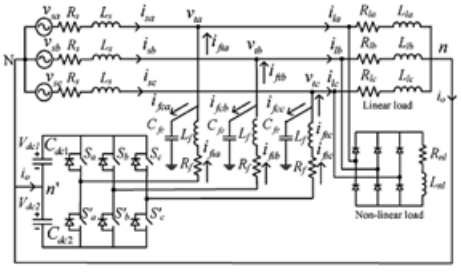

Fig.1.Circuit diagram of the DSTATCOM-compensated distribution system.

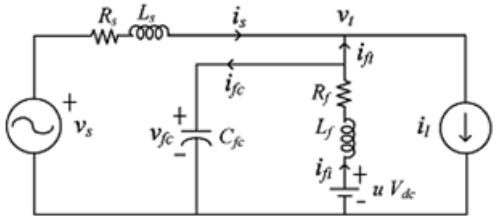

Fig.2 Single-phase equivalent circuit of DSTATCOM.

A. System Modeling and Generation of the Voltage-Control Law:

The state-space equations for the circuit shown in Fig. 2 are given by

$$x^{\cdot} = Ax + Bz \qquad (1)$$

$$A=\begin{bmatrix} 0 & \frac{1}{Cf_c} & 0 \\ -\frac{1}{L_f} & 0 & 0 \\ -\frac{1}{L_s} & 0 & -\frac{R_S}{L_s} \end{bmatrix}$$

$$B=\begin{bmatrix} 0 & -\frac{1}{Cf_c} & 0 \\ \frac{V_{dc}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix}$$

$$x=[v_{fc} \quad i_{fi} \quad i_s]^t,\ z=[u \quad i_{ft} \quad v_s]^t$$

The general time-domain solution of (1) to compute the state vector x(t) with known initial value x(t_0), is given as follows:

$$X(t) = X(e^{A(t-t_0)}\,x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}B\,z(\tau)\,d\tau \quad (2)$$

The equivalent discrete solution of the continuous state is obtained by replacing t_0= kT_d and t= (k+1)T_d as follows:

$$X(k+1) = e^{AT_d}x(k) + \int_{kT_d}^{T_d} e^{A(T_d+kt_d-\tau)}B\,z(\tau)\,d\tau \quad (3)$$

In (3), k and T_d represent the K_{th} sample and sampling period, respectively. During the consecutive sampling period, the value of z(τ) is held constant, and can be taken as z(k).After simplification and changing the integration variable, (3) is written as [12]

$$X(k+1) = e^{AT_d}x(k) + \int_{0}^{T_d} e^{A\lambda}B\lambda B\,z(K) \quad (4)$$

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$x(k+1) = G\,x(K) + H\,z(k)$ (5)

Where G and H are sampled matrices, with a sampling time of T_d. For small sampling time, matrices and are calculated as follows:

$$G=\begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix}$$

$$H=\begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda} B\lambda \quad (6)$$

$$= \int_0^{T_d} (I + A\lambda) B\lambda \quad (7)$$

From (6) and (7) $G_{11} = 1 - T_d^2/2L_F c_{fc}$,

$G_{12} = T_d/c_{fc} - T_d^2 R_f/2L_F c_{fc}$

$G_{13} = 0$,

$H_{11} = T_d^2 v_{dc}/2L_F c_{fc}$,

$H_{12} = -T_d/c_{fc}$,

$H_{13} = 0$. Hence, the capacitor voltage using (5) is given as

$$v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{f1} + H_{11} u(k) + H_{12}\, i_{f1}(k). \quad (8)$$

As seen from (8), the terminal voltage can be maintained at a reference value depending upon the VSI parameters v_{dc}, c_{fc}, L_f, R_f, and sampling time T_d. Therefore, VSI parameters must be chosen carefully. Let v_t^* be the reference load terminal voltage. A cost function J is chosen as follows [8]:

$$J = [v_{fc}(k+1) - v_t^*(k+1)^2 \quad (9)$$

The cost function is differentiated with respect to u(k) and its minimum is obtained at

The deadbeat voltage-control law, from (8) and (10), is given as

$$u_t^*(k) = \frac{v_t^*(k+1) - G_{11} v_{fc}(k) - G_{12} i_{f1}(k) - H_{12}\, i_{ft}(k)}{H_{11}} \quad (11)$$

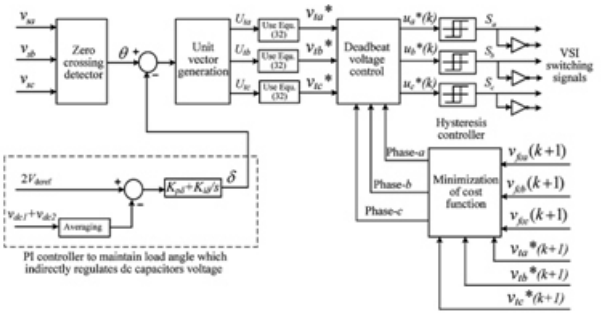

Fig.3 Overall block diagram of the controller to control DSTATCOM in a distribution system.

In (11), $v_t^*(k+1)$ is the future reference voltage which is unknown. One-step-ahead prediction of this voltage is done using a second-order Lagrange extrapolation formula as follows:

$$v_t^*(k+1) = 3\,v_t^*(k) - 3\,v_t^*(k-1) + v_t^*(k-2). \quad (12)$$

The term $v_t^*(k+1)$ is valid for a wide frequency range and when substituted in (11), yields to a one-step-ahead deadbeat voltage-control law. Finally $u_t^*(k)$, is converted into the ON/OFF switching command to the corresponding VSI switches using a deadbeat hysteresis controller.

B. Design of VSI Parameters:

DSTATCOM regulates terminal voltage satisfactorily, depending upon the properly chosen VSI parameters. The design procedure of these parameters is presented as follows.

Voltage Across DC Bus (V_{dc}):

The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

DC Capacitance (C_{dc}):

Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients. Let the total load rating be S kVA. In the worst case, the load power may vary from minimum to maximum that is, from 0 to S kVA. The compensator needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in the deviation of capacitor voltage from its reference value.

The voltage continues to decrease until the capacitor voltage controller comes into action. Consider that the voltage controller takes a ρ cycle that is ρT, seconds to act, where T the system is time period. Hence, maximum energy exchange by the compensator during transient will be. This energy will be ρ S T equal to the change in the capacitor stored energy. Therefore

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$$\frac{1}{2}C_{dc}\left(V_{dcref}^2 - V_{dc}^2\right) = pST \tag{13}$$

Where V_{dcref} and V_{dc} are the reference dc bus voltage and maximum-allowed voltage during transients, respectively. Hence

$$C_{dc} = \frac{2pST}{V_{dcref}^2 - V_{dc}^2}. \tag{14}$$

Here, S=10kVA, V_{dcref}=650V, ρ=1, and, V_{dcref}=0.8V_{dcref} or 1.2V_{dcref}. Using (14), capacitor values are found to be 2630 and 2152μF. The capacitor value 2600μF is chosen to achieve satisfactory performance during all operating conditions.

Filter Inductance(L_f) :

Filter inductance L_f should provide reasonably high switching frequency (f_{max}) and a sufficient rate of change of current such that VSI currents follow desired currents. The following equation represents inductor dynamics:

$$L_f\frac{di_{fi}}{dt} = -v_{fc} - R_f i_{fi} + V_{dc}. \tag{15}$$

The inductance L_f is designed to provide good tracking performance at a maximum switching frequency(f_{max}) which is achieved at the zero of the source voltage in the hysteresis controller. Neglecting R_f, L_f is given by

$$L_f = \frac{2V_m}{(2h_c)(2f_{max})} = \frac{0.5V_m}{h_c f_{max}} \tag{16}$$

Where $2h_c$ is the ripple in the current. With f_{max} = 10 kHz and h_c = 0.75 A (5% of rated current), the value L_f of using (16) is foundtobe21.8mH, and 22Mh is used in realizing the filter.

Shunt Capacitor (C_{fc}):

The shunt capacitor should not resonate with feeder inductance at the fundamental frequency (ω_0). Capacitance, at which resonance will occur, is given as

$$C_{fcr} = \frac{1}{\omega_o^2 L_s}. \tag{17}$$

For proper operation, C_{fc} must be chosen very small compared to C_{fcr}. Here, a value of 5μF is chosen which provides an impedance of 637 ohm atω_0. This does not allow the capacitor to draw significant fundamental reactive current.

III. CONTROLLER FOR DC BUS CAPACITOR VOLTAGE:

Average real power balance at the PCC will be

$$P_{pcc} = P_{lavg} + P_{loss} \tag{18}$$

Where P_{pcc},P_{1avg}, and P_{loss} are the average PCC power, load power, and losses in the VSI, respectively. The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle. Hence δ must be maintained P_{pcc}constant to keep constant. The voltage of the dc bus of DSTATCOM can be maintained at its reference value by taking inverter losses P_{loss} from the source. If the capacitor voltage is regulated to a constant reference valueP_{loss}, is a constant value. Consequently, δ is also a constant value. Thus, it is evident that dc-link voltage can be regulated by generating a suitable value δ of .This δ includes the effect of losses in the VSI and, therefore, it takes care of $P_{loss}$the term in its action. To calculate load angle δ, the averaged dc-link voltage (V_{dc1} + V_{dc2}) is compared with a reference voltage, and error is passed through a PI controller. The output of the PI controller, which is load angle δ, is given as follows:

$$\delta = K_{p\delta}\, e_{vdc} + K_{i\delta}\int e_{vdc}\, dt \tag{19}$$

Where $e_{vdc} = 2V_{dcref-(V_{dc1}+V_{dc2})}$ is the voltage error. Terms $K_{p\delta}$ and $K_{i\delta}$ are proportional and integral gains, respectively. δ must lie between 0 to 90^0 for the power flow from the source to PCC. Hence, controller gains must be chosen carefully.

IV. PROPOSED METHOD TO GENERATE REFERENCE TERMINAL VOLTAGES

Reference terminal voltages are generated such that, at nominal load, all advantages of CCM operation are achieved while DSTATCOM is operating in VCM. Hence, the DSTATCOM will inject reactive and harmonic components of load current.

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To achieve this, first the fundamental positive-sequence component of load currents is computed. Then, it is assumed that these currents come from the source and considered as reference source currents at nominal load. With these source currents and for UPF at the PCC, the magnitude of the PCC voltage is calculated. Let three-phase load currentsi_la,i_lb, and i_lcbe represented by the following equations:

$$i_{lj}(t) = \sum_{n=1}^{m} \sqrt{2}\, I_{lj\,n} \sin\left(n\,\omega t + \phi_{lj\,n}\right) \tag{20}$$

Where j= a, b, c represent three phases n, is the harmonic number, and m is the maximum harmonic orderϕ_{lan} represents the phase angle of the *n*th harmonic with respect to reference in phase-α and is similar to other phases. Using instantaneous symmetrical component theory, instantaneous zero-sequence$i_{la}{}^{0}(t)$, positive-sequence$i_{la}{}^{+}(t)$, and negative-sequence current $i_{la}{}^{-}(t)$, components are calculated as follows:

$$\begin{bmatrix} i_{la}^{0}(t) \\ i_{la}^{+}(t) \\ i_{la}^{-}(t) \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix} \tag{21}$$

Where α is a complex operator and defined by $e^{j2\Pi/3}$.

The fundamental positive-sequence component of load current $\bar{I}_{la1}^{+}$, calculated by finding the complex Fourier coeficient, is expressed as follows:

$$\bar{I}_{la1}^{+} = \frac{\sqrt{2}}{T} \int_0^T i_{la}^{+}(t)\, e^{-j(\omega t - 90^\circ)}\, dt. \tag{22}$$

$\bar{I}_{la1}^{+}$is a complex quantity, contains magnitude and phase angle information, and can be expressed in phasor form as follows:

$$\bar{I}_{la1}^{+} = \left|\bar{I}_{la1}^{+}\right| \angle \bar{I}_{la1}^{+}. \tag{23}$$

Hence, the instantaneous fundamental positive-sequence component of load current in phase-a,$\bar{I}_{la1}^{+}$is expressed as

$$i_{la1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t + \angle \bar{I}_{la1}^{+}\right). \tag{24}$$

The fundamental positive-sequence component of load currents must be supplied by the source at nominal load. Hence, it will be treated as reference source currents. For UPF at nominal operation, the nominal load angle δ_0 is used. By knowing$\bar{I}_{la1}^{+}$ fundamental positive-sequence currents in phases b and c can be easily computed by providing a phase displacement of $-{}^{2\Pi}/_{3}$and${}^{2\Pi}/_{3}$, respectively, and are given as

$$\begin{aligned} i_{sa}^{*} &= i_{la1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t - \delta_0\right) \\ i_{sb}^{*} &= i_{lb1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t - \frac{2\pi}{3} - \delta_0\right) \\ i_{sc}^{*} &= i_{lc1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t + \frac{2\pi}{3} - \delta_0\right). \end{aligned} \tag{25}$$

When reference source currents derived in (25) are supplied by the source, three-phase terminal voltages can be computed using the following equations:

$$v_{tj}(t) = v_{sj}(t) - L_s \frac{a i_{sj}}{dt} - R_s i_{sj}^{*}. \tag{26}$$

Let the rms value of reference terminal and source voltages be $V_t{}^{*}$ and V, respectively. For UPF, the source current and terminal voltage will be in phase. However, to obtain the expression of V*independent of δ_0 , we assume the PCC voltage as a reference phasor for the time-being. Hence, phase-a quantities, by considering UPF at the PCC, will be

$$\begin{aligned} v_{ta}(t) &= \sqrt{2}\, V_t^{*} \sin \omega t \\ i_{sa}^{*} &= \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin \omega t \\ v_{sa}(t) &= \sqrt{2}\, V \sin\left(\omega t + \delta_0\right). \end{aligned} \tag{27}$$

Substituting (27) into (26), the phasor equation will be

$$V_t^{*} \angle 0 = V \angle \delta_0 - \left(R_s + jX_s\right) \left|\bar{I}_{la1}^{+}\right| \angle 0. \tag{28}$$

Simplifying the above equation

$$V_t^{*} = V \cos\delta_0 + jV \sin\delta_0 - \left|\bar{I}_{la1}^{+}\right| R_s - j \left|\bar{I}_{la1}^{+}\right| X_s. \tag{29}$$

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Equating real and imaginary parts of both sides of (29), the following equation is obtained:

$$V\cos\delta_0 = V_t^* + |\bar{I}_{la1}^+|\,R_s$$
$$V\sin\delta_0 = |\bar{I}_{la1}^+|\,X_s. \quad (30)$$

To remove δ_0 from (30), both sides are squared and added to obtain the following:

$$V^2 = (V_t^* + |\bar{I}_{la1}^+|\,R_s)^2 + (|\bar{I}_{la1}^+|\,X_s)^2. \quad (31)$$

After rearranging (31), the expression for reference load voltage magnitude will be

$$V_t^* = \sqrt{V^2 - (|\bar{I}_{la1}^+|\,X_s)^2} - |\bar{I}_{la1}^+|\,R_s. \quad (32)$$

Finally, using v_t^* from (32), the load angle from (19), and the phase-a source voltage as reference, three-phase reference terminal voltages are given as

$$v_{ta}^*(t) = \sqrt{2}\,V_t^*\sin(\omega t - \delta)$$
$$v_{tb}^*(t) = \sqrt{2}\,V_t^*\sin\left(\omega t - \frac{2\pi}{3} - \delta\right)$$
$$v_{tc}^*(t) = \sqrt{2}\,V_t^*\sin\left(\omega t + \frac{2\pi}{3} - \delta\right). \quad (33)$$

V.MATLAB/SIMULINK RESULTS:

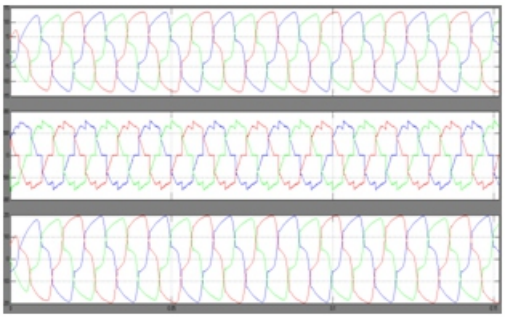

Fig.4. Simulation results for without Dstatcom

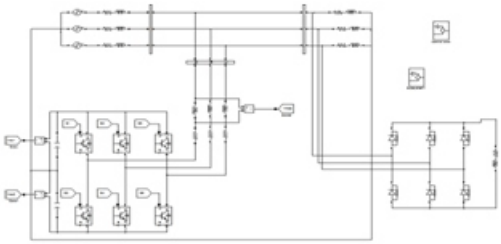

Fig.5.Simulink circuit forconventional system

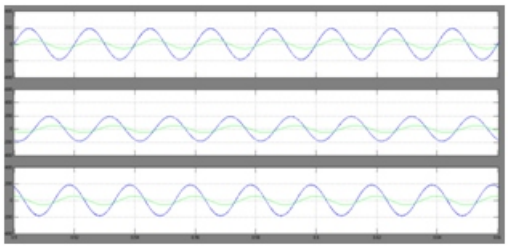

Fig. 6. Terminal voltages and source currents using the conventional method.(a) Phase a (b) Phase b. (c) Phase c.

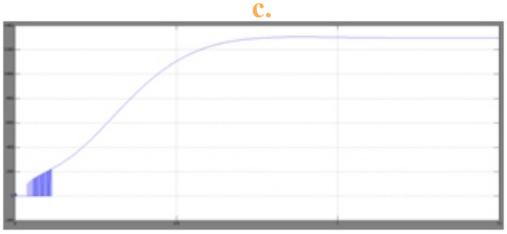

Fig.7. voltage at the dc bus

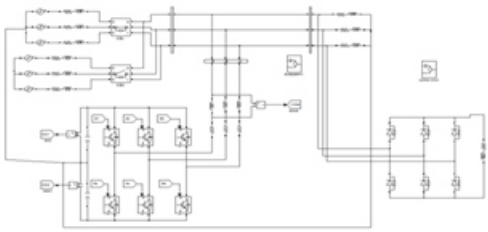

Fig.8.Simulink circuit for proposed system with PI controller

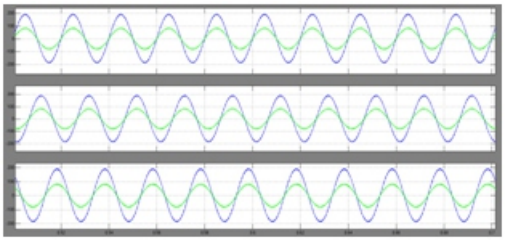

Fig. 9. Terminal voltages and source currents using the proposed method using PI controller.(a) Phase a (b) Phase b. (c) Phase c.

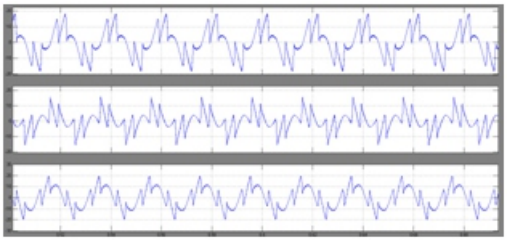

Fig.10. simulation results for compensation currents

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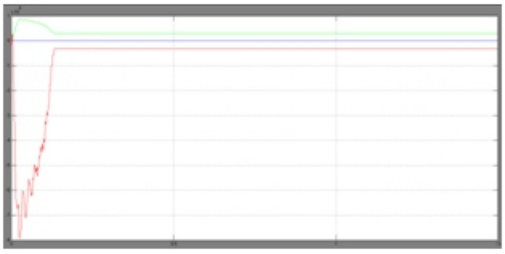

Fig. 11. Load reactive power , compensator reactive power, and reactive power at PCC for Proposed method with pi controller.

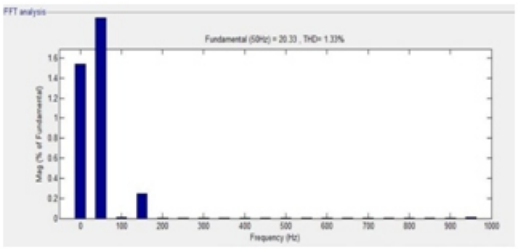

Fig.12. FFT analysis for source current by using PI controller

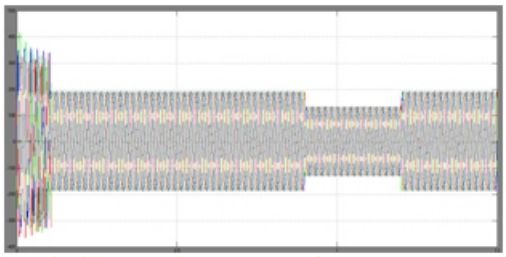

Fig.13. Simulation results for source voltage during sag

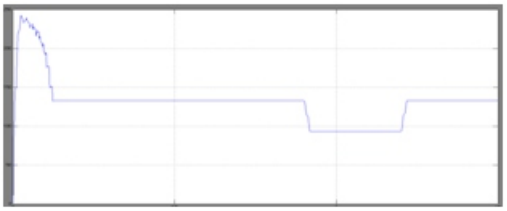

Fig.14. simulation result for RMS value of source voltage during sag

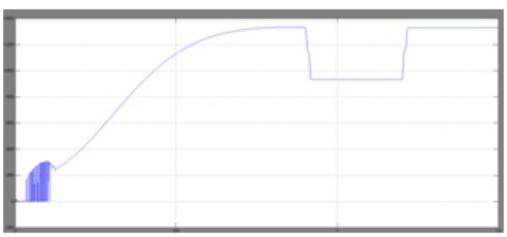

Fig 15. Simulation results for dc link voltage

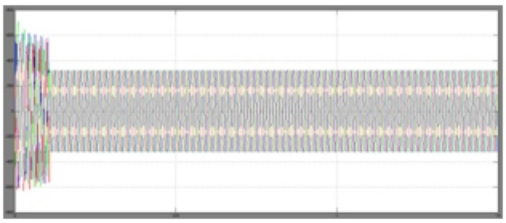

Fig.16. Simulation results for load voltage after compensation

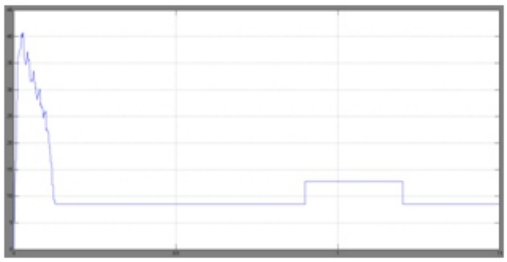

Fig.17. simulation results for compensation current of statcom

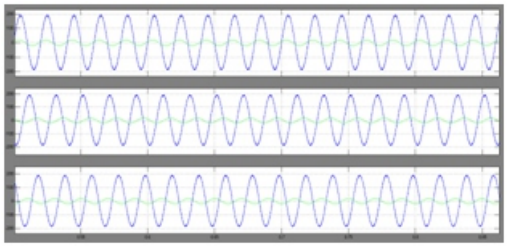

Fig. 18. Terminal voltages and source currents using the proposed method using fuzzy controller.(a) Phase a (b) Phase b. (c) Phase c.

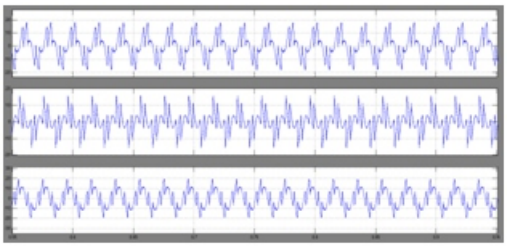

Fig.19. simulation results for compensation currents

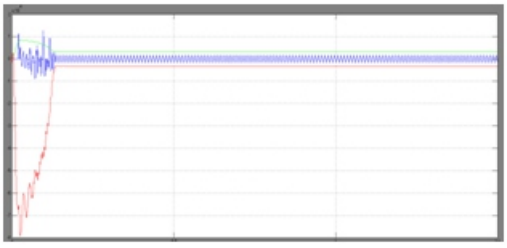

Fig. 20. Load reactive power , compensator reactive power, and reactive power at PCC for Proposed method with pi controller

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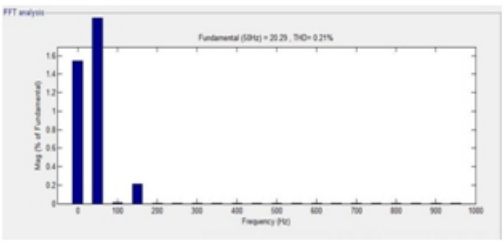

Fig.21. FFT analysis for source current by using FL controller.

VI.CONCLUSION:

In this paper, a control algorithm has been proposed for the generation of reference load voltage for a voltage-controlled DSTATCOM. The performance of the proposed scheme is compared with the traditional voltage-controlled DSTATCOM. The proposed method provides the following advantages:

1) At nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF;

2) Nearly UPF is maintained for a load change;

3) Fast voltage regulation has been achieved during voltage disturbances.

4) Losses in the VSI and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme.

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